

## 1. Product profile

### 1.1 General description

Passivated sensitive gate 4-Q triac in a SOT54 plastic package

### 1.2 Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage of 600V
- Sensitive gate in four quadrants

### 1.3 Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

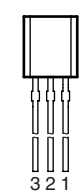
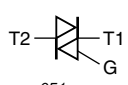
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{DRM}}$	repetitive peak off-state voltage		-	-	600	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{lead}} \leq 38\text{ °C}$ ; see <a href="#">Figure 4</a> and <a href="#">1</a>	-	-	1	A
<b>Static characteristics</b>						
$I_{\text{GT}}$	gate trigger current	$V_{\text{D}} = 12\text{ V}$ ; $T_{\text{j}} = 25\text{ °C}$ ; T2+ G-; see <a href="#">Figure 6</a>	-	-	3	mA
		$V_{\text{D}} = 12\text{ V}$ ; $T_{\text{j}} = 25\text{ °C}$ ; T2- G-	-	-	3	mA
		$V_{\text{D}} = 12\text{ V}$ ; $T_{\text{j}} = 25\text{ °C}$ ; T2+ G+	-	-	3	mA
		$V_{\text{D}} = 12\text{ V}$ ; $T_{\text{j}} = 25\text{ °C}$ ; T2- G+	-	-	5	mA

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 <p>SOT54 (TO-92)</p>	 <p>sym051</p>
2	G	gate		
3	T1	main terminal 1		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
Z0103MA	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 38\text{ °C}$ ; see <a href="#">Figure 4</a> and <a href="#">1</a>	-	1	A
$di_T/dt$	rate of rise of on-state current	$I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $di_G/dt = 100\text{ mA}/\mu\text{s}$ ; T2+ G+	-	50	A/ $\mu\text{s}$
		$I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $di_G/dt = 100\text{ mA}/\mu\text{s}$ ; T2- G+	-	20	A/ $\mu\text{s}$
		$I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $di_G/dt = 100\text{ mA}/\mu\text{s}$ ; T2+ G-	-	50	A/ $\mu\text{s}$
		$I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $di_G/dt = 100\text{ mA}/\mu\text{s}$ ; T2- G-	-	50	A/ $\mu\text{s}$
$I_{GM}$	peak gate current		-	1	A
$P_{GM}$	peak gate power		-	2	W
$T_{stg}$	storage temperature		-40	150	°C
$T_j$	junction temperature		-	125	°C
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $t_p = 16.7\text{ ms}$ ; $T_{j(init)} = 25\text{ °C}$	-	8.5	A
		full sine wave; $t_p = 20\text{ ms}$ ; $T_{j(init)} = 25\text{ °C}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	8	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; sin-wave pulse	-	0.32	A <sup>2</sup> s
$P_{G(AV)}$	average gate power		-	0.1	W

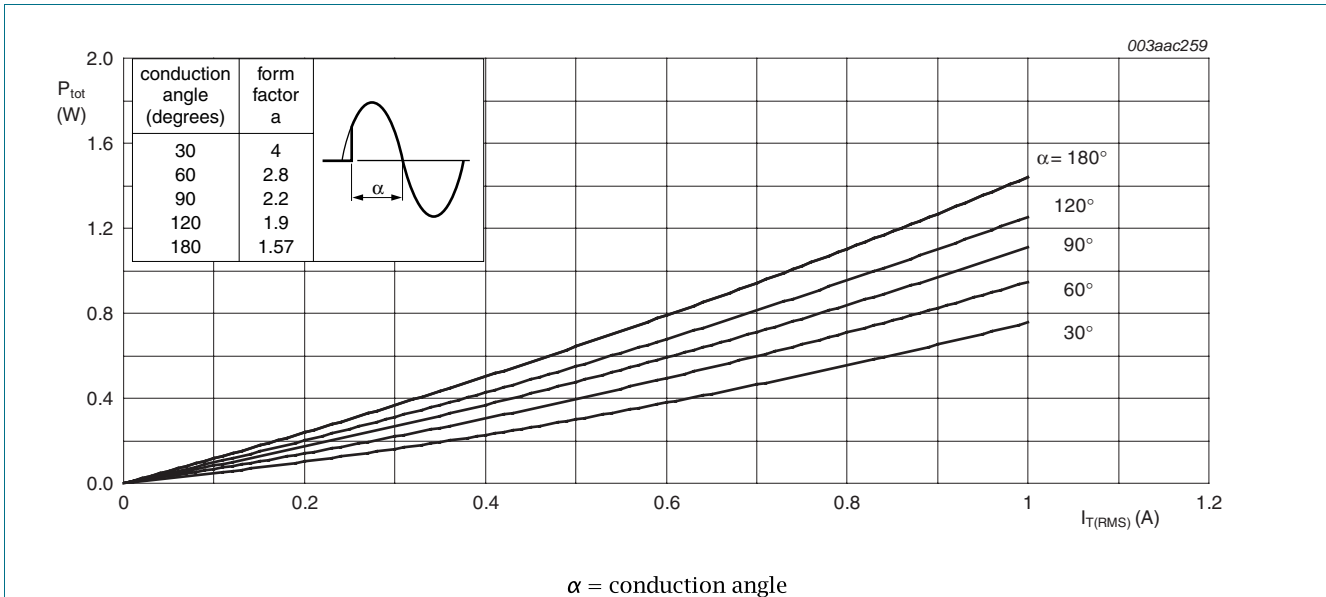


Fig 1. Total power dissipation as a function of RMS on-state current; maximum values

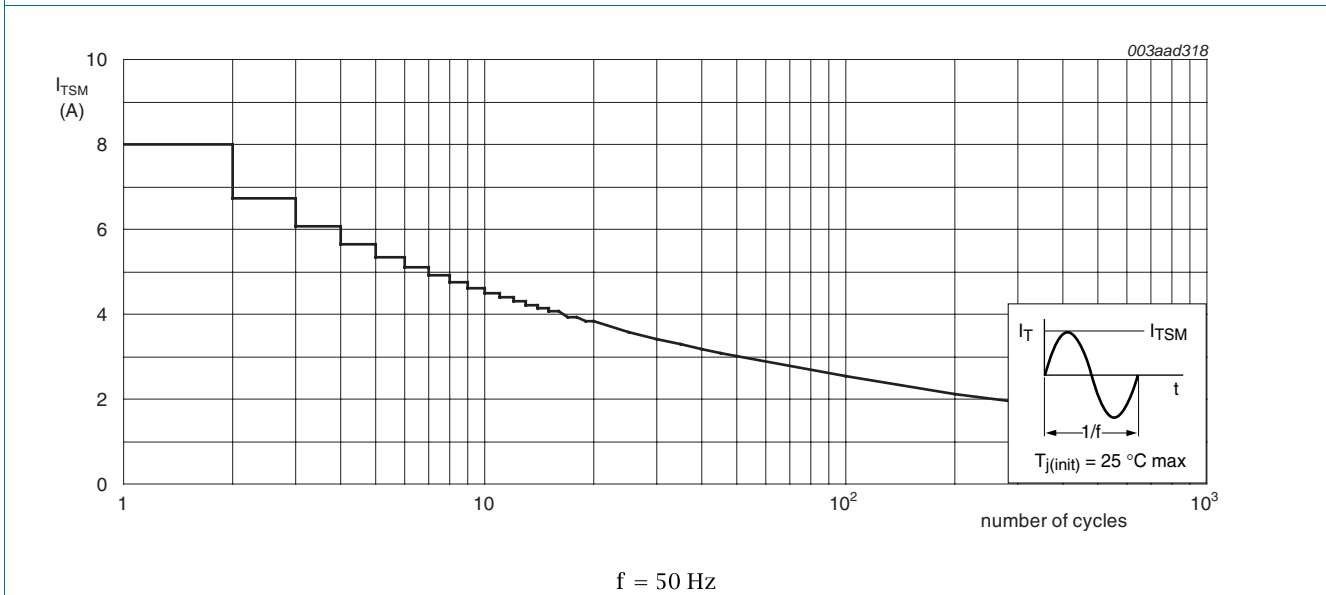
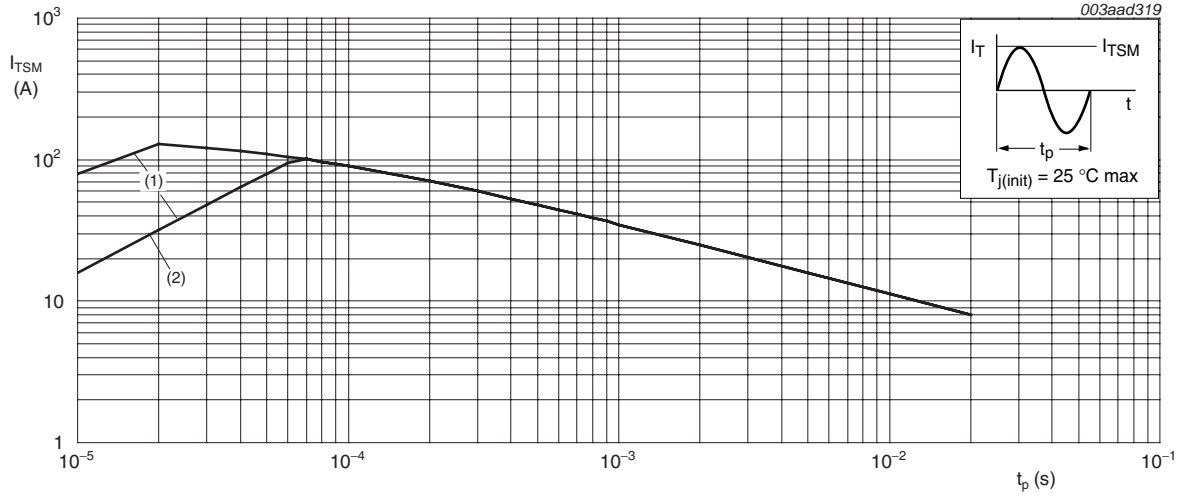


Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$  ms; (1) is  $dI_T/dt$  limit;  
 (2) is T2 – G + quadrant limit

Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

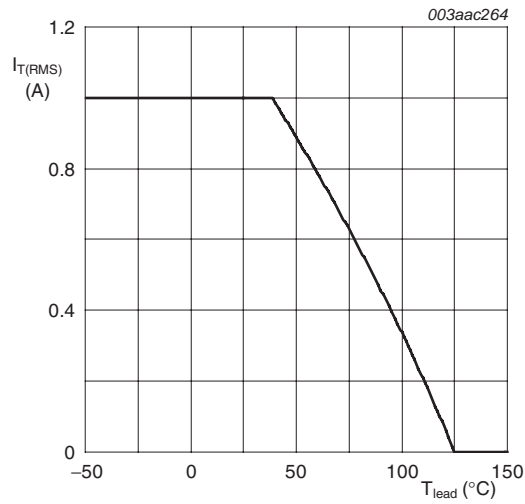
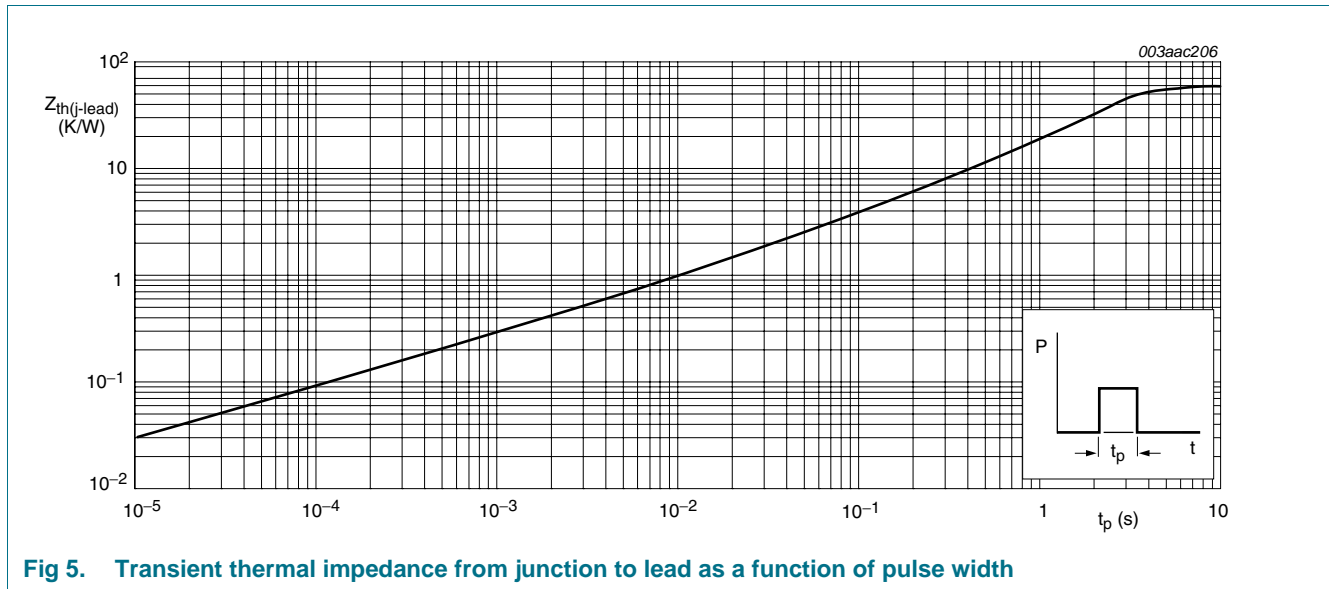


Fig 4. RMS on-state current as a function of lead temperature; maximum values

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	150	-	K/W
$R_{th(j-lead)}$	thermal resistance from junction to lead	Full cycle; see <a href="#">Figure 5</a>	-	-	60	K/W

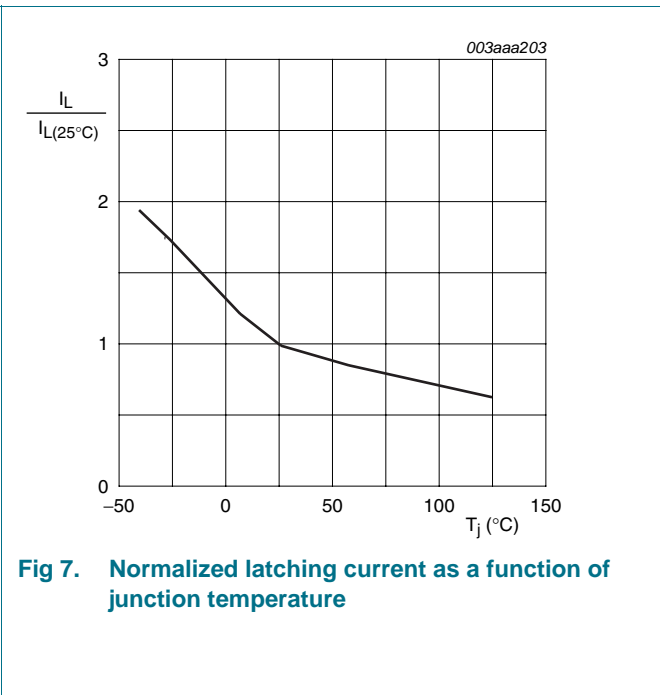
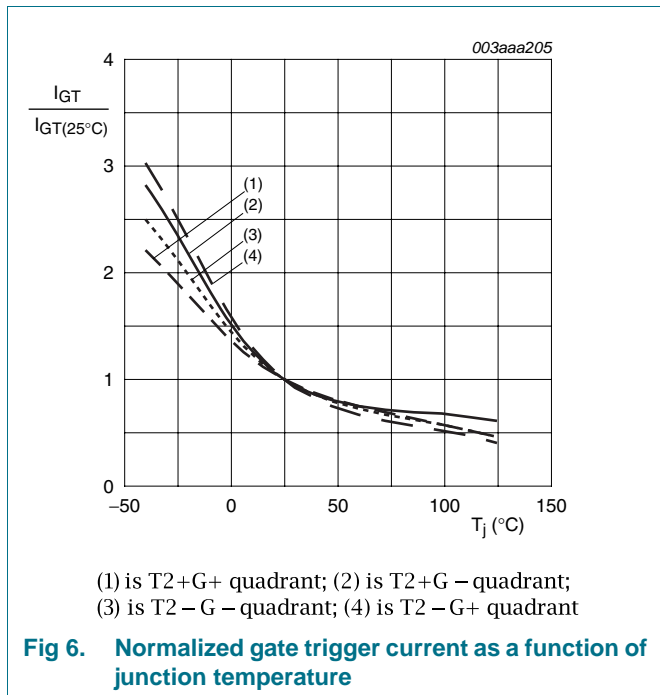


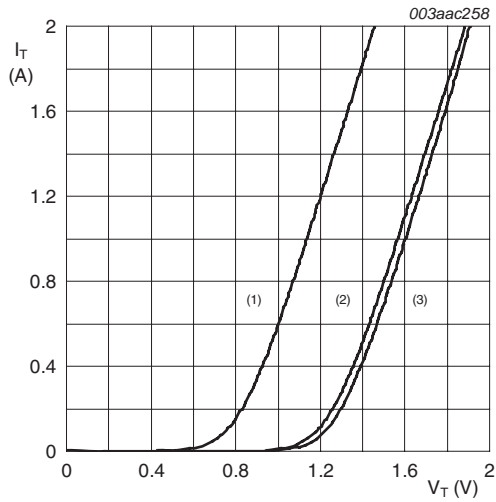
**Fig 5. Transient thermal impedance from junction to lead as a function of pulse width**

## 6. Characteristics

Table 6. Characteristics

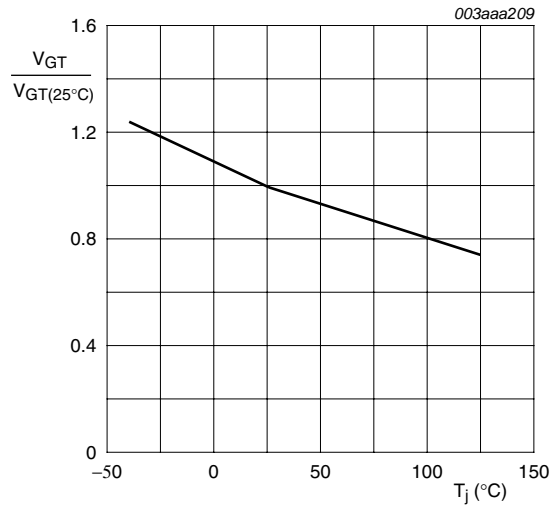
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; T2+ G-;$ see <a href="#">Figure 6</a>	-	-	3	mA
		$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; T2- G-$	-	-	3	mA
		$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; T2+ G+$	-	-	3	mA
		$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; T2- G+$	-	-	5	mA
$I_L$	latching current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; I_G = 0.1\text{ A}; T2+ G-;$ see <a href="#">Figure 7</a>	-	-	15	mA
		$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; I_G = 0.1\text{ A}; T2+ G+$	-	-	7	mA
		$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; I_G = 0.1\text{ A}; T2- G+$	-	-	7	mA
		$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; I_G = 0.1\text{ A}; T2- G-$	-	-	7	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	-	7	mA
$V_T$	on-state voltage	$I_T = 1\text{ A};$ see <a href="#">Figure 8</a>	-	1.3	1.6	V
$V_{GT}$	gate trigger voltage	$I_T = 0.1\text{ A}; V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	-	-	1.3	V
		$I_T = 0.1\text{ A}; V_D = 600\text{ V}; T_j = 125\text{ }^\circ\text{C}$	0.2	-	-	V
$I_D$	off-state current	$V_D = 600\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	-	0.5	mA
<b>Dynamic characteristics</b>						
$dV_{D}/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}; T_j = 110\text{ }^\circ\text{C};$ gate open circuit; see <a href="#">Figure 11</a>	10	-	-	V/ $\mu$ s
$dV_{com}/dt$	rate of rise of commutating voltage	$V_D = 400\text{ V}; T_j = 110\text{ }^\circ\text{C};$ $di_{com}/dt = 0.44\text{ A/ms};$ gate open circuit	0.5	-	-	V/ $\mu$ s



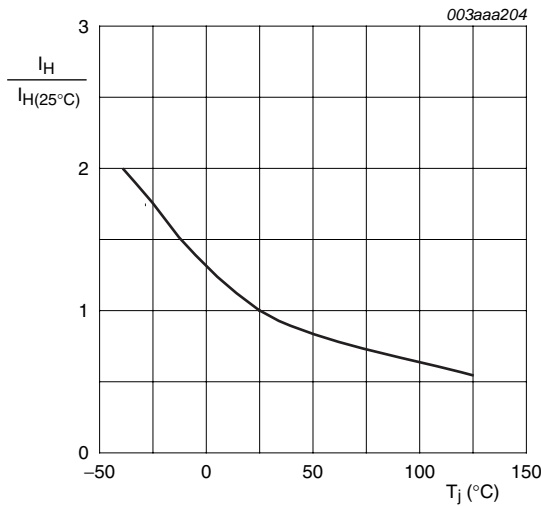


$V_0 = 1.254 \text{ V}; R_s = 0.31 \Omega$   
 (1)  $T_j = 125 \text{ }^\circ\text{C}$ ; typical values  
 (2)  $T_j = 125 \text{ }^\circ\text{C}$ ; maximum values  
 (3)  $T_j = 25 \text{ }^\circ\text{C}$ ; maximum values

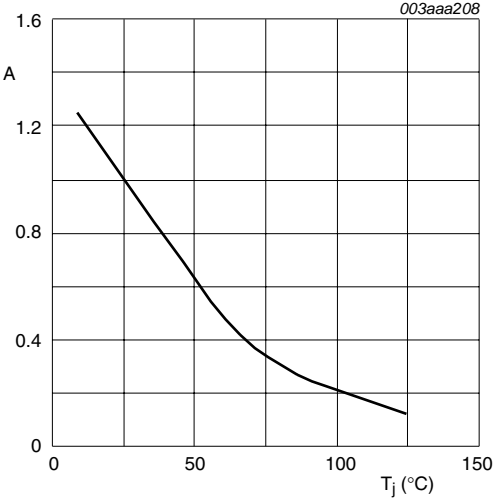
**Fig 8. On-state current as a function of on-state voltage**



**Fig 9. Normalized gate trigger voltage as a function of junction temperature**



**Fig 10. Normalized holding current as a function of junction temperature**



$$A = \frac{dV_D/dt}{dV_{D(25^\circ\text{C})}/dt}$$

Fig 11. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values



7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

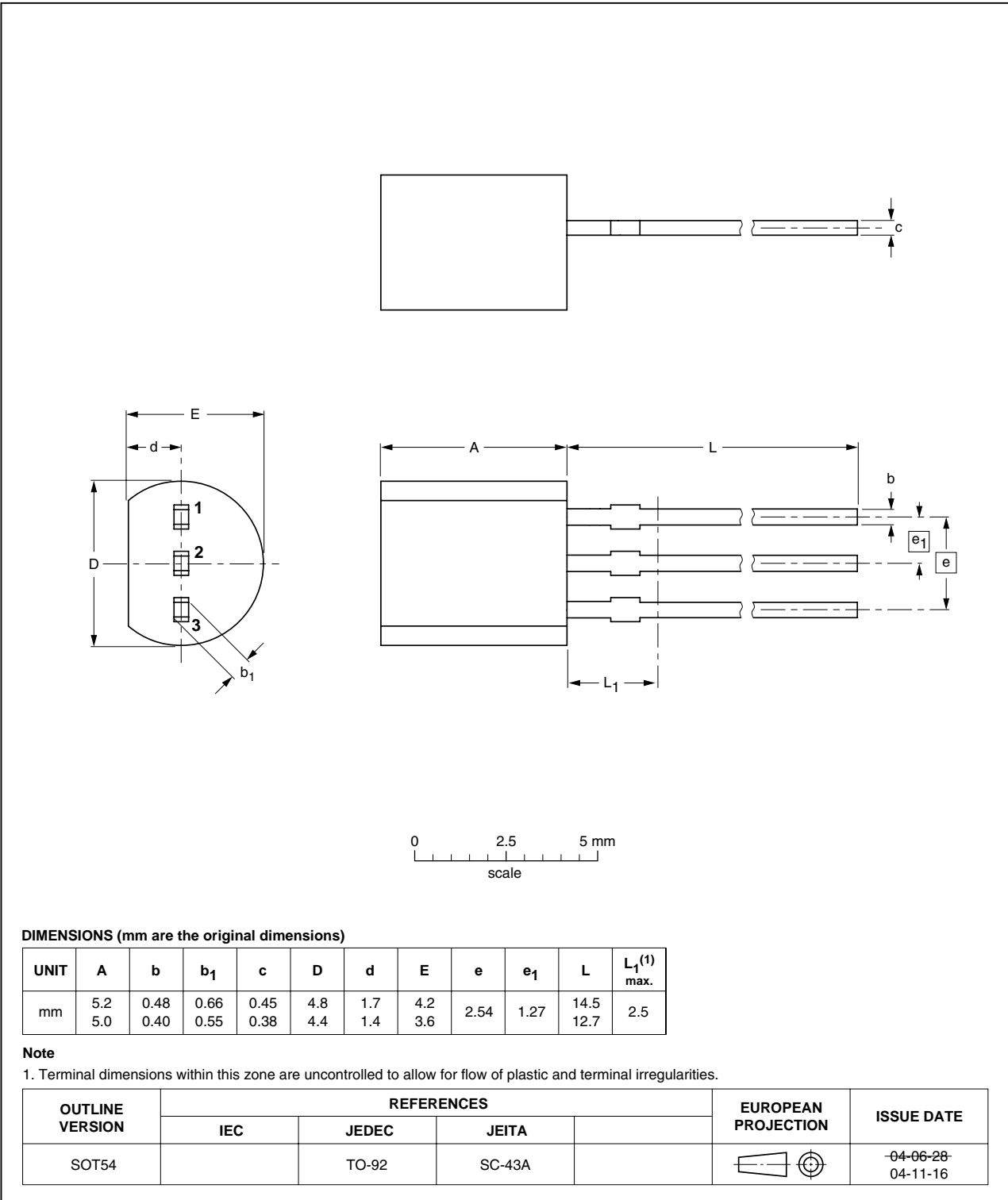


Fig 12. Package outline SOT54 (TO-92)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
Z0103MA_3	20090805	Product data sheet	-	Z0103_07_09_SERIES-02
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number Z0103MA separated from data sheet Z0103_07_09_SERIES-02.</li></ul>		
Z0103_07_09_SERIES-02 (9397 750 10102)	20020912	Product data	-	Z0103_07_09_SERIES-01
Z0103_07_09_SERIES-01 (9397 750 09419)	20020411	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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