

HA1630D08

Dual CMOS High Drive Operational Amplifier

REJ03D0860-0200

Rev.2.00

Nov 30, 2007

Description

HA1630D08 is a low power dual CMOS operational amplifier featuring high output current with typical current supply of 340 μ A for both channels (2.7 - 5.5 V). This IC designed to operate from a single power supply and have full swing outputs. Available in MMPAK-8 and TSSOP-8 package, the miniature size of this IC not only allows compact integration in portable devices but also minimizes distance of signal sources (sensors), thus reducing external noise pick up prior to amplification. This IC exhibit excellent current drive-power ratio capable of 600 Ω load driving and yet resistant to oscillation for capacitive loads up to 400 pF.

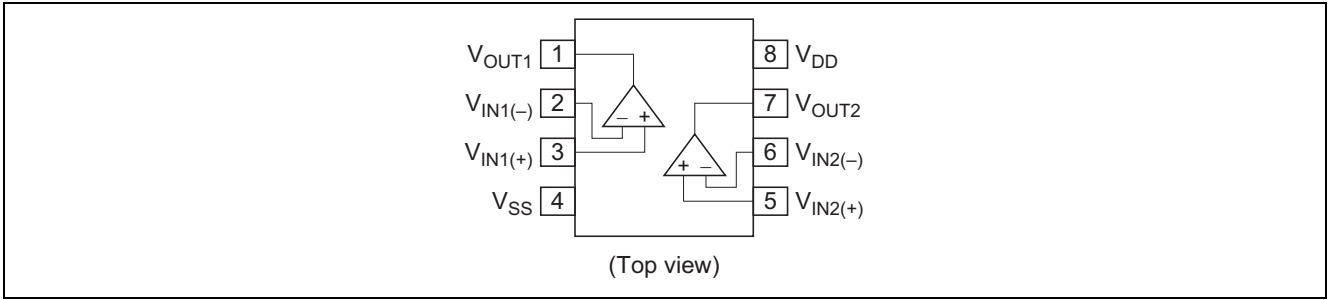
Features

- Low supply current $I_{DD} = 340 \mu\text{A Typ (}V_{DD} = 3 \text{ V, }R_L = \text{No load)}$
- Low voltage operation $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$
- Low input offset voltage $V_{IO} = 6 \text{ mV Max}$
- Low input bias current $I_{IB} = 1 \text{ pA Typ}$
- High output current $I_{OSOURCE} = 30 \text{ mA Typ (}V_{DD} = 3.0 \text{ V, }V_{OH} = 2.5 \text{ V)}$
 $I_{OSINK} = 30 \text{ mA Typ (}V_{DD} = 3.0 \text{ V, }V_{OL} = 0.5 \text{ V)}$
- Input common voltage range includes ground

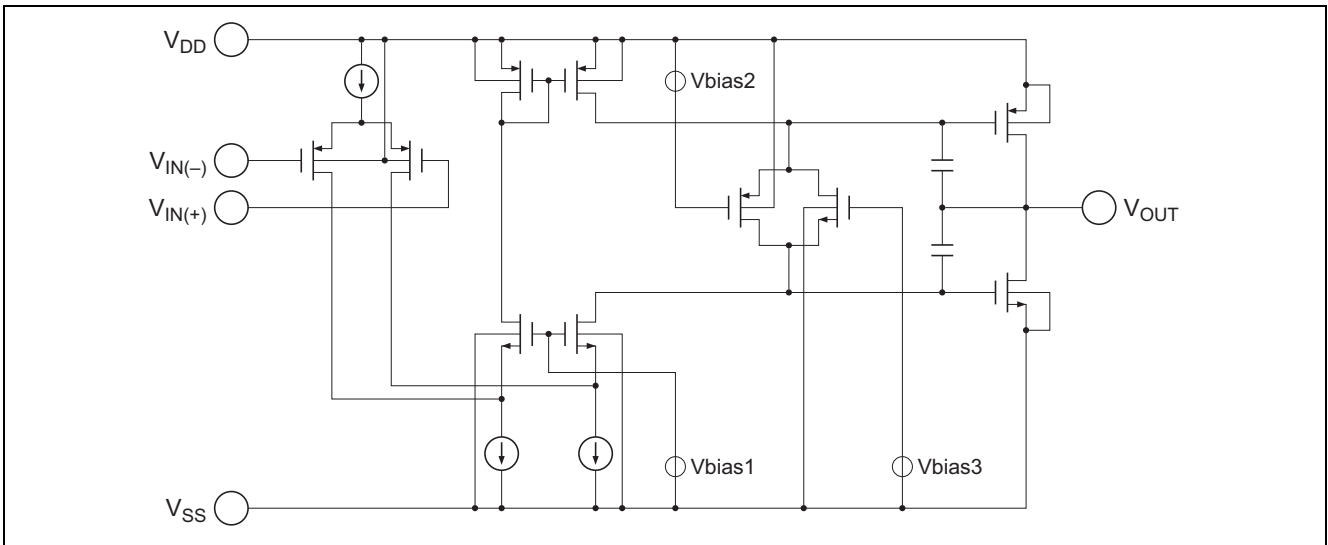
Ordering Information

| Part No. | Package Name | Package Code |
|-------------|--------------|--------------|
| HA1630D08MM | MMPAK-8 | PLSP0008JC-A |
| HA1630D08T | TSSOP-8 | PTSP0008JC-B |

Pin Arrangement



Equivalent Circuit (1/2)



Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Ratings | Unit | Note |
|----------------------------|-----------------------|--------------------------------------|------|------|
| Supply voltage | V _{DD} | 7.0 | V | |
| Differential input voltage | V _{IN(diff)} | -V _{DD} to +V _{DD} | V | 1 |
| Input voltage | V _{IN} | -0.1 to +V _{DD} | V | |
| Output current | I _{OUT} | 70 | mA | |
| Power dissipation | P _T | 145 (MMPAK-8) | mW | 2 |
| | | 192 (TSSOP-8) | | |
| Operating temperature | T _{opr} | -40 to +85 | °C | |
| Storage temperature | T _{stg} | -55 to +125 | °C | |

Note: 1. Do not apply input voltage exceeding V_{DD} or 7 V.

2. If Ta > 25°C,

MMPAK-8: derate by -1.45 mW/°C

TSSOP-8: derate by -1.92 mW/°C

Electrical Characteristics

DC Characteristics

(Ta = 25°C, V_{DD} = 3.0 V, V_{SS} = 0 V)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---------------------------------|----------------------|------|-----|------|------|--|
| Input offset voltage | V _{IO} | — | — | 6 | mV | V _{IN} = 1.5 V, R _L = 1 MΩ |
| Input bias current | I _{IB} | — | (1) | — | pA | V _{IN} = 1.5 V |
| Input offset current | I _{IO} | — | (1) | — | pA | V _{IN} = 1.5 V |
| Common mode input voltage range | V _{CM} | -0.1 | — | 1.8 | V | |
| Supply current | I _{DD} | — | 340 | 1000 | μA | V _{IN(+)} = 1.0 V, R _L = ∞ |
| Output source current | I _{OSOURCE} | 15 | 30 | — | mA | V _{out} = 2.5 V |
| Output sink current | I _{OSINK} | 15 | 30 | — | mA | V _{out} = 0.5 V |
| Open loop voltage gain | A _V | 55 | 80 | — | dB | R _L = 100 kΩ |
| Common mode rejection ratio | CMRR | 50 | 80 | — | dB | V _{IN1} = 0 V, V _{IN2} = 1.8 V |
| Power supply rejection ratio | PSRR | 55 | 80 | — | dB | V _{DD1} = 2.7 V, V _{DD2} = 5.5 V |
| Output high voltage | V _{OH} | 2.9 | — | — | V | R _L = 600 Ω to V _{SS} |
| Output low voltage | V _{OL} | — | — | 0.1 | V | R _L = 600 Ω to V _{DD} |

Note: () : Design specification

AC Characteristics

(Ta = 25°C, V_{DD} = 3.0 V, V_{SS} = 0 V)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|------------------------|-----------------|-----|-------|-----|------|---|
| Slew rate | SR _r | — | (1.5) | — | V/μs | V _{IN} = 1.5 V, C _L = 15 pF (V _{INL} = 0.2 V, V _{INH} = 1.7 V) |
| | SR _f | — | (1.5) | — | | |
| Gain bandwidth product | GBW | — | (2.0) | — | MHz | V _{IN} = 1.5 V, C _L = 15 pF |

Note: () : Design specification

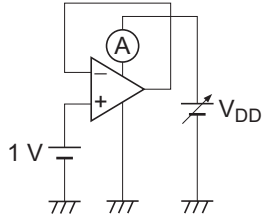
Table of Graphs

| Electrical Characteristics | | | Characteristic Curves | Test Circuit No. |
|---------------------------------|---------------|-------------------------|-----------------------|------------------|
| Supply current | I_{DD} | vs. Supply voltage | 1 | 1 |
| | | vs. Temperature | 2 | 1 |
| Output high voltage | V_{OH} | vs. Rload | 3 | 2 |
| Output low voltage | V_{OL} | vs. Rload | 4 | 3 |
| Output source current | $I_{OSOURCE}$ | vs. Output high voltage | 5 | 4 |
| | | vs. Temperature | 6 | 4 |
| Output sink current | I_{OSINK} | vs. Output low voltage | 7 | 5 |
| | | vs. Temperature | 8 | 5 |
| Input offset voltage | V_{IO} | vs. Supply voltage | 9 | 6 |
| | | vs. Input voltage | 10 | 6 |
| | | vs. Temperature | 11 | 7 |
| Common mode input voltage range | V_{CM} | vs. Supply voltage | 12 | 8 |
| | | vs. Temperature | 13 | 8 |
| Common mode rejection ratio | CMRR | vs. Input voltage | 14 | 9 |
| Power supply rejection ratio | PSRR | vs. Supply voltage | 15 | 10 |
| Input bias current | I_{IB} | vs. Input voltage | 16 | 11, 12 |
| | | vs. Temperature | 17 | 11, 12 |
| Slew rate (rising) | SRr | vs. Cload | 18 | 13 |
| | | vs. Temperature | 19 | 13 |
| | | Time waveform | 20 | 13 |
| Slew rate (falling) | SRf | vs. Cload | 21 | 13 |
| | | vs. Temperature | 22 | 13 |
| | | Time waveform | 23 | 13 |
| Open loop gain | A_V | vs. Rload | 24 | 14 |
| | | vs. Frequency | 25, 26 | 14 |
| Phase margin | PM | vs. Cload | 27 | 14 |
| Channel separation | CS | vs. Frequency | 28 | 15 |
| Noise input voltage | VNI | vs. Frequency | 29 | 16 |

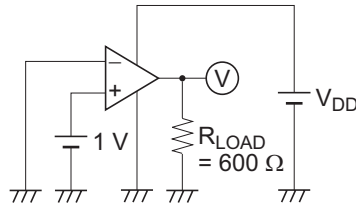
Test Circuits

(Unless otherwise noted, $V_{DD} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$)

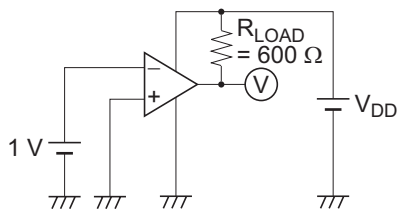
1. Supply Current, I_{DD}



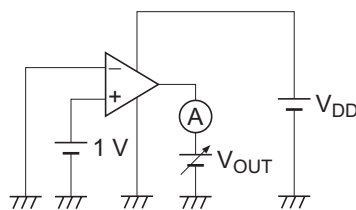
2. Output High Voltage, V_{OH} (Output High)



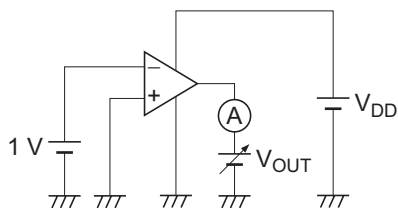
3. Output Low Voltage, V_{OL} (Output Low)



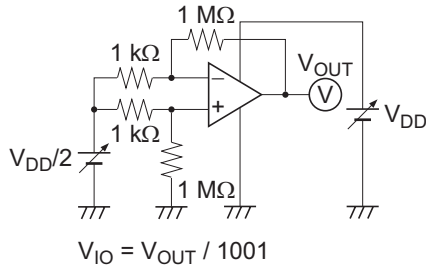
4. Output Source Current, $I_{OSOURCE}$



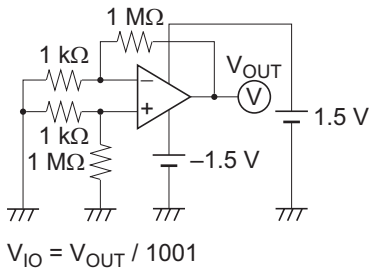
5. Output Sink Current, I_{OSINK}



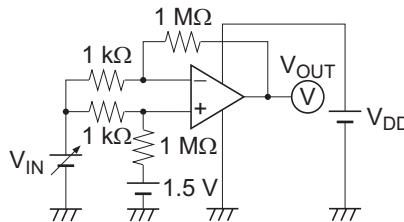
6. Input Offset Voltage vs. Operating Voltage



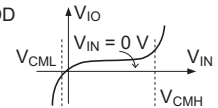
7. Input Offset Voltage, V_{IO}



8. Common Mode Input Voltage Range, V_{CM}



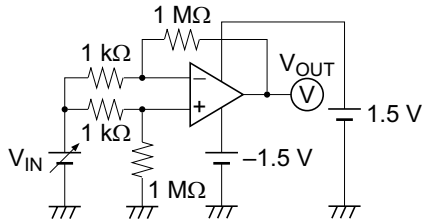
Note:
 V_{CML} and V_{CMH} are values of V_{IN} when V_{IO} changes more than 50 dB taking $V_{IN} = 0\text{ V}$ as reference.



Test Circuits (cont.)

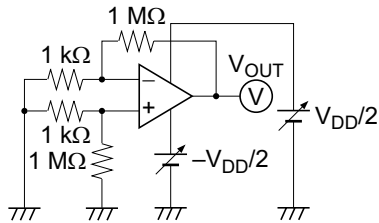
(Unless otherwise noted, $V_{DD} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$)

9. Common Mode Rejection Ratio, CMRR



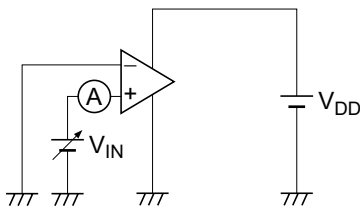
| V_{IN} | Measure Point | Calculate V_{IO} | CMRR Calculation |
|----------|---------------|-----------------------------|---|
| -1.5 V | V_{OUT1} | $V_{IO1} = V_{OUT1} / 1001$ | $\text{CMRR} = \left 20 \log_{10} \frac{ V_{IO2} - V_{IO1} }{0.3 - (-1.5\text{ V})} \right $ |
| 0.3 V | V_{OUT2} | $V_{IO2} = V_{OUT2} / 1001$ | |

10. Power Supply Rejection Ratio, PSRR

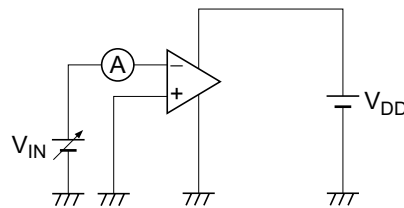


| V_{DD} | Measure Point | Calculate V_{IO} | CMRR Calculation |
|----------|---------------|-----------------------------|---|
| 2.7 V | V_{OUT1} | $V_{IO1} = V_{OUT1} / 1001$ | $\text{PSRR} = \left 20 \log_{10} \frac{ V_{IO2} - V_{IO1} }{5.5\text{ V} - 2.7\text{ V}} \right $ |
| 5.5 V | V_{OUT2} | $V_{IO2} = V_{OUT2} / 1001$ | |

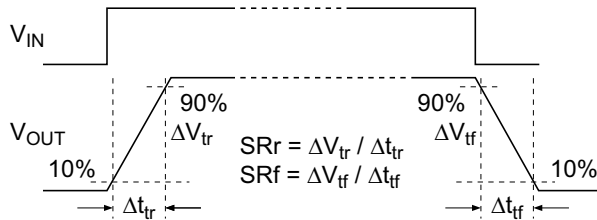
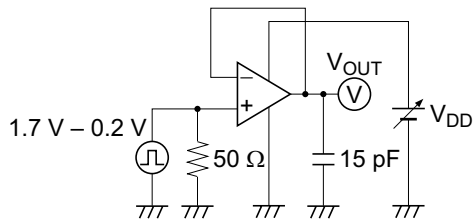
11. Input Bias Current, I_{B+}



12. Input Bias Current, I_{B-}



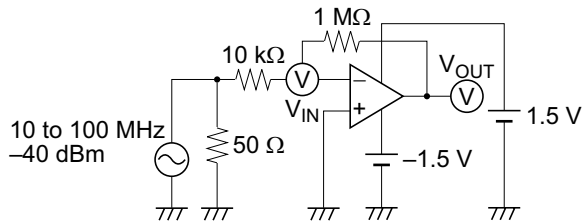
13. Slew Rate (Large Signal Input)



Test Circuits (cont.)

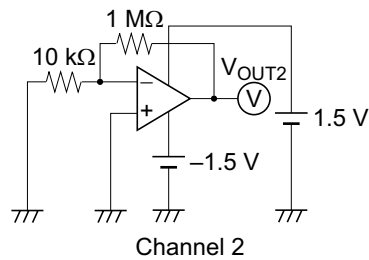
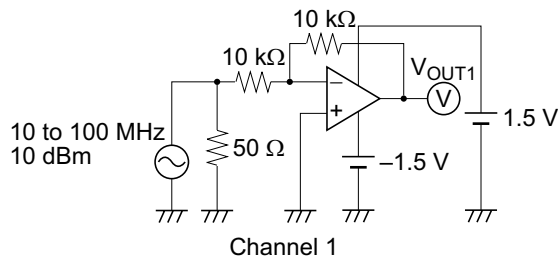
(Unless otherwise noted, $V_{DD} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$)

14. Open Loop Voltage Gain, A_V



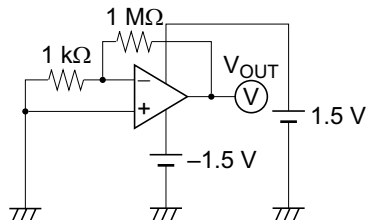
$$A_V = \left| 20 \log_{10} \frac{101 \times |V_{OUT}|}{|V_{IN}|} \right|$$

15. Channel Separation, CS



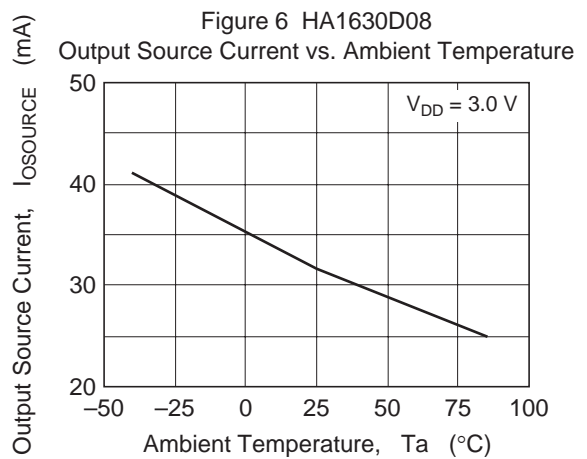
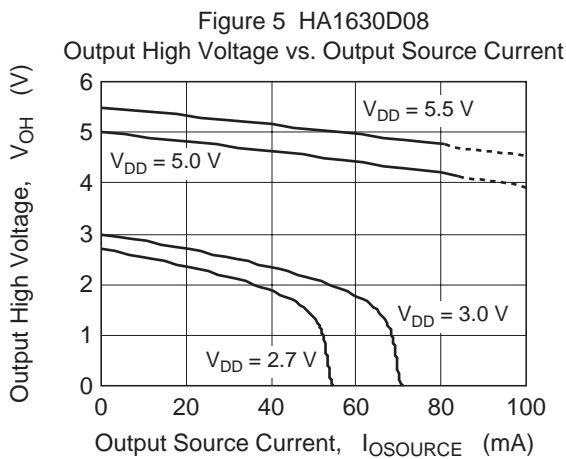
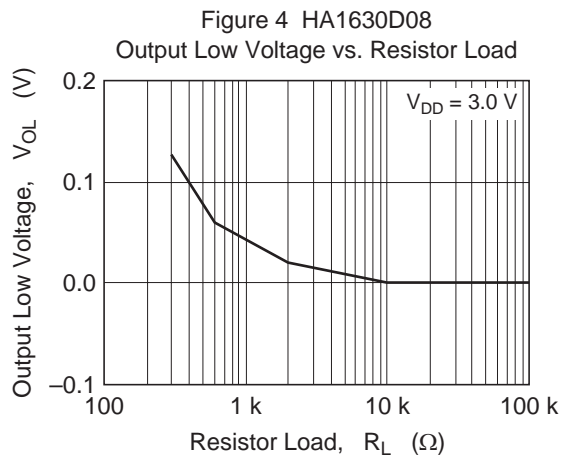
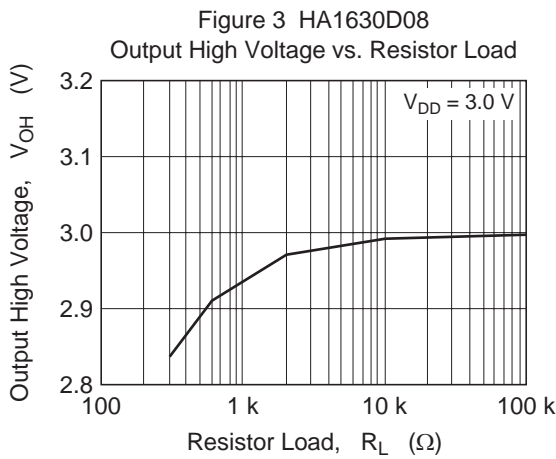
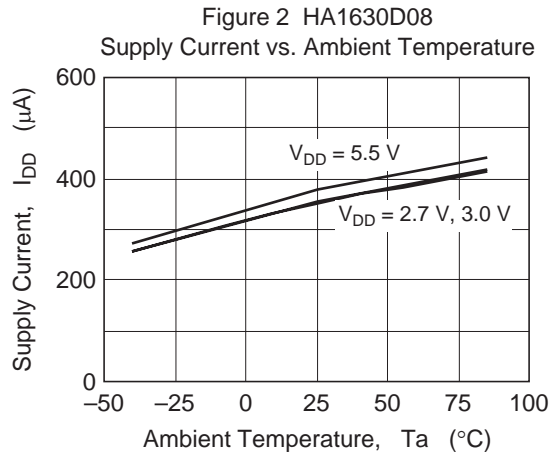
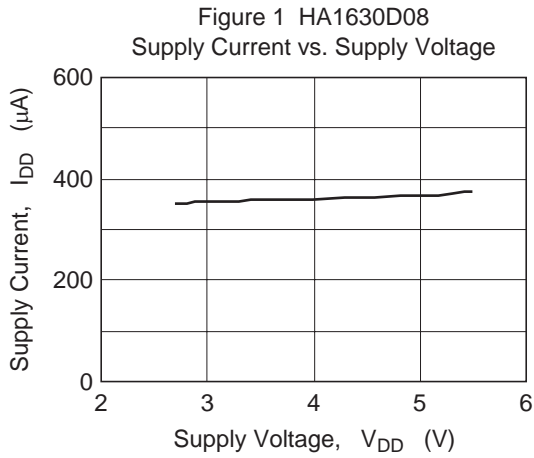
$$CS = \left| 20 \log_{10} \frac{101 \times |V_{OUT2}|}{|V_{OUT1}|} \right|$$

16. Noise Input Voltage, VNI

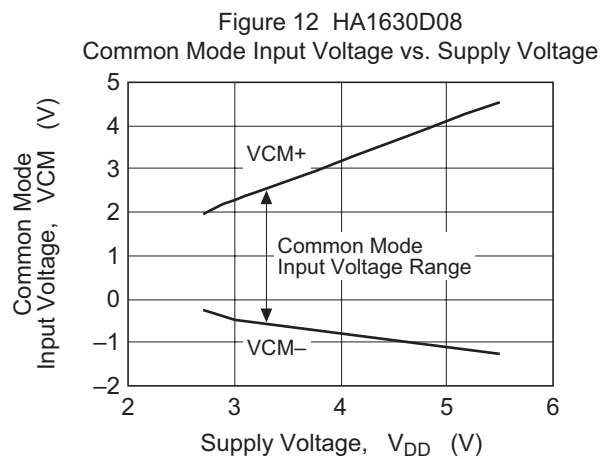
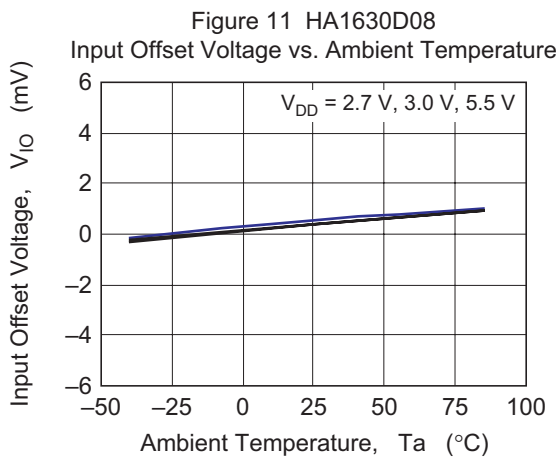
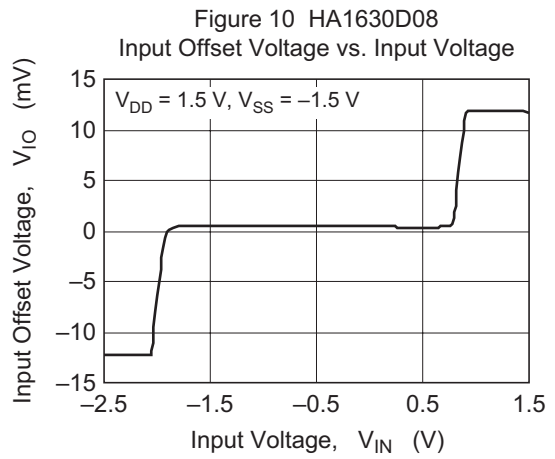
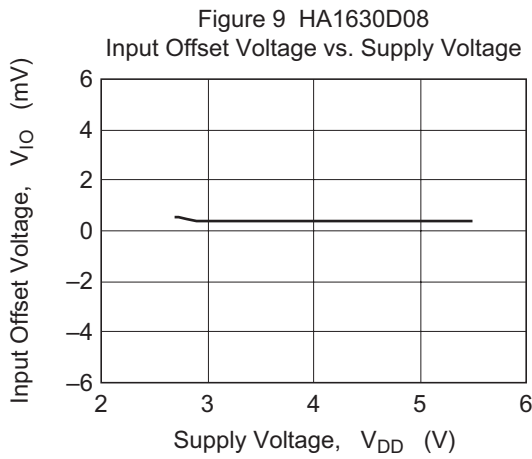
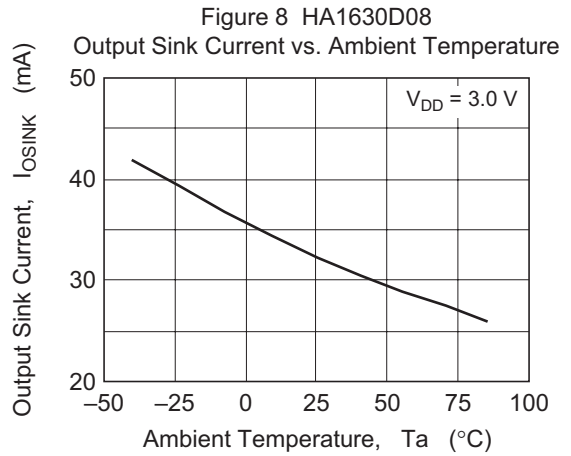
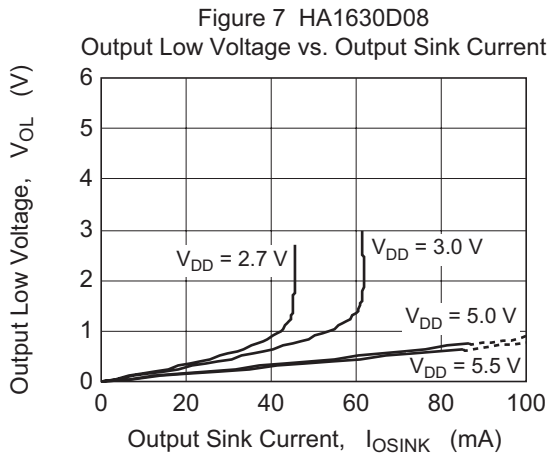


$$VNI = \frac{V_{OUT}}{1001}$$

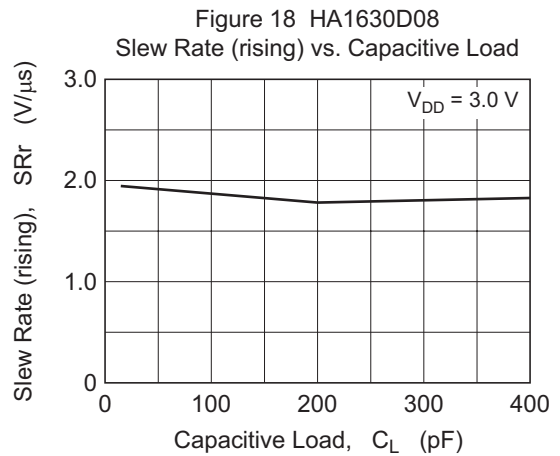
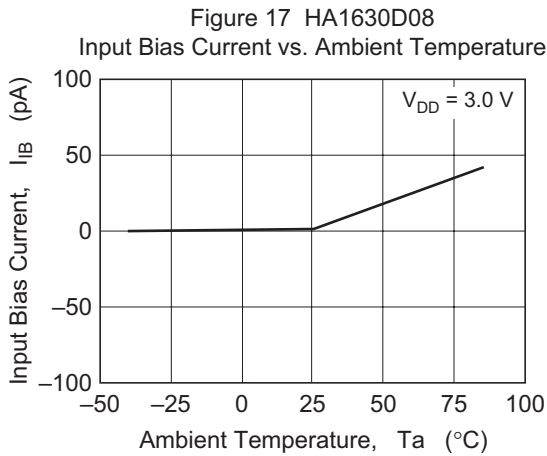
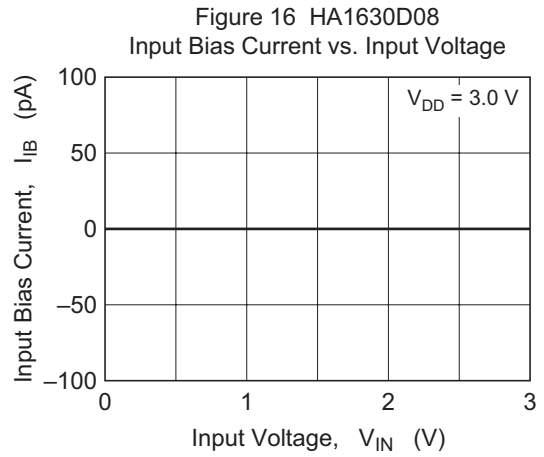
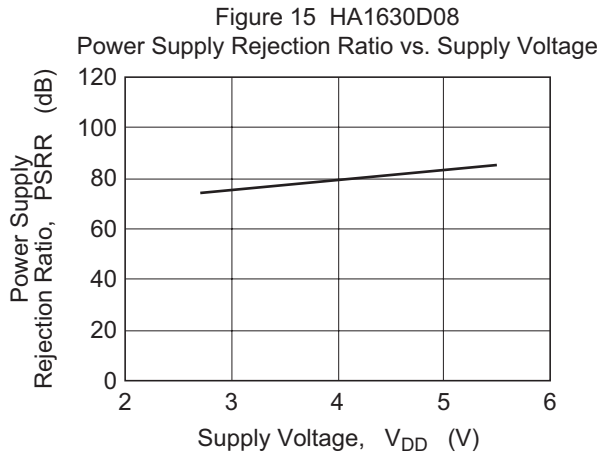
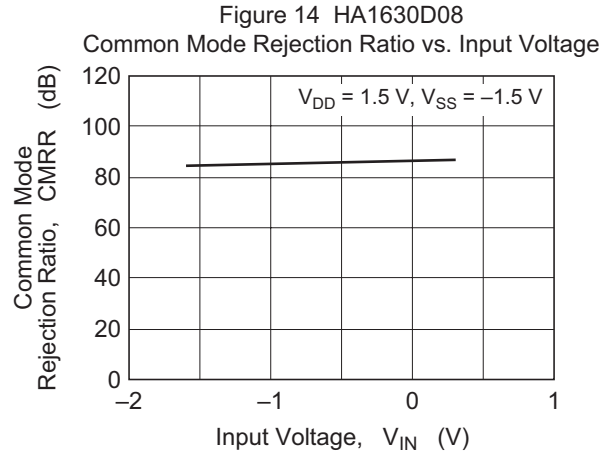
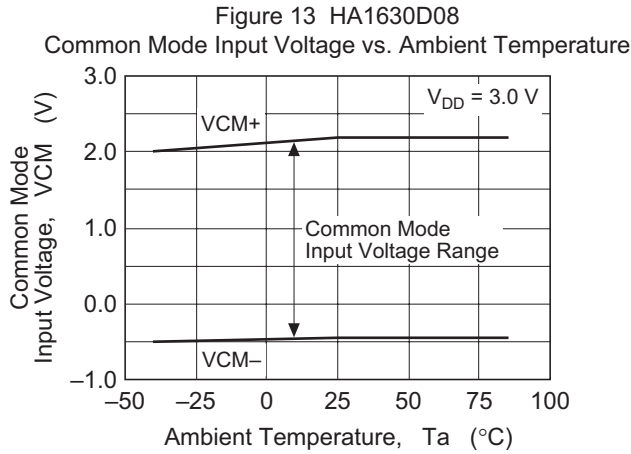
Characteristic Curves



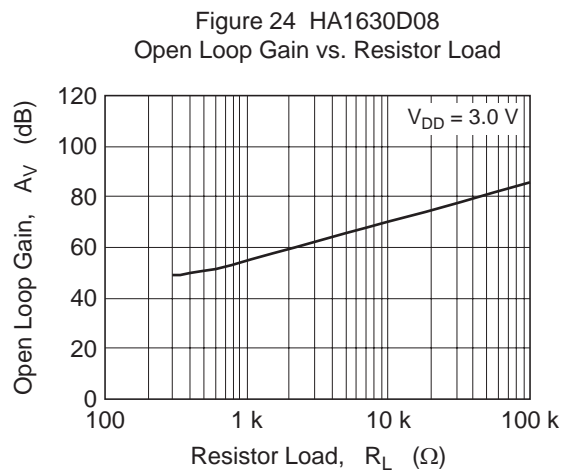
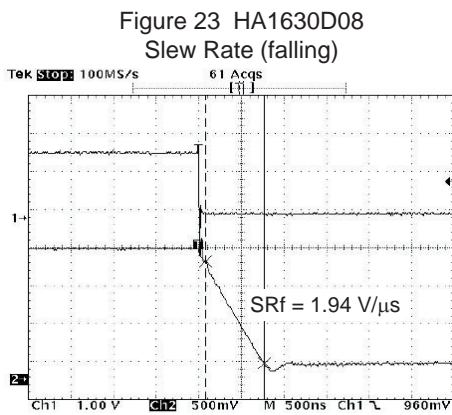
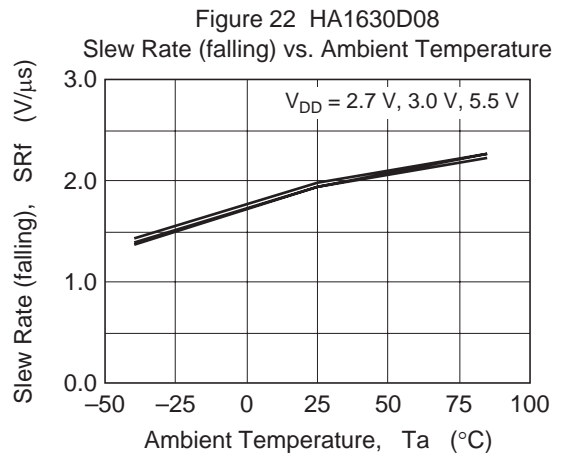
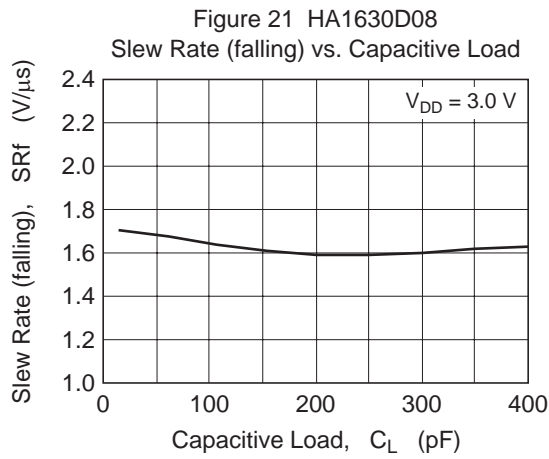
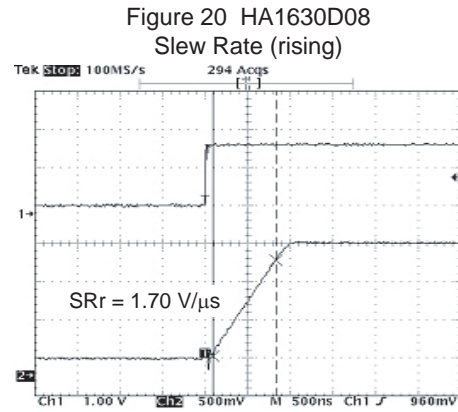
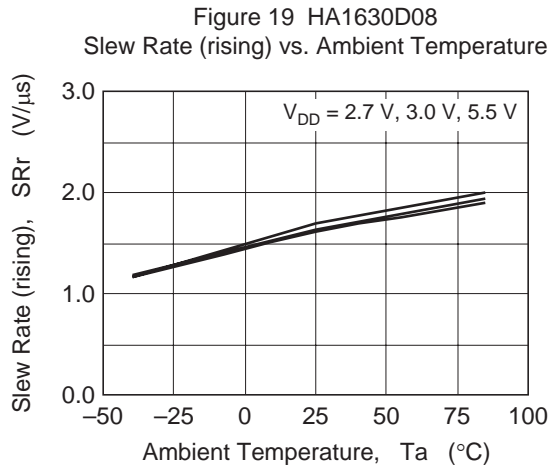
Characteristic Curves (cont.)



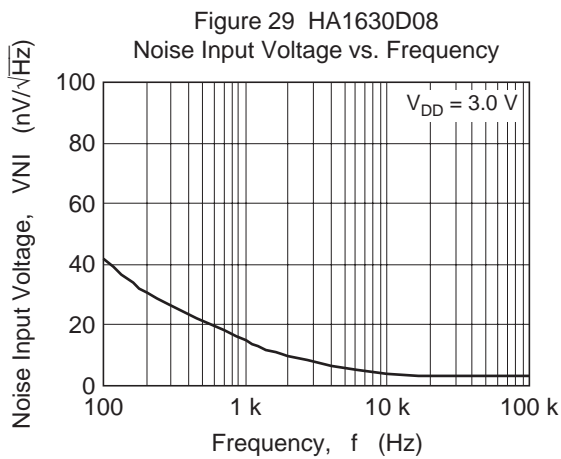
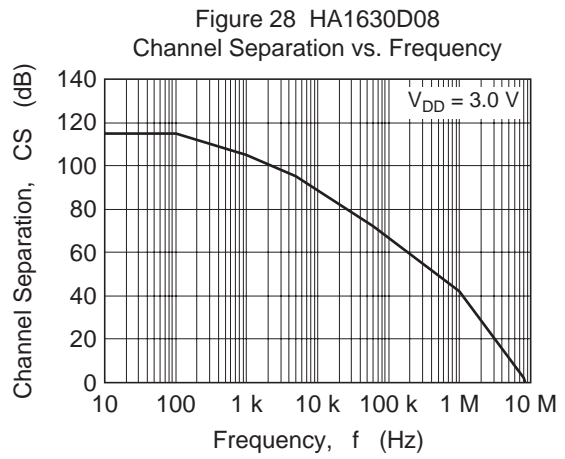
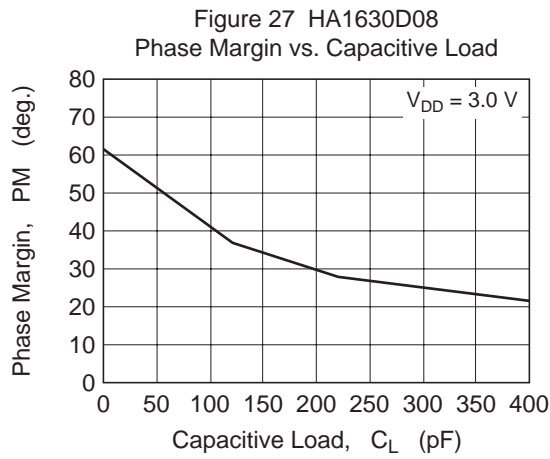
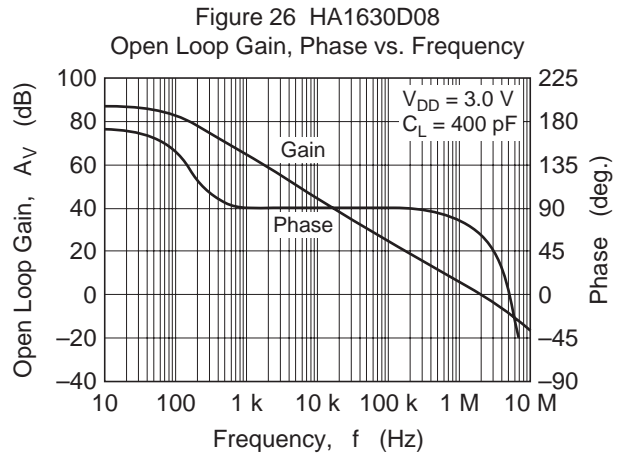
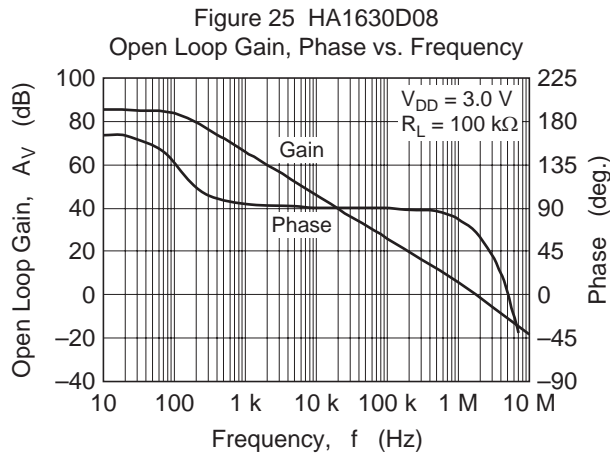
Characteristic Curves (cont.)



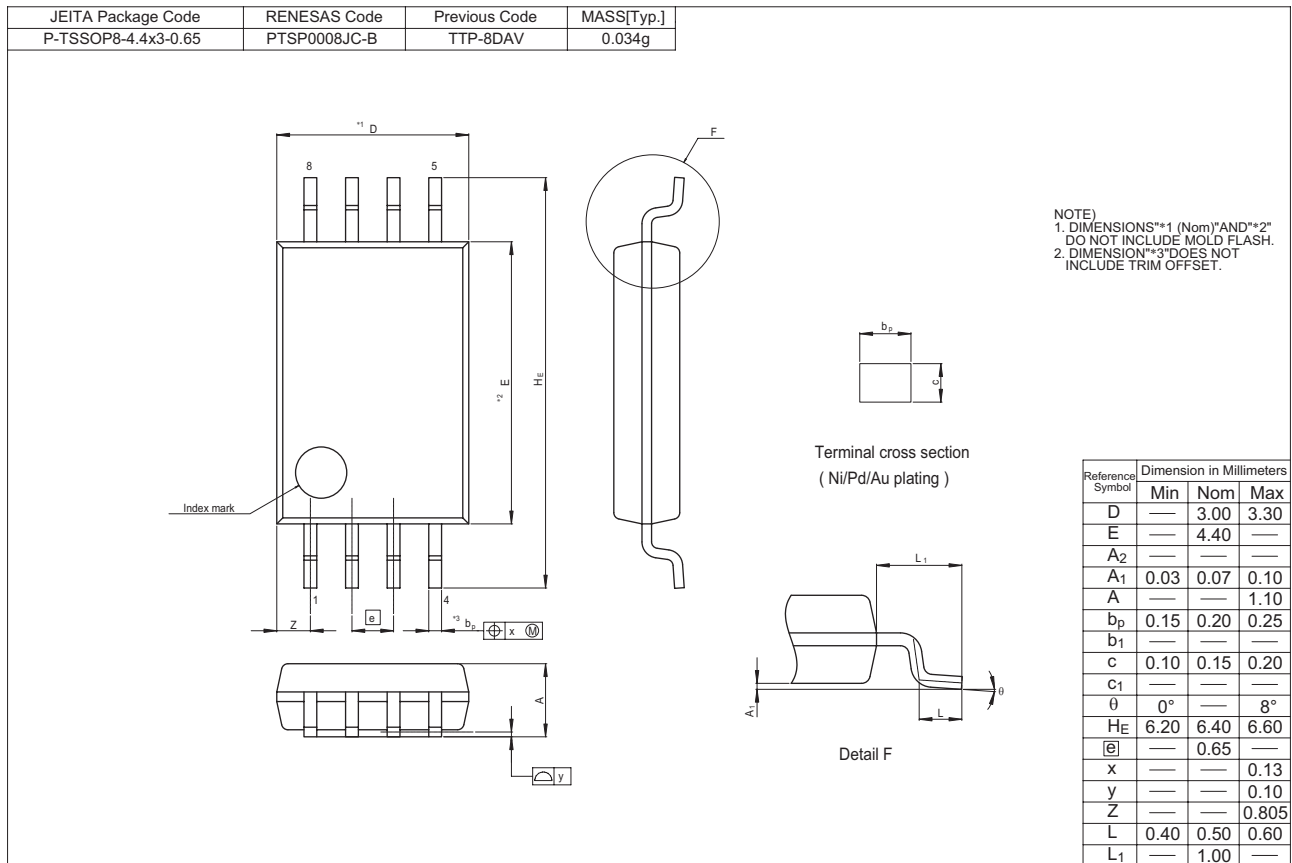
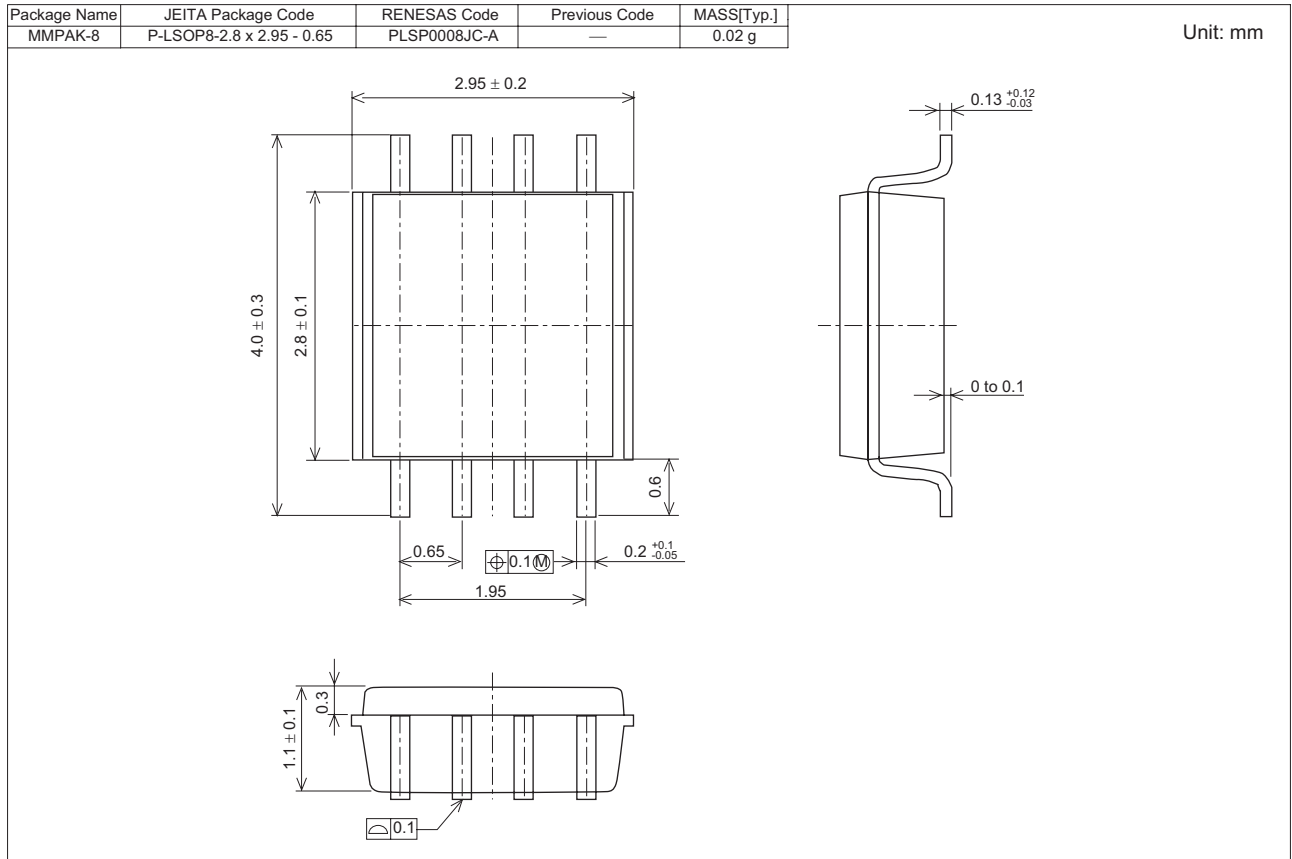
Characteristic Curves (cont.)



Characteristic Curves (cont.)



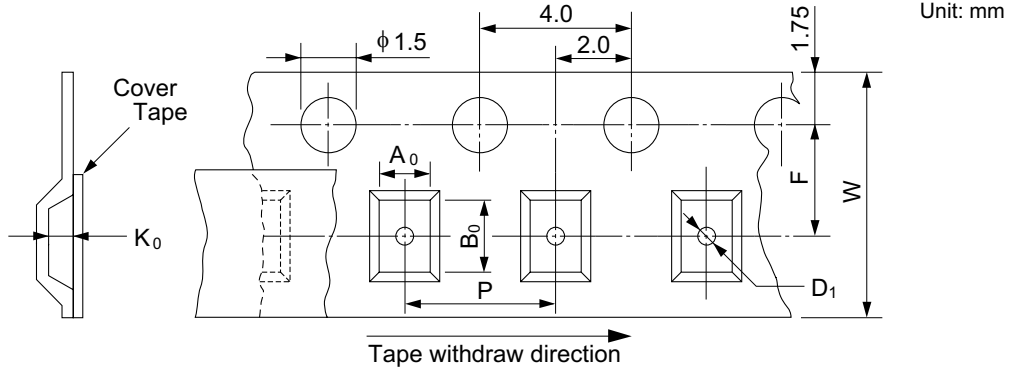
Package Dimensions



Taping & Reel Specification

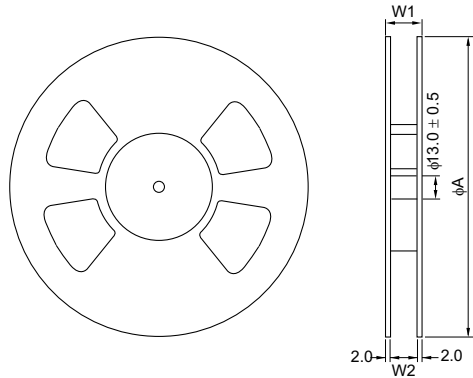
[Taping]

| Package Code | W | P | Ao | Bo | Ko | E | F | D1 | Maximum Storage No. |
|--------------|----|-----|------|------|-----|------|-----|------|---------------------|
| TSSOP-8 | 12 | 8 | 6.9 | 3.6 | 1.7 | 1.75 | 5.5 | 1.5 | 3,000 pcs/reel |
| MMPAK-8 | 12 | 4.0 | 3.15 | 4.35 | — | — | 5.5 | 1.05 | 3,000 pcs/reel |



[Reel]

| Package | Tape width | W1 | W2 | A |
|---------|------------|------|------|-----|
| TSSOP-8 | 12 | 17.4 | 13.4 | 330 |
| MMPAK-8 | 12 | 17.0 | 13.0 | 178 |

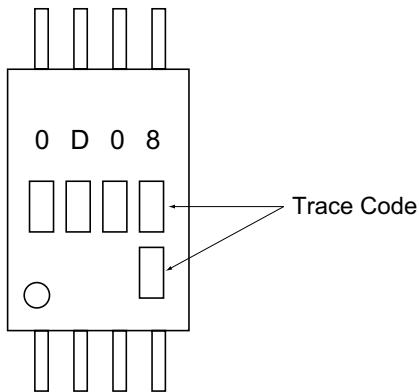


[Ordering Information]

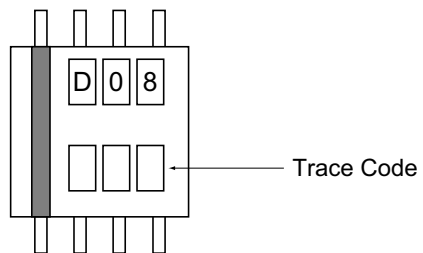
| |
|---------------|
| Ordering Unit |
| 3,000 pcs |

Mark Indication

• TSSOP-8



• MMPAK-8



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