

---

# R1LV0408D Series

4M SRAM (512-kword × 8-bit)

REJ03C0310-0100

Rev.1.00

May.24.2007

---

## Description

The R1LV0408D is a 4-Mbit static RAM organized 512-kword × 8-bit, fabricated by Renesas's high-performance 0.15μm CMOS and TFT technologies. R1LV0408D Series has realized higher density, higher performance and low power consumption. The R1LV0408D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 32-pin SOP, 32-pin TSOP II and 32-pin STSOP.

## Features

- Single 3 V supply: 2.7 V to 3.6 V
- Access time: 55/70 ns (max)
- Power dissipation:
  - Standby: 3 μW (typ)
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Directly TTL compatible.
  - All inputs and outputs
- Battery backup operation.

## R1LV0408D Series

---

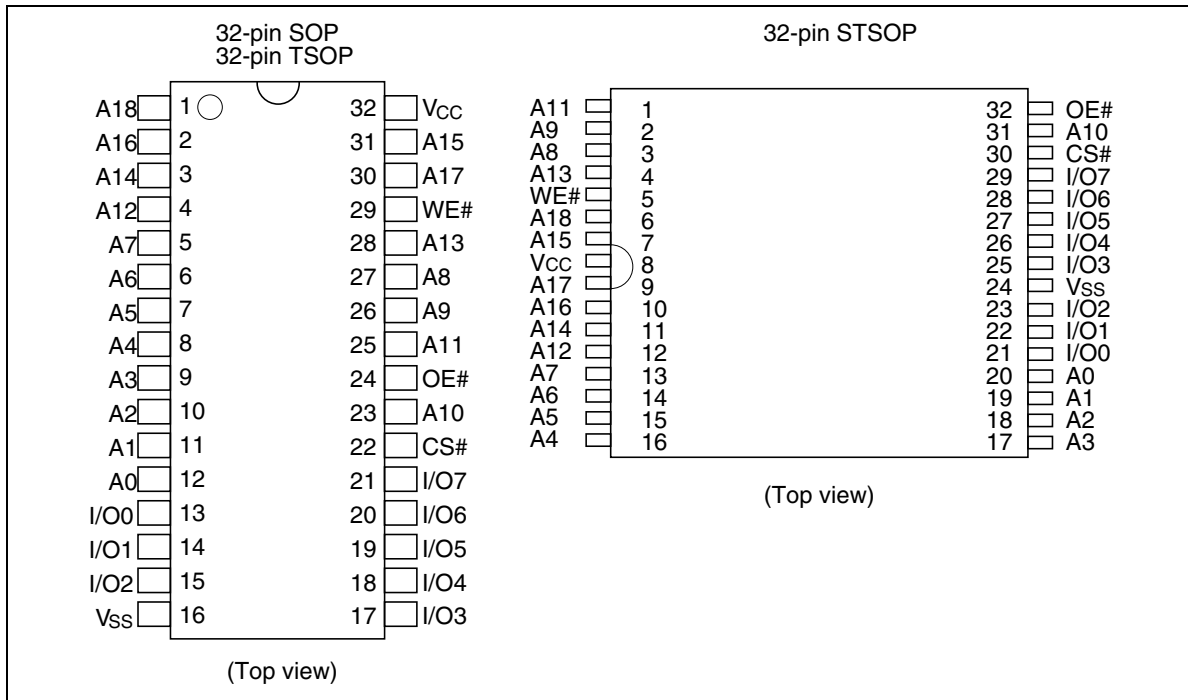
### Ordering Information

Type No.	Access time	Package
R1LV0408DSP-5S%	55 ns	525-mil 32-pin plastic SOP (32P2M-A)
R1LV0408DSP-7L%	70 ns	
R1LV0408DSB-5S%	55 ns	400-mil 32-pin plastic TSOP II (32P3Y-H)
R1LV0408DSB-7L%	70 ns	
R1LV0408DSA-5S%	55 ns	8mm × 13.4mm STSOP (32P3K-B)
R1LV0408DSA-7L%	70 ns	

?: Temperature version; see table below.

?	Temperature Range
R	0 to +70°C
I	-40 to +85°C

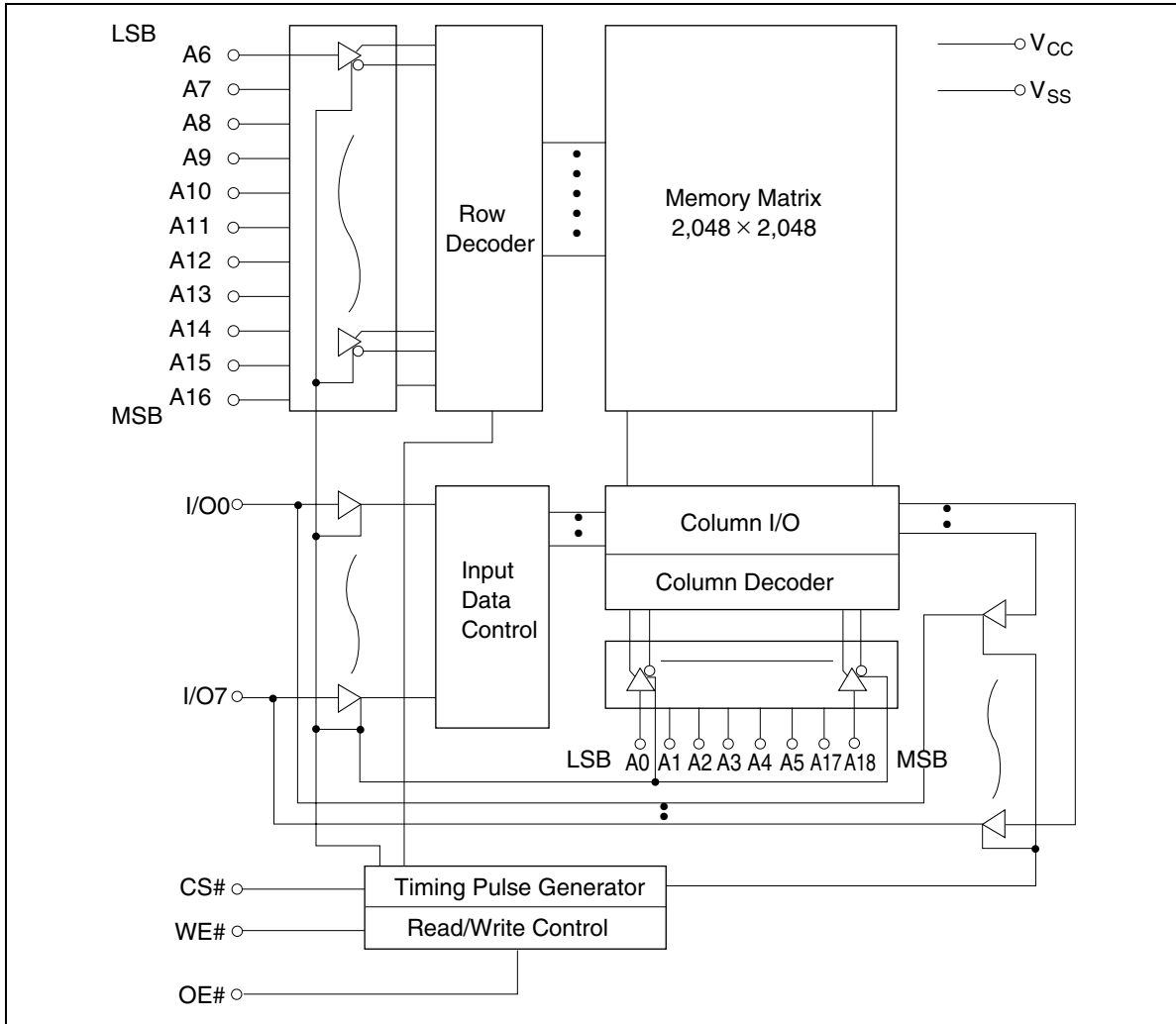
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS# ( $\overline{CS}$ )	Chip select
OE# ( $\overline{OE}$ )	Output enable
WE# ( $\overline{WE}$ )	Write enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

### Block Diagram



### Operation Table

WE#	CS#	OE#	Mode	V <sub>CC</sub> current	I/O0 to I/O7	Ref. cycle
×	H	×	Not selected	I <sub>SB</sub> , I <sub>SB1</sub>	High-Z	—
H	L	H	Output disable	I <sub>CC</sub>	High-Z	—
H	L	L	Read	I <sub>CC</sub>	Dout	Read cycle
L	L	H	Write	I <sub>CC</sub>	Din	Write cycle (1)
L	L	L	Write	I <sub>CC</sub>	Din	Write cycle (2)

Note: H: V<sub>IH</sub>, L: V<sub>IL</sub>, ×: V<sub>IH</sub> or V<sub>IL</sub>

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5 to +4.6	V
Terminal voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	-0.5* <sup>1</sup> to V <sub>CC</sub> + 0.5* <sup>2</sup>	V
Power dissipation	P <sub>T</sub>	0.7	W
Operating temperature	Topr	R ver.	0 to +70
		I ver.	-40 to +85
Storage temperature range	Tstg	-65 to +150	°C
Storage temperature range under bias	Tbias	R ver.	0 to +70
		I ver.	-40 to +85

Notes: 1. V<sub>T</sub> min: -3.0 V for pulse half-width ≤ 30 ns.  
2. Maximum voltage is +4.6 V.

### DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V
	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	-0.3* <sup>1</sup>	—	0.6	V
Ambient temperature range	R ver.	Ta	0	+70	°C
	I ver.		-40	+85	

Note: 1. V<sub>IL</sub> min: -3.0 V for pulse half-width ≤ 30 ns.

## DC Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Input leakage current		$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$	
Output leakage current		$ I_{LO} $	—	—	1	$\mu\text{A}$	CS# = $V_{IH}$ or OE# = $V_{IH}$ or WE# = $V_{IL}$ or $V_{IO} = V_{SS}$ to $V_{CC}$	
Operating current		$I_{CC}$	—	—	10	mA	CS# = $V_{IL}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA	
Average operating current		$I_{CC1}$	—	—	25	mA	Min. cycle, duty = 100%, CS# = $V_{IL}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA	
		$I_{CC2}$	—	—	5	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100%, $I_{IO} = 0$ mA, CS# $\leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V	
Standby current		$I_{SB}$	—	0.1*1	0.3	mA	CS# = $V_{IH}$	
Standby current	-5S%	to +85°C	$I_{SB1}$	—	—	10	$\mu\text{A}$	Average values $V_{in} \geq 0$ V, CS# $\geq V_{CC} - 0.2$ V
		to +70°C	$I_{SB1}$	—	—	8	$\mu\text{A}$	
		to +40°C	$I_{SB1}$	—	—	3	$\mu\text{A}$	
		to +25°C	$I_{SB1}$	—	1*1	2.5	$\mu\text{A}$	
	-7L%	to +85°C	$I_{SB1}$	—	—	20	$\mu\text{A}$	
		to +70°C	$I_{SB1}$	—	—	16	$\mu\text{A}$	
		to +40°C	$I_{SB1}$	—	—	10	$\mu\text{A}$	
		to +25°C	$I_{SB1}$	—	1*1	10	$\mu\text{A}$	
Output low voltage		$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1$ mA	
		$V_{OL2}$	—	—	0.2	V	$I_{OL} = 100$ $\mu\text{A}$	
Output high voltage		$V_{OH}$	2.4	—	—	V	$I_{OH} = -1.0$ mA	
		$V_{OH2}$	$V_{CC} - 0.2$	—	—	—	V	$I_{OH} = -0.1$ mA

Note: 1. Typical values are at  $V_{CC} = 3.0$  V,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.

## Capacitance

( $T_a = +25^\circ\text{C}$ ,  $f = 1.0$  MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	—	8	pF	$V_{in} = 0$ V	1
Input/output capacitance	$C_{IO}$	—	—	10	pF	$V_{IO} = 0$ V	1

Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$  /  $-40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7$  V to  $3.6$  V)

### Test Conditions

- Input pulse levels:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.4$  V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate +  $C_L$  (50 pF) (R1LV0408D-5S%)  
 1 TTL Gate +  $C_L$  (100 pF) (R1LV0408D-7L%)  
 (Including scope and jig)

Note: Temperature range depends on R/I-version. Please see table on page 2.

### Read Cycle

Parameter	Symbol	R1LV0408D				Unit	Notes
		-5S%		-7L%			
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	55	—	70	—	ns	
Address access time	$t_{AA}$	—	55	—	70	ns	
Chip select access time	$t_{CO}$	—	55	—	70	ns	
Output enable to output valid	$t_{OE}$	—	30	—	35	ns	
Chip select to output in low-Z	$t_{LZ}$	10	—	10	—	ns	2
Output enable to output in low-Z	$t_{OLZ}$	5	—	5	—	ns	2
Chip deselect to output in high-Z	$t_{HZ}$	0	20	0	25	ns	1, 2
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	ns	1, 2
Output hold from address change	$t_{OH}$	10	—	10	—	ns	

**Write Cycle**

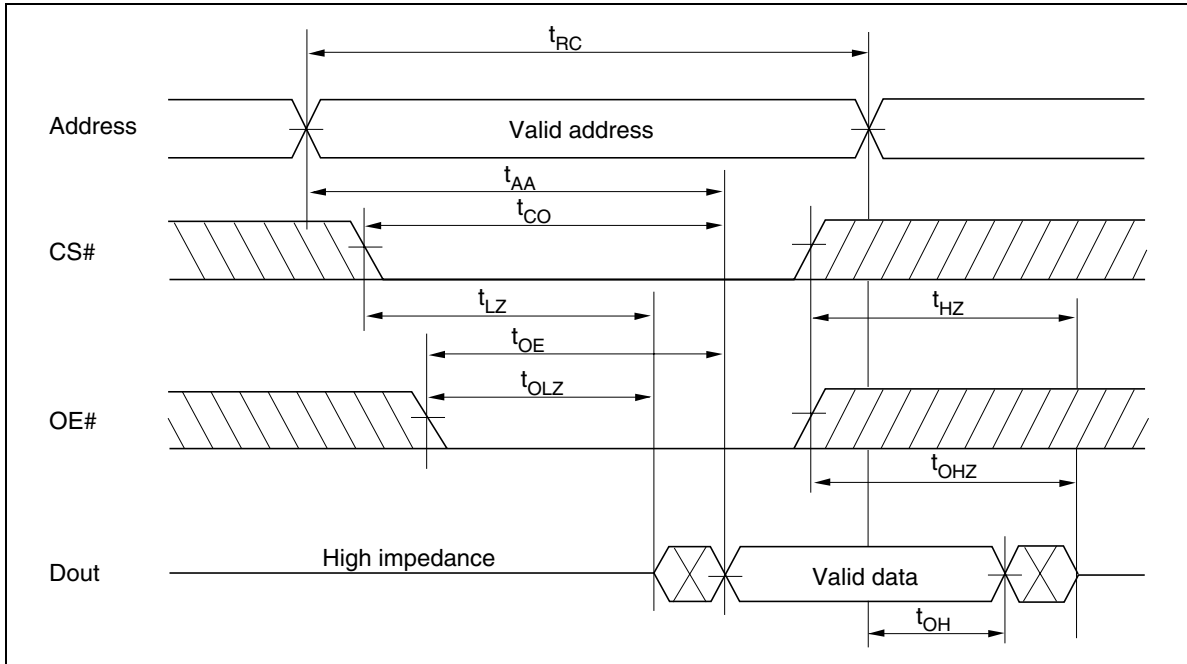
Parameter	Symbol	R1LV0408D				Unit	Notes
		-5S%		-7L%			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	55	—	70	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	60	—	ns	4
Address setup time	$t_{AS}$	0	—	0	—	ns	5
Address valid to end of write	$t_{AW}$	50	—	60	—	ns	
Write pulse width	$t_{WP}$	40	—	50	—	ns	3, 12
Write recovery time	$t_{WR}$	0	—	0	—	ns	6
Write to output in high-Z	$t_{WHZ}$	0	20	0	25	ns	1, 2, 7
Data to write time overlap	$t_{DW}$	25	—	30	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	ns	1, 2, 7

- Notes:
- $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  - This parameter is sampled and not 100% tested.
  - A write occurs during the overlap ( $t_{WP}$ ) of a low CS# and a low WE#. A write begins at the later transition of CS# going low or WE# going low. A write ends at the earlier transition of CS# going high or WE# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  - $t_{CW}$  is measured from CS# going low to the end of write.
  - $t_{AS}$  is measured from the address valid to the beginning of write.
  - $t_{WR}$  is measured from the earlier of WE# or CS# going high to the end of write cycle.
  - During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
  - If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
  - Dout is the same phase of the write data of this write cycle.
  - Dout is the read data of next address.
  - If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
  - In the write cycle with OE# low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

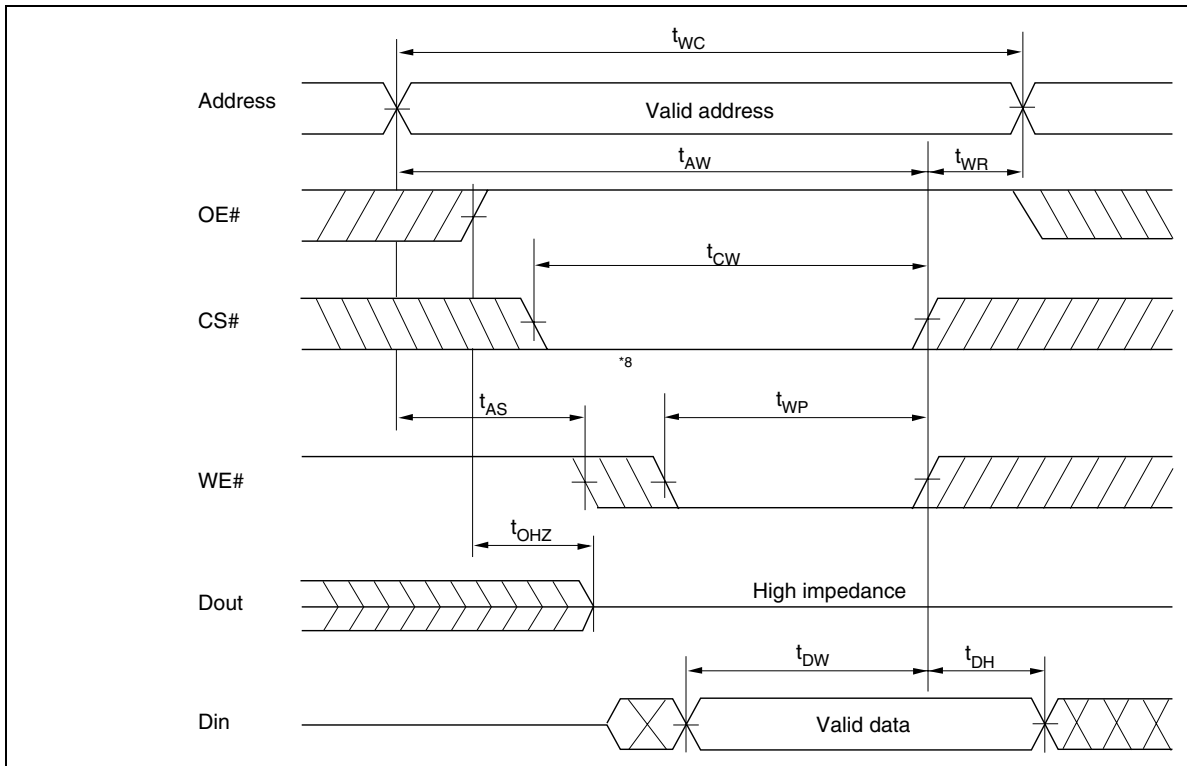


## Timing Waveform

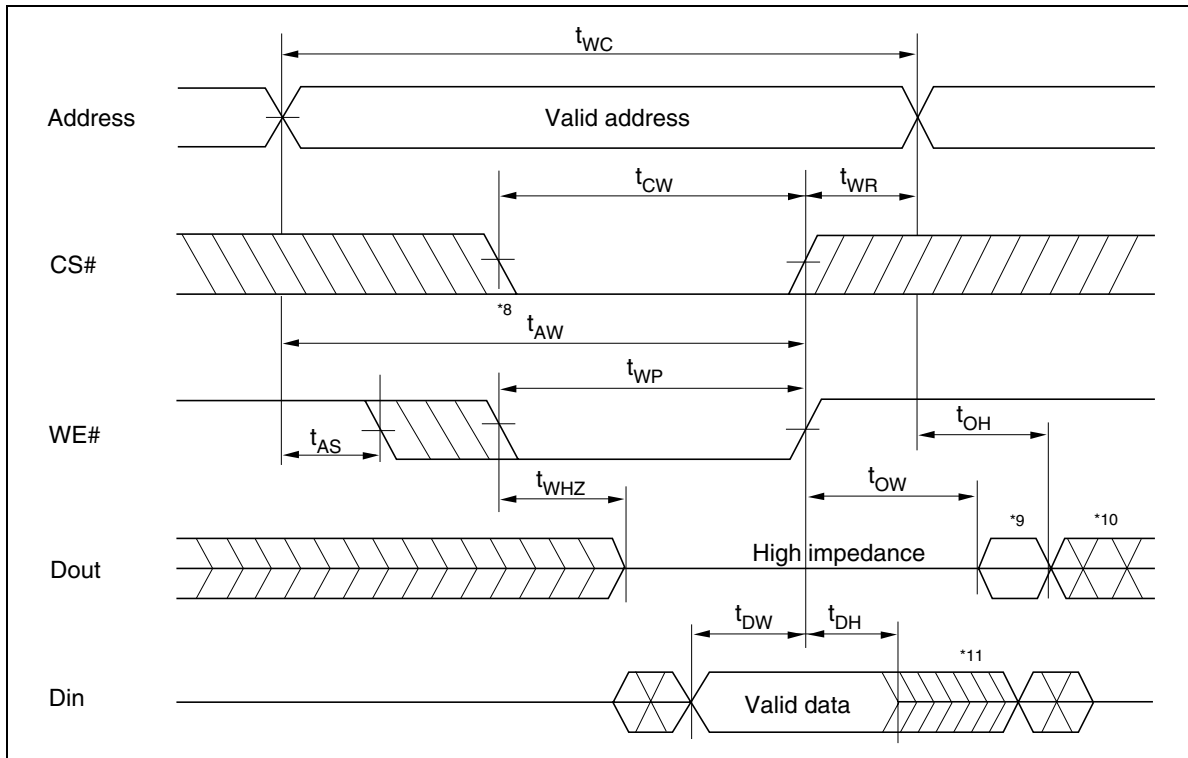
### Read Timing Waveform (WE# = V<sub>ih</sub>)



Write Timing Waveform (1) (OE# Clock)



Write Timing Waveform (2) (OE# Low Fixed)



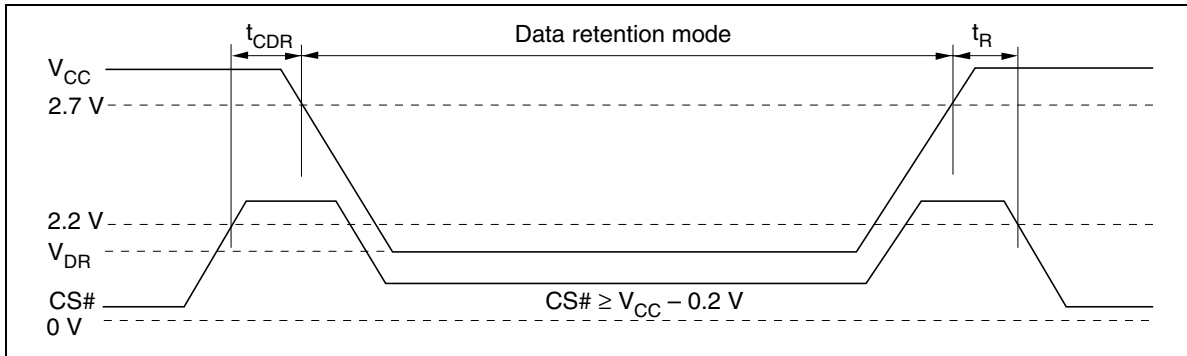
### Low V<sub>CC</sub> Data Retention Characteristics

(T<sub>a</sub> = 0 to +70°C / -40 to +85°C)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
V <sub>CC</sub> for data retention		V <sub>DR</sub>	2	—	—	V	CS# ≥ V <sub>CC</sub> - 0.2 V, Vin ≥ 0 V	
Data retention current	-5S%	to +85°C	I <sub>CCDR</sub>	—	—	10	μA	V <sub>CC</sub> = 3.0 V, Vin ≥ 0 V CS# ≥ V <sub>CC</sub> - 0.2 V Average values
		to +70°C	I <sub>CCDR</sub>	—	—	8	μA	
		to +40°C	I <sub>CCDR</sub>	—	—	3	μA	
		to +25°C	I <sub>CCDR</sub>	—	1*1	2.5	μA	
	-7L%	to +85°C	I <sub>CCDR</sub>	—	—	20	μA	
		to +70°C	I <sub>CCDR</sub>	—	—	16	μA	
		to +40°C	I <sub>CCDR</sub>	—	—	10	μA	
		to +25°C	I <sub>CCDR</sub>	—	1*1	10	μA	
Chip deselect to data retention time		t <sub>CDR</sub>	0	—	—	ns	See retention waveform	
Operation recovery time		t <sub>R</sub>	5	—	—	ms		

Note: 1. Typical values are at V<sub>CC</sub> = 3.0 V, T<sub>a</sub> = +25°C and specified loading, and not guaranteed.

### Low V<sub>CC</sub> Data Retention Timing Waveform (CS# Controlled)



**Revision History****R1LV0408D Series Data Sheet**

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Dec. 25, 2006	—	Initial issue
1.00	May. 24, 2007	6	DC Characteristics $I_{SB1}$ (-5S%) (to +25°C) max: 3 $\mu$ A to 2.5 $\mu$ A
		12	Low $V_{CC}$ Data Retention Characteristics $I_{CCDR}$ (-5S%) (to +25°C) max: 3 $\mu$ A to 2.5 $\mu$ A Deletion of note 2

Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
  - (1) artificial life support devices or systems
  - (2) surgical implantations
  - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
  - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



**RENESAS SALES OFFICES**

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

**Renesas Technology America, Inc.**  
450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

**Renesas Technology Hong Kong Ltd.**  
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2730-6071

**Renesas Technology Taiwan Co., Ltd.**  
10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology Singapore Pte. Ltd.**  
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**  
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510