

HAT2175H

Silicon N Channel Power MOS FET Power Switching

REJ03G0006-0400

Rev.4.00

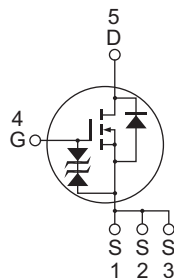
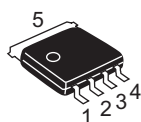
Sep 20, 2005

Features

- Capable of 8 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 33 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline

RENESAS Package code: PTZZ0005DA-A)
(Package name: LFPAK)



1, 2, 3 Source
4 Gate
5 Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	60	A
Body-drain diode reverse drain current	I_{DR}	15	A
Avalanche current	I_{AP} ^{Note 2}	15	A
Avalanche energy	E_{AR} ^{Note 2}	22.5	mJ
Channel dissipation	P_{ch} ^{Note 3}	15	W
Channel to Case Thermal Resistance	θ_{ch-C}	8.34	$^\circ\text{C}/\text{W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$

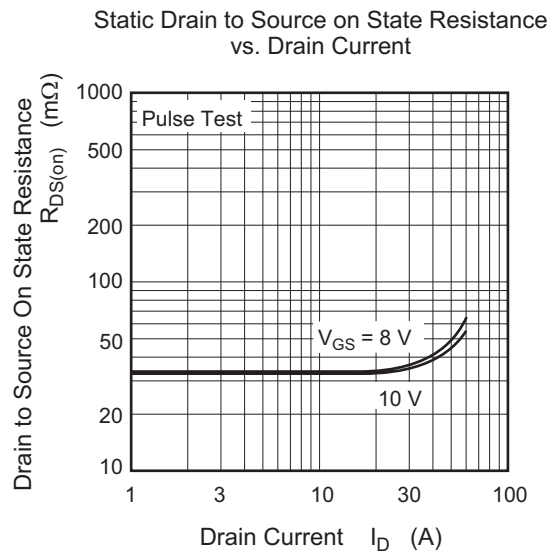
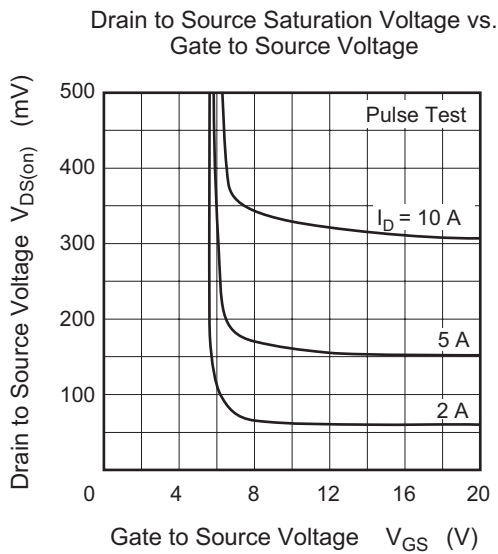
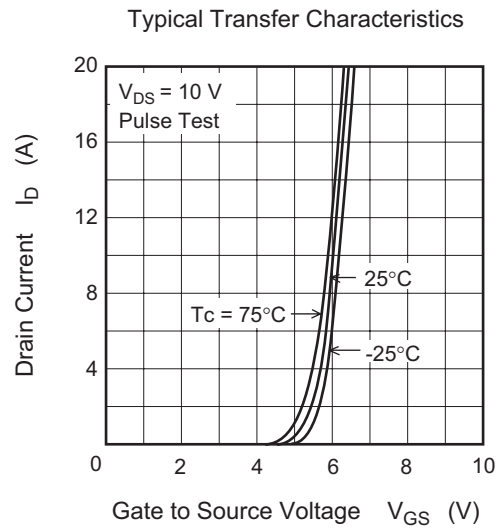
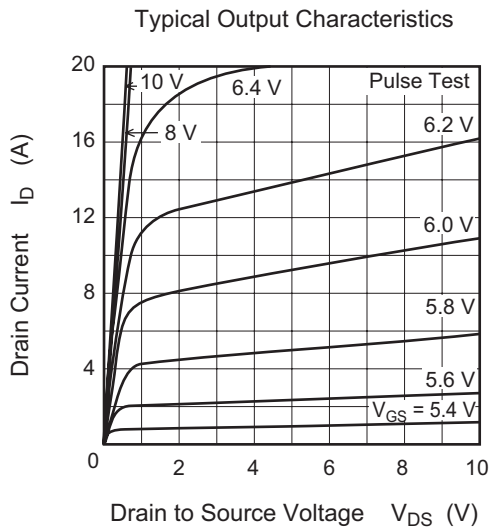
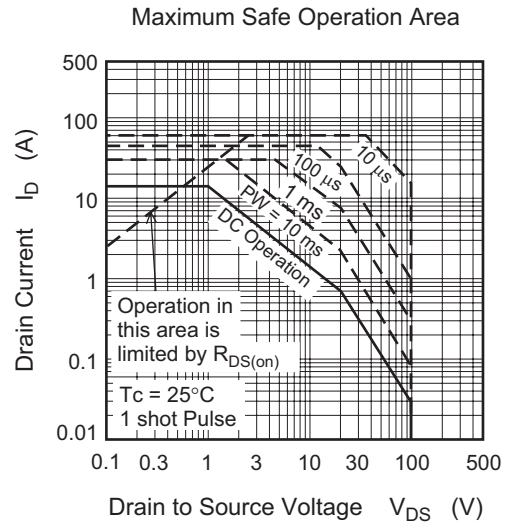
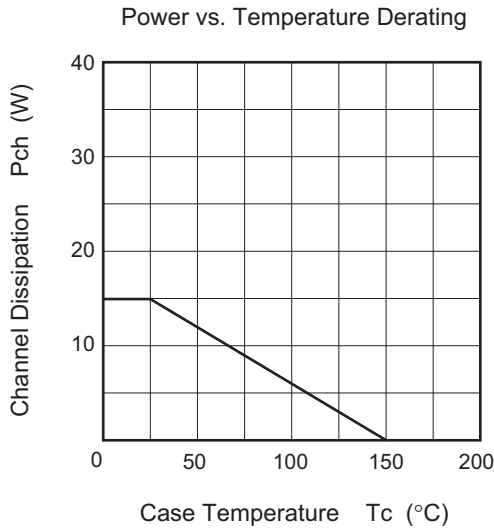
Electrical Characteristics

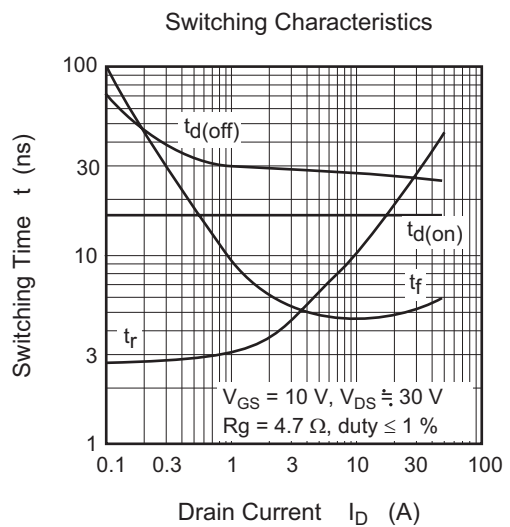
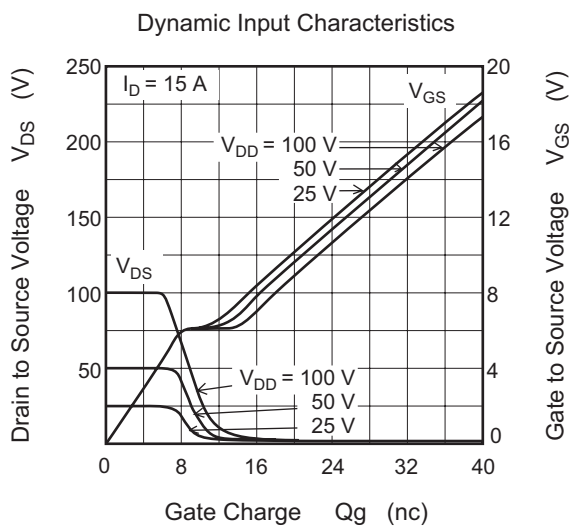
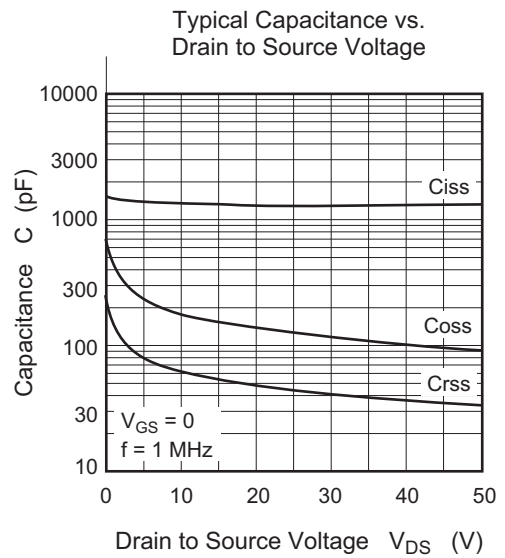
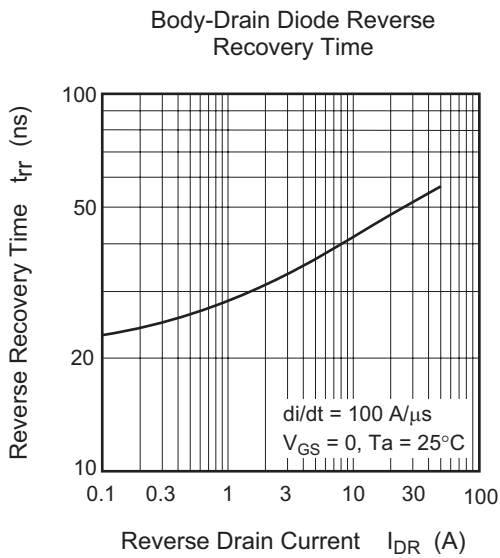
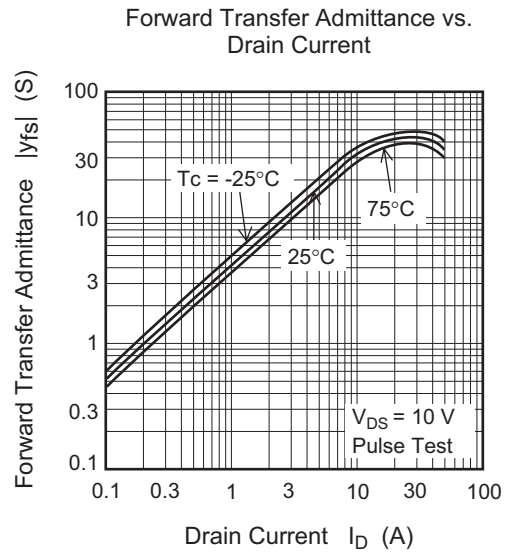
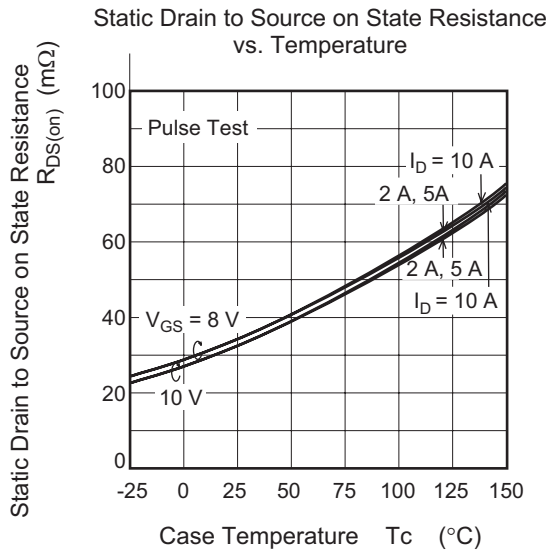
(Ta = 25°C)

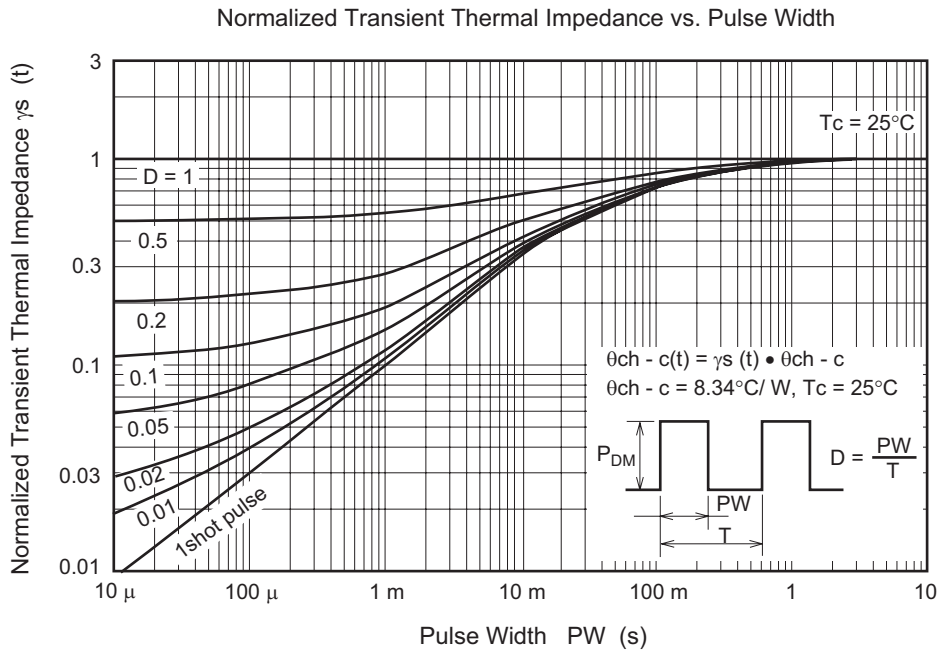
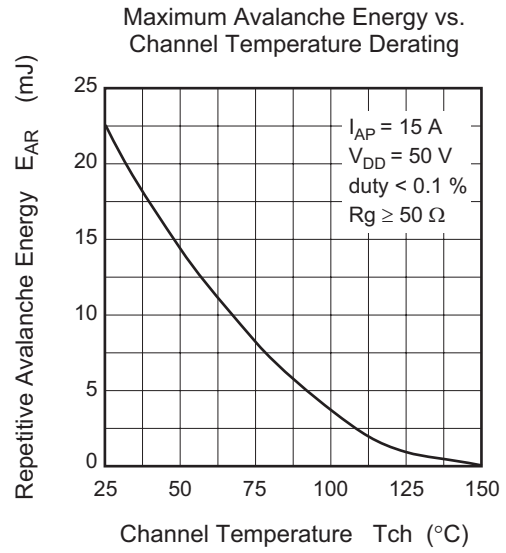
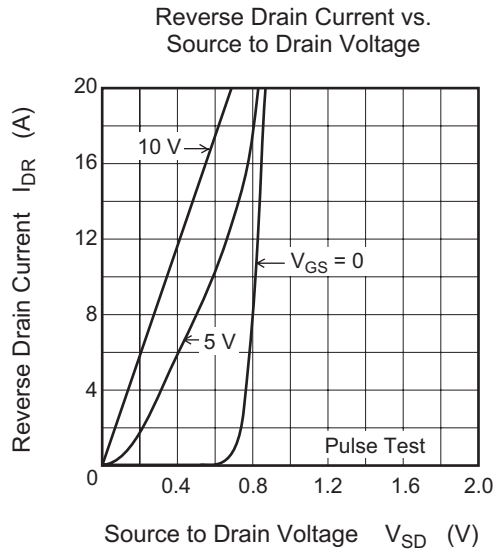
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 100 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	4.0	—	6.0	V	$V_{DS} = 10 \text{ V}, I_D = 20 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	33	42	$\text{m}\Omega$	$I_D = 7.5 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	34	46	$\text{m}\Omega$	$I_D = 7.5 \text{ A}, V_{GS} = 8 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	15	25	—	S	$I_D = 7.5 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1445	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	185	—	pF	
Reverse transfer capacitance	C_{rss}	—	61	—	pF	
Gate Resistance	R_g	—	0.55	—	Ω	
Total gate charge	Q_g	—	21	—	nC	$V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V},$ $I_D = 15 \text{ A}$
Gate to source charge	Q_{gs}	—	8	—	nC	
Gate to drain charge	Q_{gd}	—	4.5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	$V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A},$ $V_{DD} \cong 30 \text{ V}, R_L = 4 \Omega,$ $R_g = 4.7 \Omega$
Rise time	t_r	—	8.2	—	ns	
Turn-off delay time	$t_{d(off)}$	—	28	—	ns	
Fall time	t_f	—	4.7	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.84	1.10	V	$I_F = 15 \text{ A}, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	45	—	ns	$I_F = 15 \text{ A}, V_{GS} = 0,$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

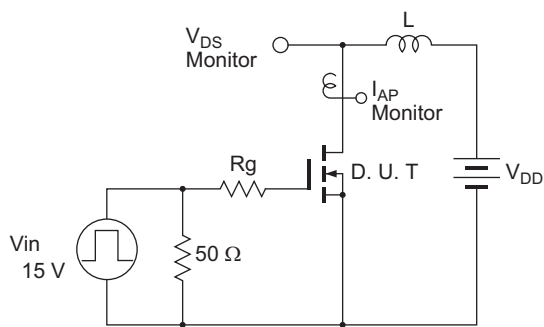
Main Characteristics





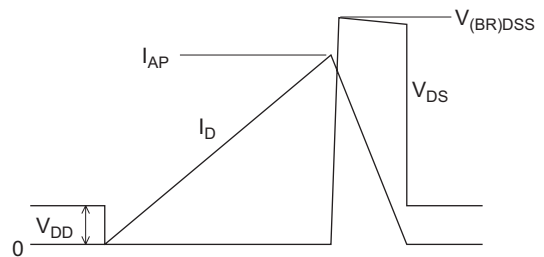


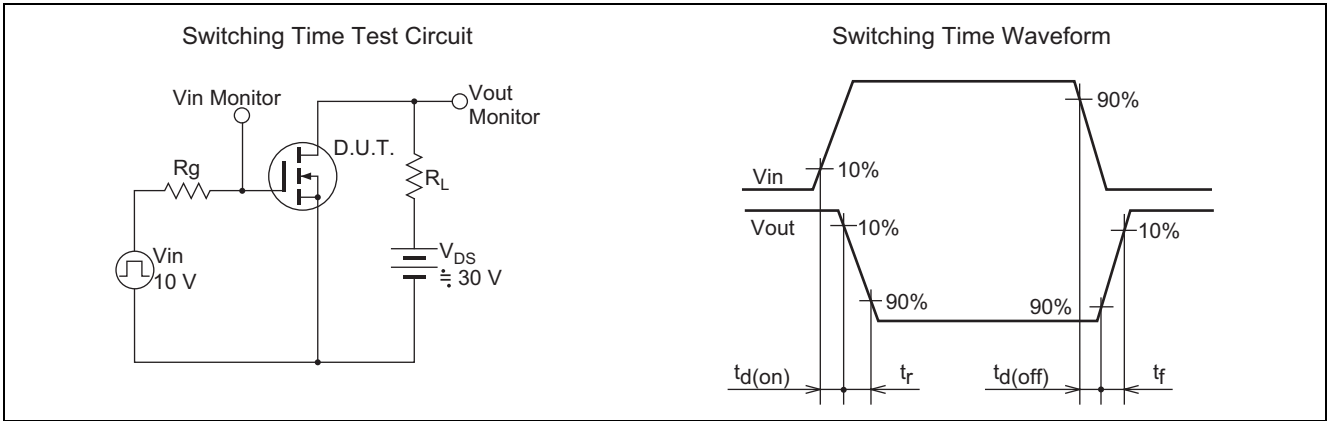
Avalanche Test Circuit



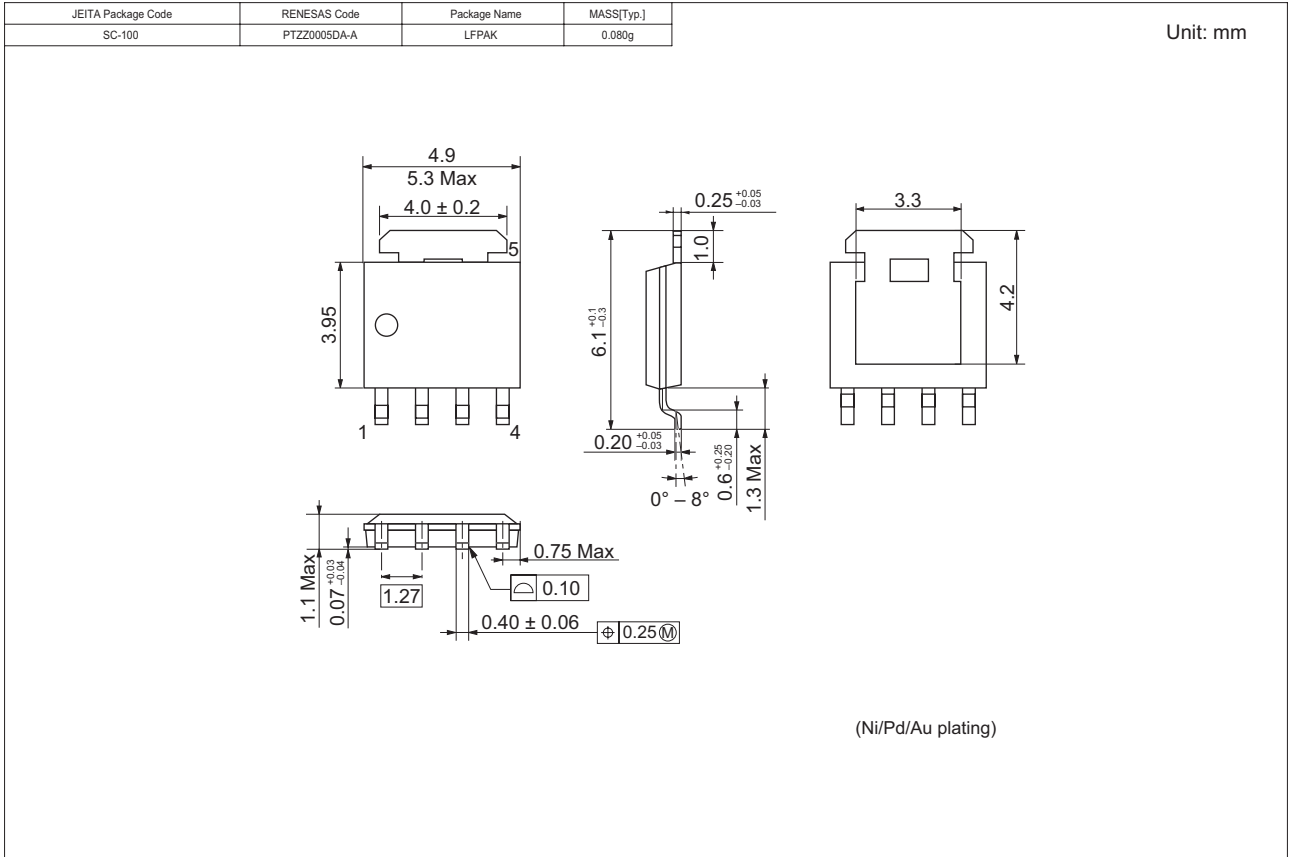
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$





Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAT2175H-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
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Renesas Technology Singapore Pte. Ltd.

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Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

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Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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