HAT1127H

Silicon P Channel Power MOS FET
Power Switching

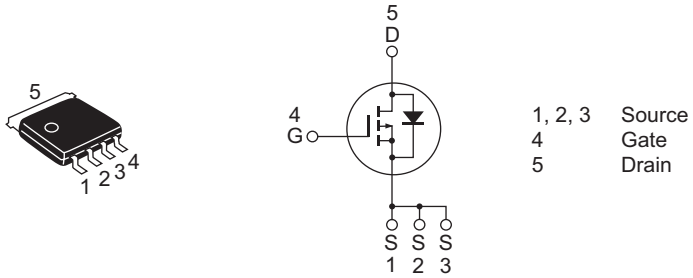
REJ03G1330-0500
Rev.5.00
Jan 20, 2006

Features

- Capable of –4.5 V gate drive
- Low drive current
- High density mounting
- Ultra Low on-resistance
  $R_{DS(on)}$ = 3.6 mΩ typ. (at V_{GS} = –10 V)

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	–20/+10	V
Drain current	I_D	–40	A
Drain peak current	$I_{D(pulse)}$ Note1	–160	A
Body-drain diode reverse drain current	I_{DR}	–40	A
Channel dissipation	Pch Note2	30	W
Channel to Case Thermal Impedance	θch-c Note2	4.17	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Tc = 25°C

Electrical Characteristics

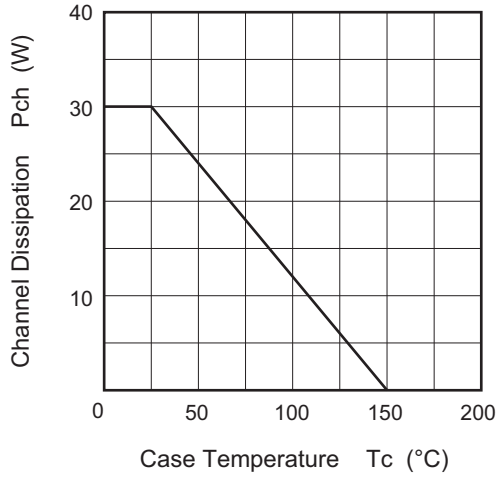
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = –20/+10 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	3.6	4.5	mΩ	I_D = –20 A, V_{GS} = –10 V Note3
	$R_{DS(on)}$	—	5.3	7.7	mΩ	I_D = –20 A, V_{GS} = –4.5 V Note3
Forward transfer admittance	$\|y_{fs}\|$	40	70	—	S	I_D = –20 A, V_{DS} = –10 V Note3
Input capacitance	Ciss	—	5600	—	pF	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	1180	—	pF	
Reverse transfer capacitance	Crss	—	890	—	pF	
Total gate charge	Qg	—	125	—	nC	V_{DD} = –10 V, V_{GS} = –10 V, I_D = –40 A
Gate to source charge	Qgs	—	15	—	nC	
Gate to drain charge	Qgd	—	28	—	nC	
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	V_{GS} = –10 V, I_D = -20 A, V_{DD} ≅ –10 V, R_L = 0.5 Ω, Rg = 4.7 Ω
Rise time	t_r	—	40	—	ns	
Turn-off delay time	$t_{d(off)}$	—	130	—	ns	
Fall time	t_f	—	115	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.88	–1.15	V	I_F = –40 A, V_{GS} = 0 Note3
Body–drain diode reverse recovery time	t_{rr}	—	120	—	ns	I_F = –40 A, V_{GS} = 0 di_F/ dt = 100 A/ µs

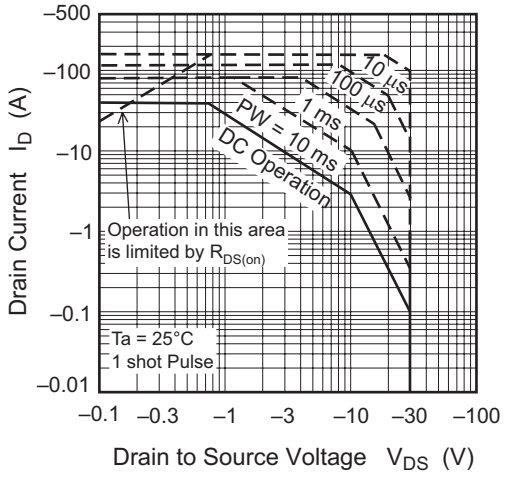
Notes: 3. Pulse test

Main Characteristics

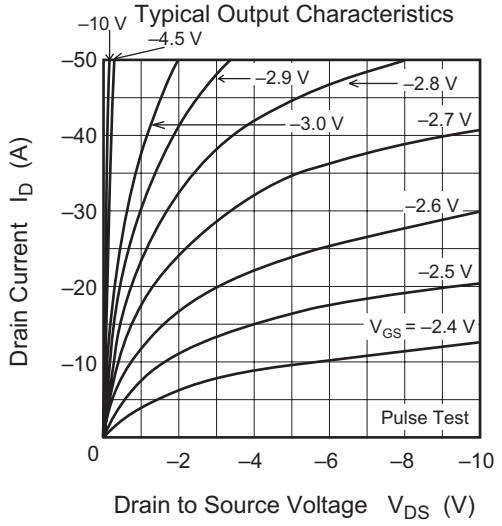
Power vs. Temperature Derating



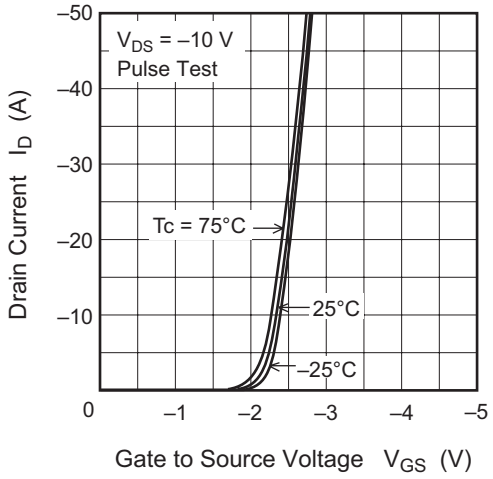
Maximum Safe Operation Area



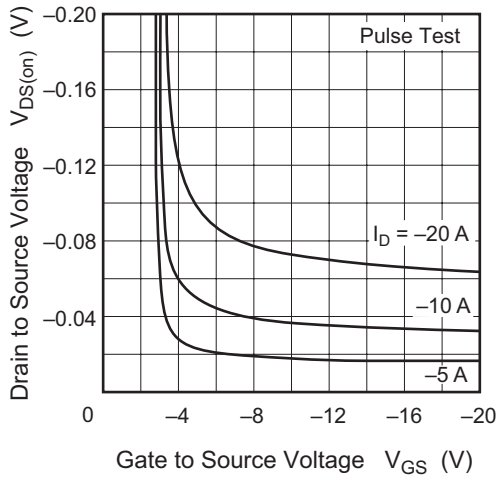
Typical Output Characteristics



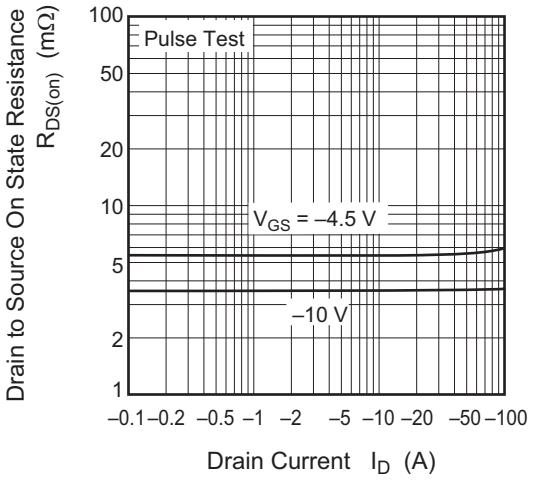
Typical Transfer Characteristics



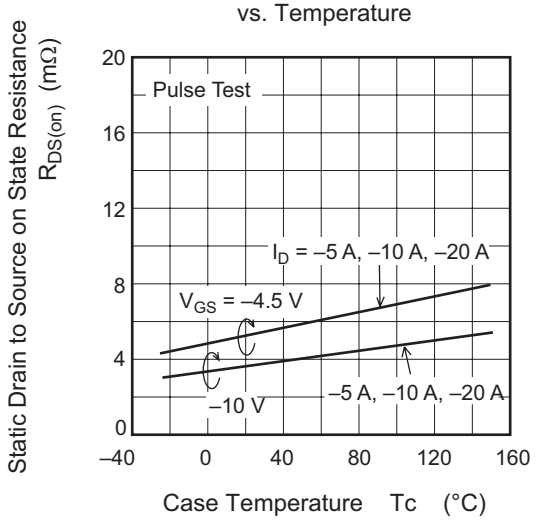
Drain to Source Saturation Voltage vs. Gate to Source Voltage



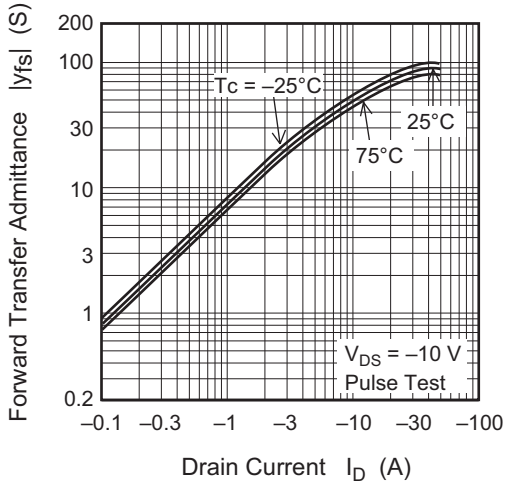
Static Drain to Source on State Resistance vs. Drain Current



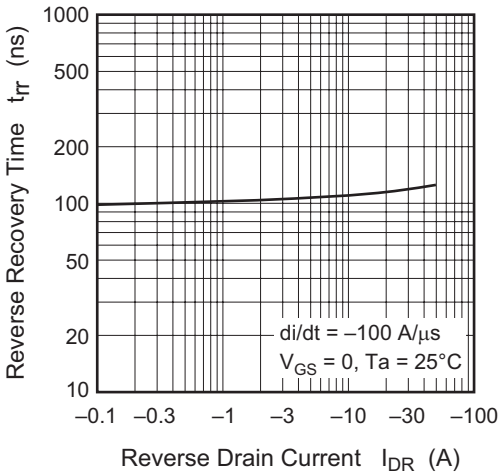
Static Drain to Source on State Resistance vs. Temperature



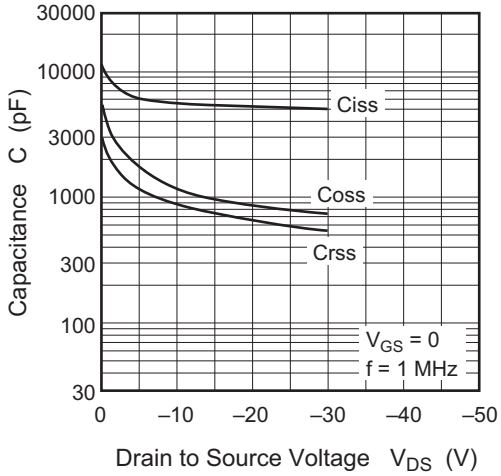
Forward Transfer Admittance vs. Drain Current



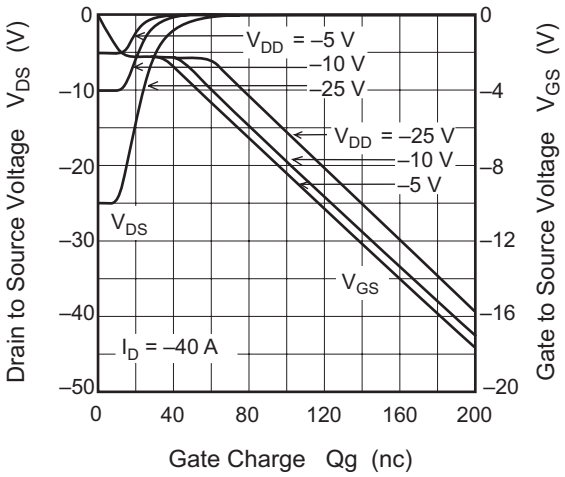
Body–Drain Diode Reverse Recovery Time



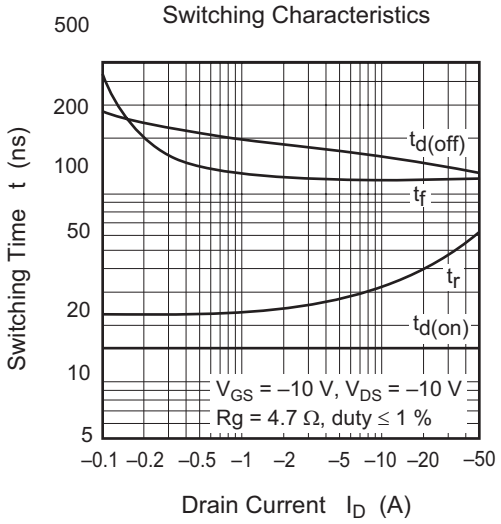
Typical Capacitance vs. Drain to Source Voltage



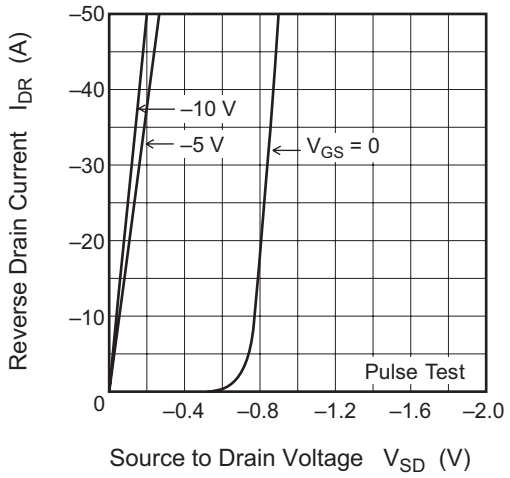
Dynamic Input Characteristics



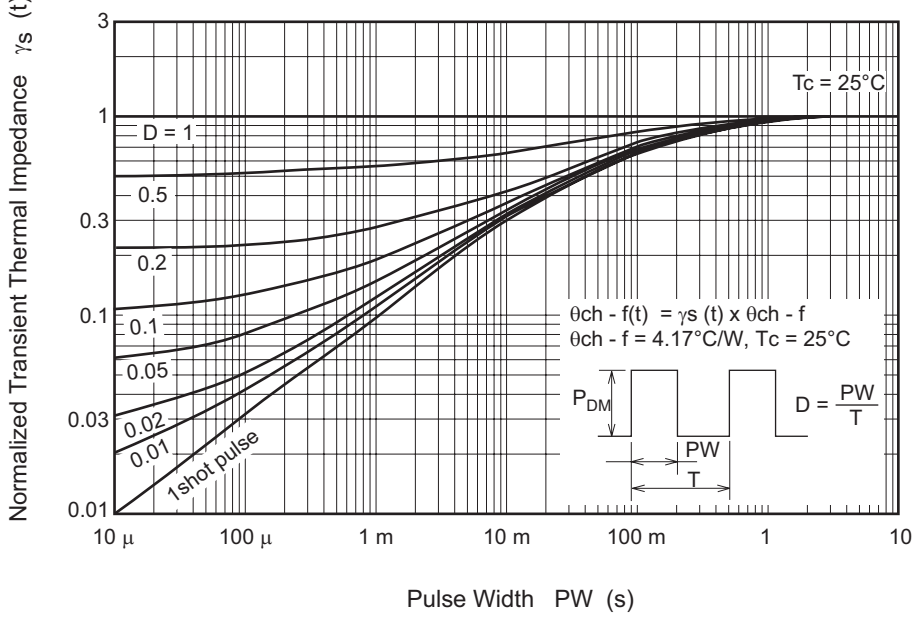
Switching Characteristics



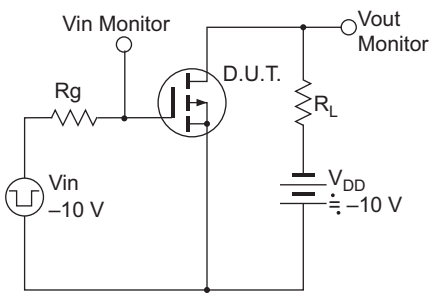
Reverse Drain Current vs.
Source to Drain Voltage



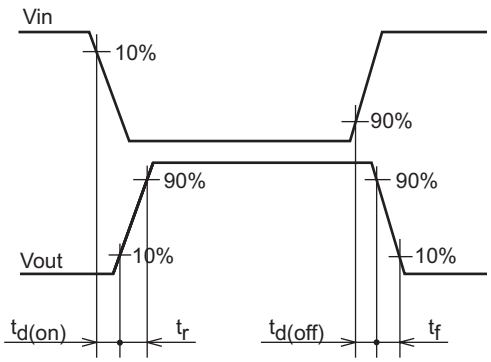
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



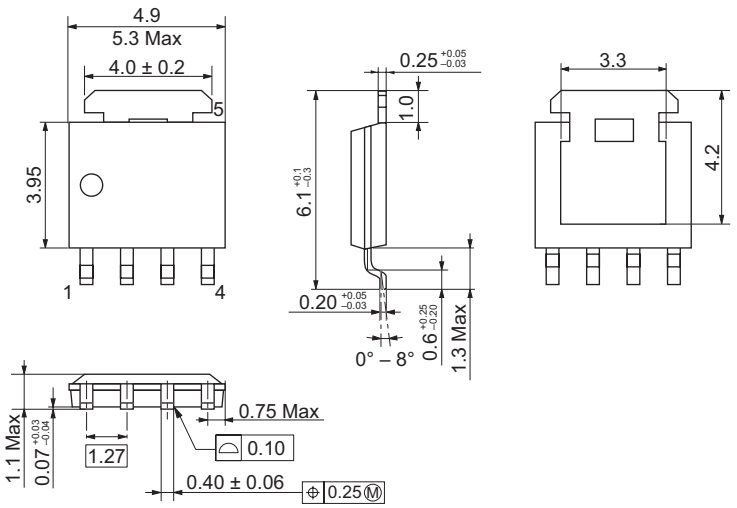
Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LFPAK	SC-100	PTZZ0005DA-A	LFPAKV	0.080g

Unit: mm



(Ni/Pd/Au plating)

Ordering Information

Part Name	Quantity	Shipping Container
HAT1127H-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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