

H7N0310LD, H7N0310LS, H7N0310LM

Silicon N Channel MOS FET
High Speed Power Switching

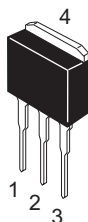
REJ03G1125-0500
(Previous: ADE-208-1422C)
Rev.5.00
Apr 07, 2006

Features

- Low on-resistance
 $R_{DS(on)} = 8 \text{ m}\Omega$ typ.
- Low drive current

Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))



H7N0310LD

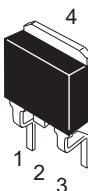
RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK (S)-(1))



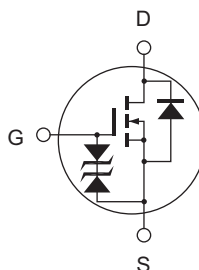
H7N0310LS

1. Gate
2. Drain
3. Source
4. Drain

RENESAS Package code: PRSS0004AE-C
(Package name: LDKPAK (S)-(2))



H7N0310LM



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	30	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	120	A
Body to drain diode reverse drain current	I_{DR}	30	A
Channel dissipation	P_{ch} ^{Note 2}	50	W
Channel to case thermal impedance	θ_{ch-c}	2.5	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value at Tc = 25°C

Electrical Characteristics

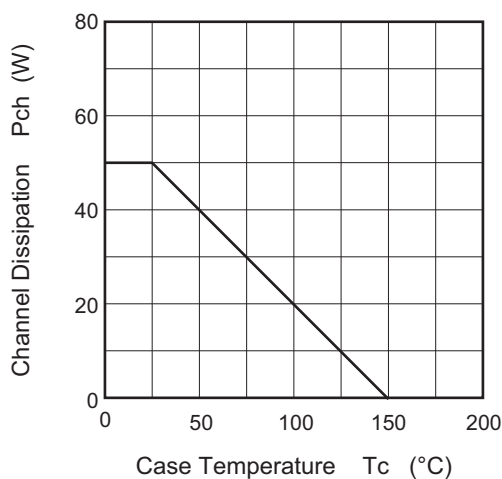
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10\text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 30\text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1\text{ mA}$, $V_{DS} = 10\text{ V}$ ^{Note 3}
Static drain to source on state resistance	$R_{DS(on)}$	—	8.0	10	mΩ	$I_D = 15\text{ A}$, $V_{GS} = 10\text{ V}$ ^{Note 3}
		—	13	19	mΩ	$I_D = 15\text{ A}$, $V_{GS} = 5\text{ V}$ ^{Note 3}
Forward transfer admittance	$ y_{fs} $	21	35	—	S	$I_D = 15\text{ A}$, $V_{DS} = 10\text{ V}$ ^{Note 3}
Input capacitance	C_{iss}	—	1400	—	pF	$V_{DS} = 10\text{ V}$
Output capacitance	C_{oss}	—	380	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	210	—	pF	$f = 1\text{ MHz}$
Total gate charge	Q_g	—	24	—	nC	$V_{DD} = 10\text{ V}$
Gate to source charge	Q_{gs}	—	4.8	—	nC	$V_{GS} = 10\text{ V}$
Gate to drain charge	Q_{gd}	—	4.6	—	nC	$I_D = 30\text{ A}$
Turn-on delay time	$t_{d(on)}$	—	21	—	ns	$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$
Rise time	t_r	—	250	—	ns	$R_L = 0.67\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	$R_g = 4.7\text{ }\Omega$
Fall time	t_f	—	16	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.90	—	V	$I_F = 30\text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	35	—	ns	$I_F = 30\text{ A}$, $V_{GS} = 0$ $di_F/dt = 50\text{ A}/\mu\text{s}$

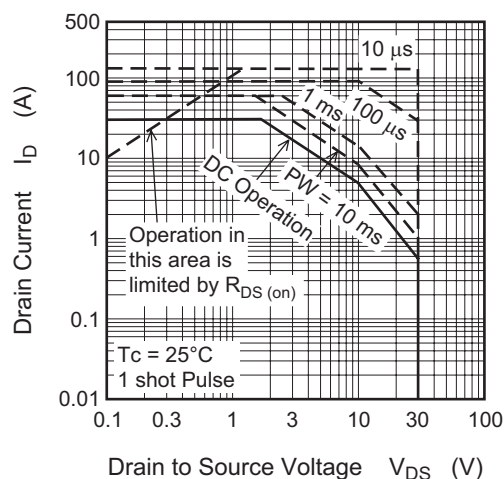
Note: 3. Pulse test

Main Characteristics

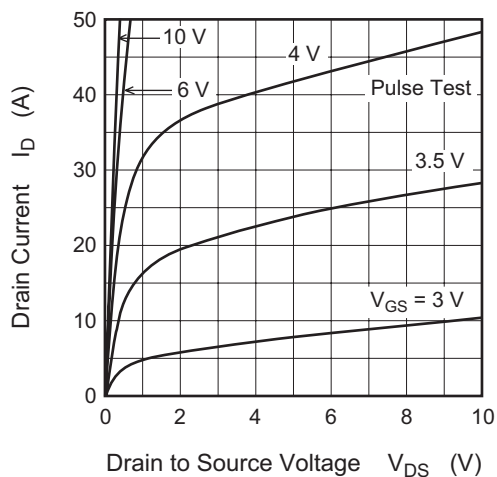
Power vs. Temperature Derating



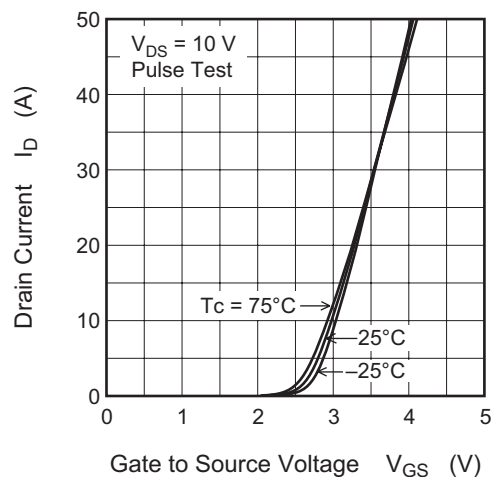
Maximum Safe Operation Area



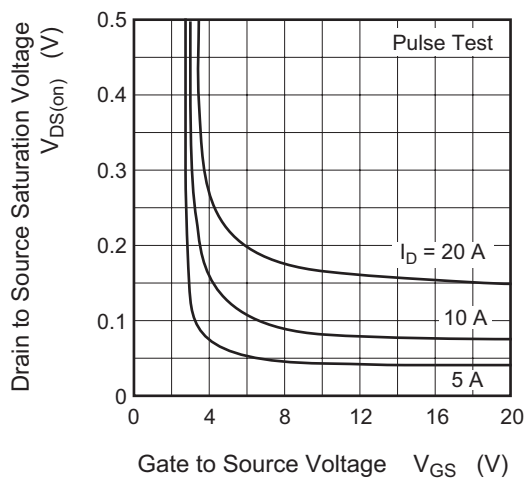
Typical Output Characteristics



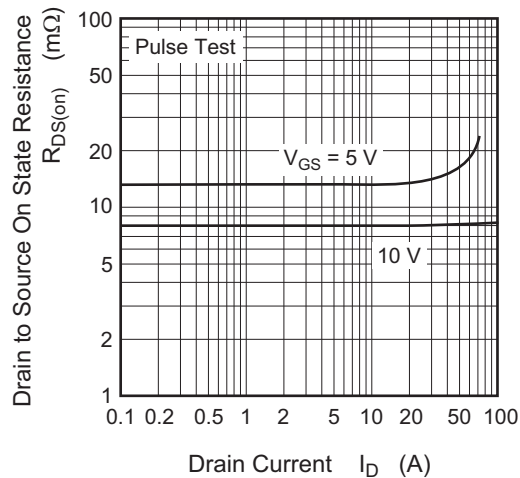
Typical Transfer Characteristics

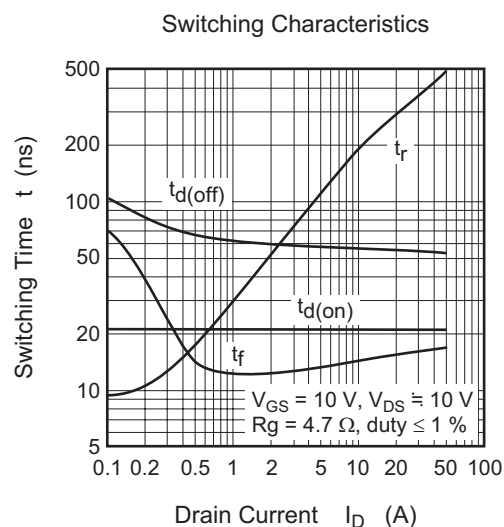
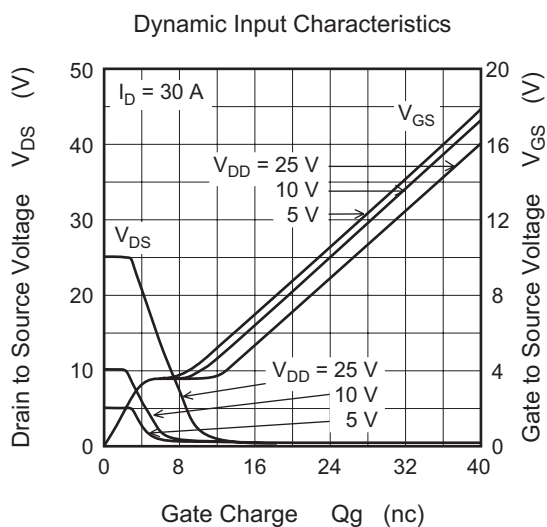
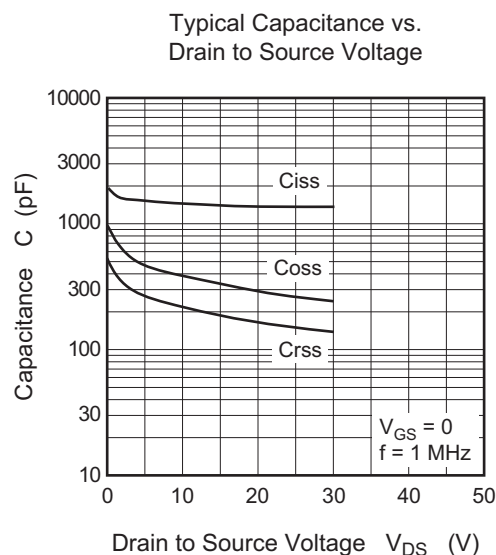
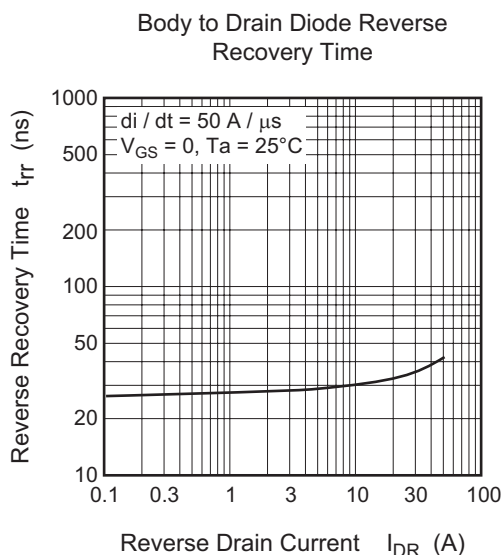
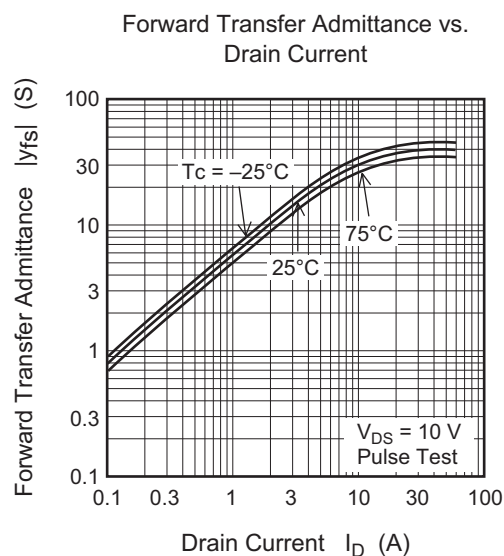
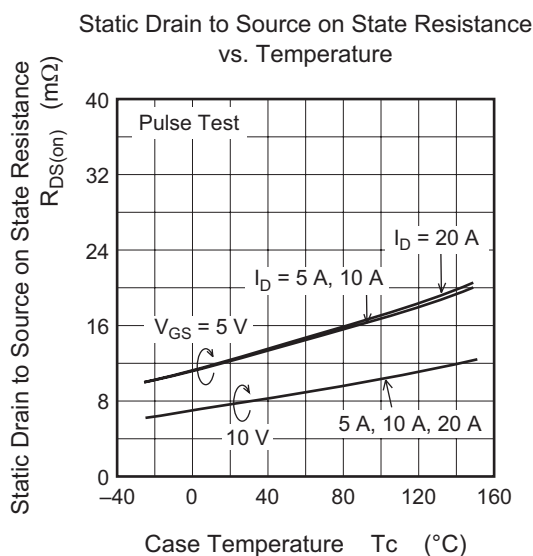


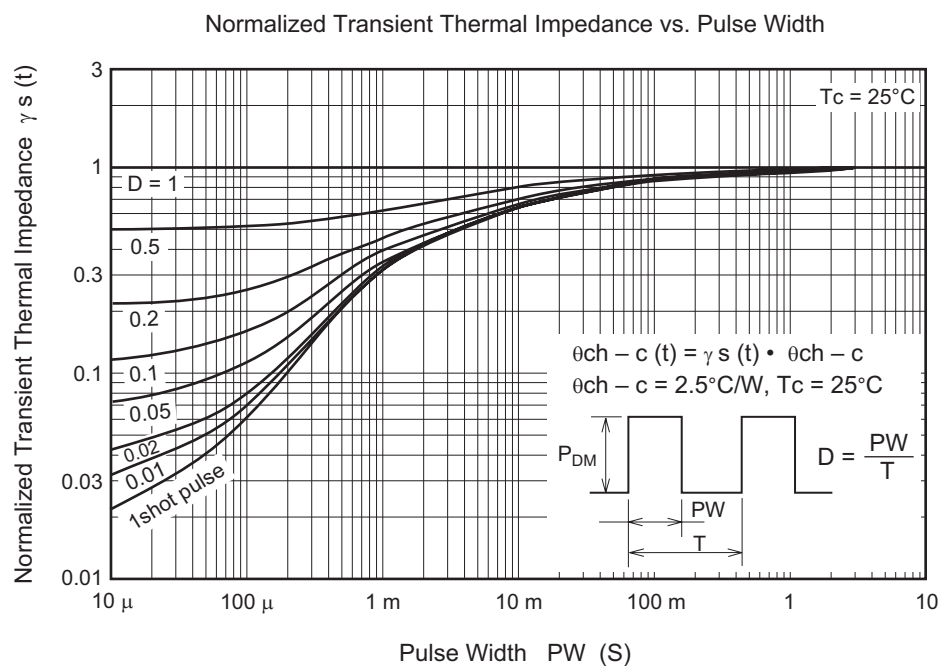
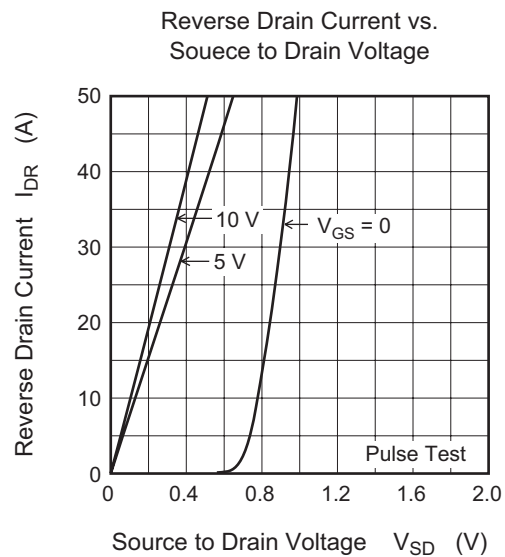
Drain to Source Saturation Voltage vs. Gate to Source Voltage



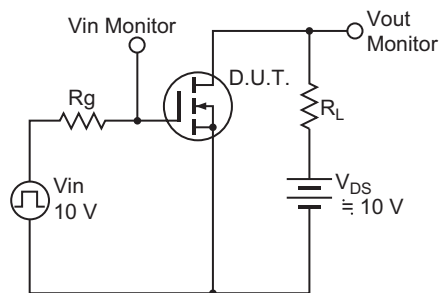
Static Drain to Source on State Resistance vs. Drain Current



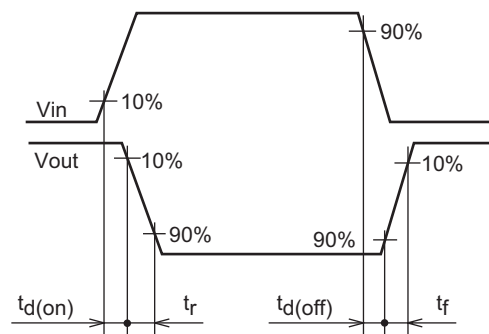




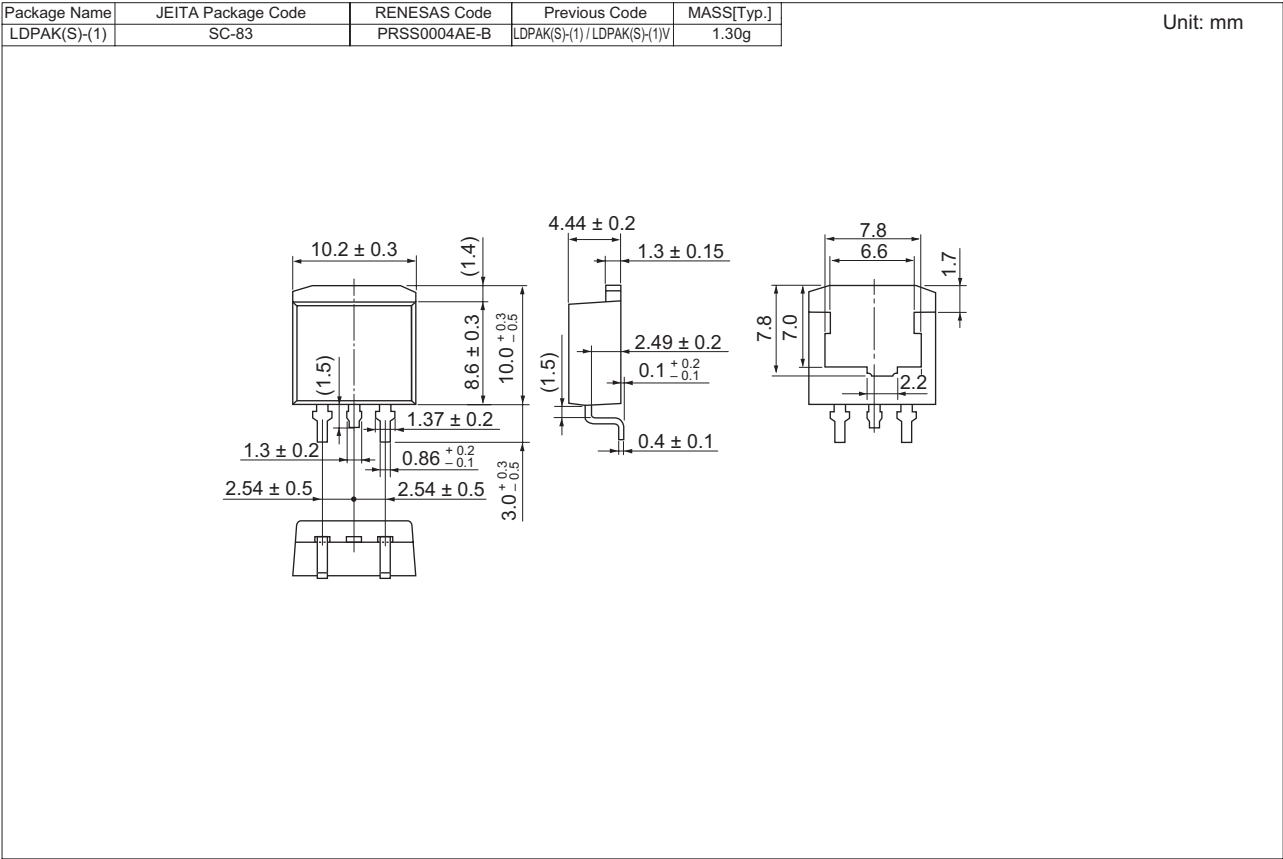
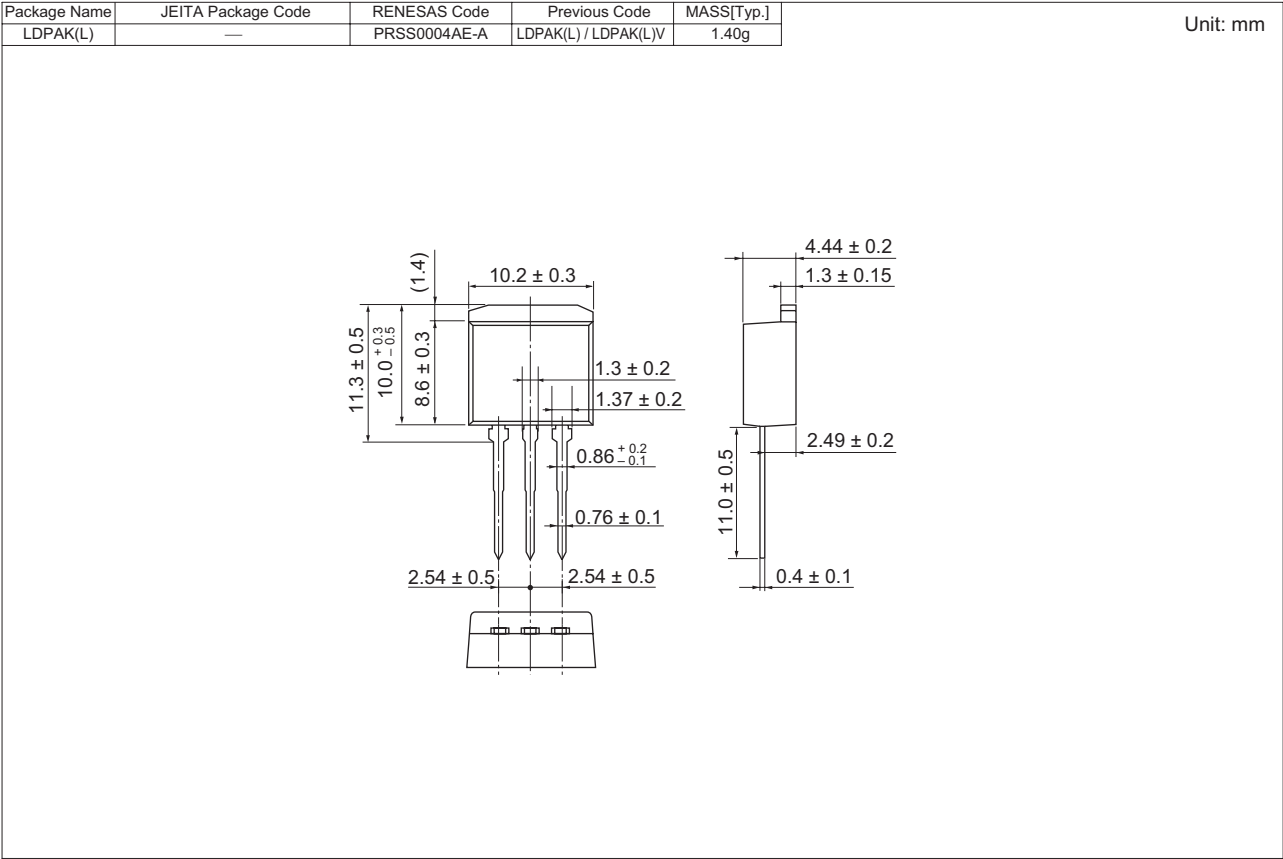
Switching Time Test Circuit



Switching Time Waveform

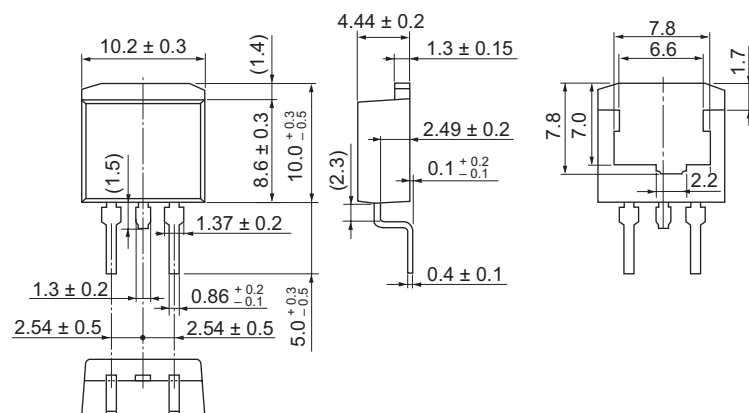


Package Dimensions



Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBPAK(S)-(2)	—	PRSS0004AE-C	LDBPAK(S)-(2) / LDBPAK(S)-(2)V	1.35g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
H7N0310LD-E	500 pcs	Box (Conductive Sack)
H7N0310LSTL-E	1000 pcs	Taping
H7N0310LMTL-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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