NBXSPA008

2.5 V / 3.3 V, 161.1328 MHz LVDS Clock Oscillator

The NBXSPA008 single frequency crystal oscillator (XO) is designed to meet today's requirements for 2.5 V and 3.3 V LVDS clock generation applications. The device uses a high Q fundamental crystal and Phase Lock Loop (PLL) multiplier to provide 161.1328 MHz, ultra low jitter and phase noise LVDS differential output.

This device is a member of ON Semiconductor's PureEdge™ clock family that provides accurate and precision clock solutions.

Available in 5 mm x 7 mm SMD (CLCC) package on 16 mm tape and reel in quantities of 1000.

Features

- LVDS Differential Output
- Uses High Q Fundamental Mode Crystal and PLL Multiplier
- Ultra Low Jitter and Phase Noise − 0.5 ps (12 kHz − 20 MHz)
- Output Frequency − 161.1328 MHz
- Hermetically Sealed Ceramic SMD Package
- RoHS Compliant
- Operating Range: 2.5 V ±5%
  3.3 V ±10%
- Total Frequency Stability − ±50 ppm
- This is a Pb−Free Device

Applications

- Ethernet, Gigabit Ethernet
- WAN
- Networking

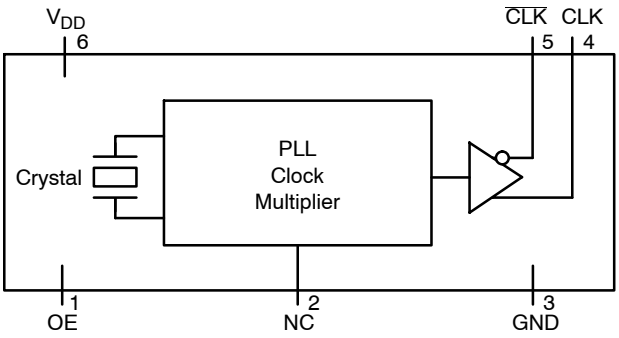

Figure 1. Simplified Logic Diagram

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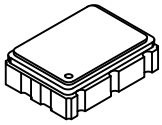


6 PIN CLCC
LN SUFFIX
CASE 848AB

MARKING DIAGRAM

NBXSPA008	= NBXSPA008 (±50 PPM)
161.1328	= Output Frequency (MHz)
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NBXSPA008LN1TAG	CLCC−6 (Pb−Free)	1000/ Tape & Reel
NBXSPA008LNHTAG	CLCC−6 (Pb−Free)	100/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

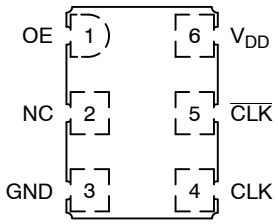


Figure 2. Pin Connections (Top View)

Table 1. PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OE	LVTTL/LVCMOS Control Input	Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2.
2	NC	N/A	No Connect
3	GND	Power Supply	Ground 0 V
4	CLK	LVDS Output	Non−Inverted Clock Output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
5	$\overline{CLK}$	LVDS Output	Inverted Clock Output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
6	V_{DD}	Power Supply	Positive power supply voltage. Voltage should not exceed 2.5 V ±5% or 3.3 V ±10%.

Table 2. OUTPUT ENABLE TRI−STATE FUNCTION

OE Pin	Output Pins
Open	Active
HIGH Level	Active
LOW Level	High Z

Table 3. ATTRIBUTES

Characteristic		Value
Input Default State Resistor		170 kΩ
ESD Protection	Human Body Model Machine Model	2 kV 200 V
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test		

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
I_{out}	LVDS Output Current	Continuous Surge		25 50	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−55 to +120	°C
T_{sol}	Wave Solder	See Figure 5		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC CHARACTERISTICS (V_{DD} = 2.5 V ± 5% or V_{DD} = 3.3 V ± 10%, GND = 0 V, T_A = −40°C to +85°C) (Note 2)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current			85	105	mA
V_{IH}	OE Input HIGH Voltage		2000		V_{DD}	mV
V_{IL}	OE Input LOW Voltage		GND − 300		800	mV
I_{IH}	Input HIGH Current		−100		+100	μA
I_{IL}	Input LOW Current		−100		+100	μA
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States (Note 3)		0	1	25	mV
V_{OS}	Offset Voltage		1125		1375	mV
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States (Note 3)		0	1	25	mV
V_{OH}	Output HIGH Voltage	V_{DD} = 2.5 V V_{DD} = 3.3 V		1425	1600	mV
V_{OL}	Output LOW Voltage	V_{DD} = 2.5 V V_{DD} = 3.3 V	900	1075		mV
V_{OD}	Differential Output Voltage		250		450	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Measurement taken with outputs terminated with 100 ohm across differential pair. See Figure 4.
3. Parameter guaranteed by design verification not tested in production.

Table 6. AC CHARACTERISTICS (V_{DD} = 2.5 V ± 5% or V_{DD} = 3.3 V ± 10%, GND = 0 V, T_A = −40°C to +85°C) (Note 4)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
f_{CLKOUT}	Output Clock Frequency			161.1328		MHz
Δf	Frequency Stability – NBXSPA008	(Note 5)			±50	ppm
Φ_{NOISE}	Phase−Noise Performance f_{CLKout} = 161.1328 MHz (See Figures 3 and NO TAG)	100 Hz of Carrier		−101		dBc/Hz
		1 kHz of Carrier		−119		dBc/Hz
		10 kHz of Carrier		−126		dBc/Hz
		100 kHz of Carrier		−127		dBc/Hz
		1 MHz of Carrier		−135		dBc/Hz
		10 MHz of Carrier		−159		dBc/Hz
$t_{jit}(\Phi)$	RMS Phase Jitter	12 kHz to 20 MHz		0.5	0.75	ps
t_{jitter}	Cycle to Cycle, RMS	1000 Cycles		1	8	ps
	Cycle to Cycle, Peak−to−Peak	1000 Cycles		7	35	ps
	Period, RMS	10,000 Cycles		0.6	4	ps
	Period, Peak−to−Peak	10,000 Cycles		5	20	ps
$t_{OE/OD}$	Output Enable/Disable Time				200	ns
t_{DUTY_CYCLE}	Output Clock Duty Cycle (Measured at Cross Point)		48	50	52	%
t_R	Output Rise Time (20% and 80%)			115	400	ps
t_F	Output Fall Time (80% and 20%)			115	400	ps
t_{start}	Start−up Time			1	5	ms
	Aging	1st Year			3	ppm
		Every Year After 1st			1	ppm

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Measurement taken with outputs terminated with 100 ohm across differential pair. See Figure 4.
5. Parameter guarantees 10 years of aging. Includes initial stability at 25°C, shock, vibration and first year aging.

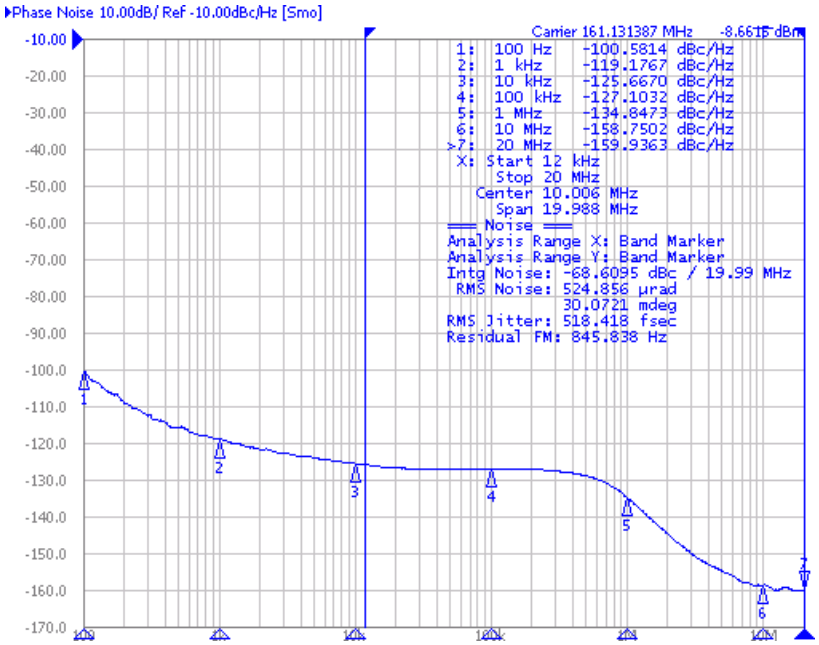


Figure 3. Typical Phase Noise Plot at 161.1328 MHz

Table 7. RELIABILITY COMPLIANCE

Parameter	Standard	Method
Shock	Mechanical	MIL−STD−833, Method 2002, Condition B
Solderability	Mechanical	MIL−STD−833, Method 2003
Vibration	Mechanical	MIL−STD−833, Method 2007, Condition A
Solvent Resistance	Mechanical	MIL−STD−202, Method 215
Resistance to Soldering Heat	Mechanical	MIL−STD−203, Method 210, Condition I or J
Thermal Shock	Environment	MIL−STD−833, Method 1001, Condition A
Moisture Resistance	Environment	MIL−STD−833, Method 1004

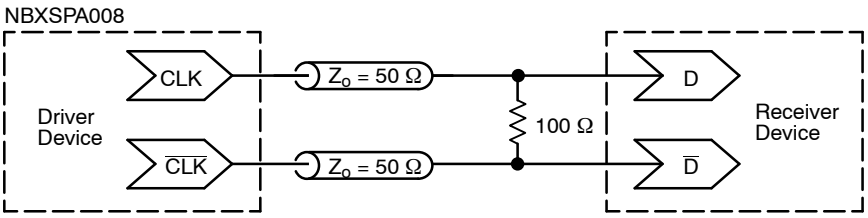


Figure 4. Typical Termination for Output Driver and Device Evaluation

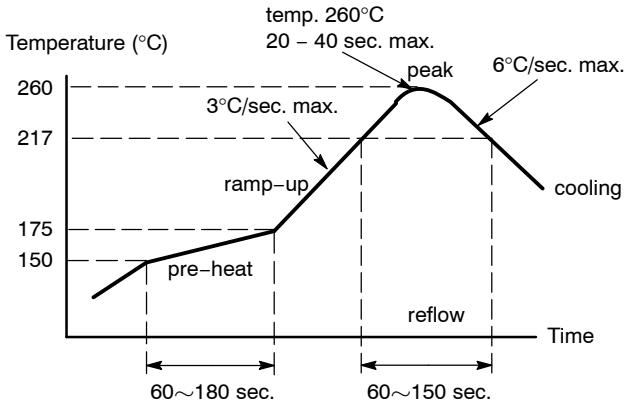
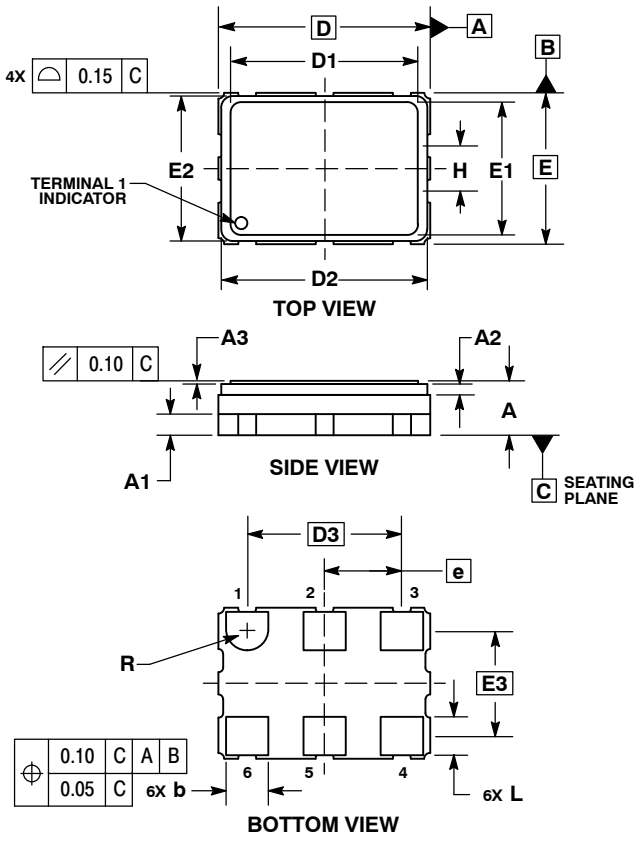


Figure 5. Recommended Reflow Soldering Profile

NBXSPA008

PACKAGE DIMENSIONS

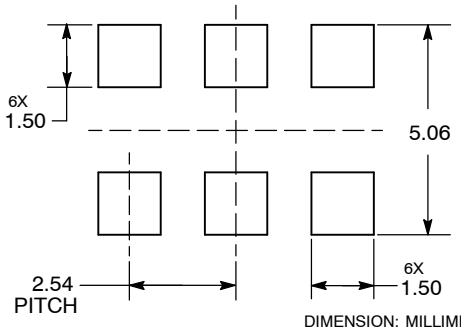
6 PIN CLCC, 7x5, 2.54P
CASE 848AB−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	1.70	1.80	1.90
A1		0.70 REF	
A2		0.36 REF	
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D		7.00 BSC	
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3		5.08 BSC	
E		5.00 BSC	
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3		3.49 BSC	
e		2.54 BSC	
H		1.80 REF	
L	1.17	1.27	1.37
R		0.70 REF	

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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