

FEATURES

- DC to 4.25 Gbps per port NRZ data rate
- Programmable receive equalization
 - 12 dB boost at 2 GHz
- Compensates 40 inches of FR4 at 4.25 Gbps
- Programmable transmit preemphasis/deemphasis
 - Up to 12 dB boost at 4.25 Gbps
- Compensates 40 inches of FR4 at 4.25 Gbps
- Low power: 130 mW per channel at 3.3 V (outputs enabled)
- 16 × 16, fully differential, nonblocking array
 - Double rank connection programming with dual connection maps
- Low jitter, typically 20 ps
- Flexible I/O supply range
- DC- or ac-coupled differential CML inputs
- Programmable CML output levels
- Per-lane input P/N pair inversion for routing ease
- 50 Ω on-chip I/O termination
- Supports 8b/10b, scrambled or uncoded NRZ data
- Serial (I²C slave or SPI) control interface
- 100-lead TQFP, Pb-free package

APPLICATIONS

- Fiber optic network switching
- High speed serial backplane routing to OC-48 with FEC
- XAUI: 10GBASE-KX4
- Gigabit Ethernet over backplane: 1000BASE-KX
- 1×, 2×, and 4× Fibre Channel
- InfiniBand®
- Digital video (HDMI, DVI, DisplayPort, 3G-/HD-/SD-SDI)
- Data storage networks

GENERAL DESCRIPTION

The ADN4604 is a 16 × 16 asynchronous, protocol agnostic, digital crosspoint switch, with 16 differential PECL-/CML-compatible inputs and 16 differential CML outputs.

The ADN4604 is optimized for nonreturn-to-zero (NRZ) signaling with data rates of up to 4.25 Gbps per port. Each port offers a fixed level of input equalization and programmable output swing and output preemphasis.

FUNCTIONAL BLOCK DIAGRAM

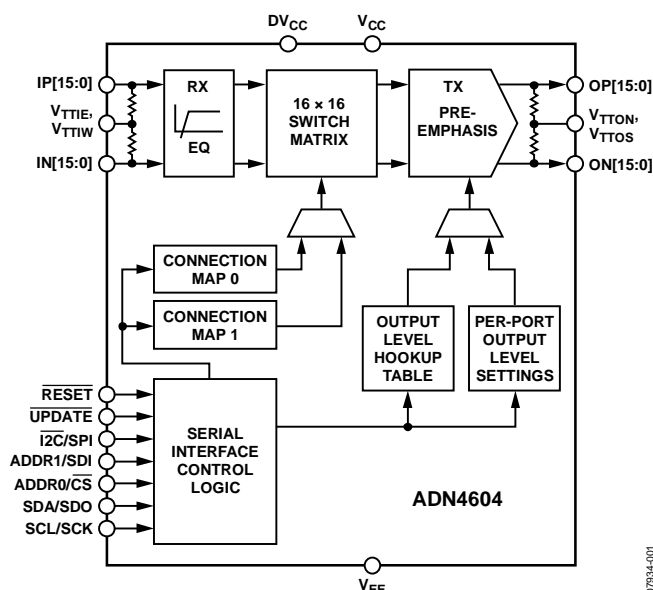


Figure 1.

The ADN4604 nonblocking switch core implements a 16 × 16 crossbar and supports independent channel switching through the serial control interface. The ADN4604 has low latency and very low channel-to-channel skew.

An I²C® or SPI interface is used to control the device and provide access to advanced features, such as additional levels of preemphasis and output disable.

The ADN4604 is packaged in a 100-lead TQFP package and operates from –40°C to +85°C.

Rev. 0

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REVISION HISTORY

10/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

$V_{CC} = 3.3\text{ V}$, $V_{TTk} = 3.3\text{ V}$, $V_{TTOx} = 3.3\text{ V}$, $DV_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 50\ \Omega$, data rate = 4.25 Gbps, ac-coupled inputs and outputs, differential input swing = 800 mV p-p, $T_A = 27^\circ\text{C}$, unless otherwise noted.

Table 1.

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|------------------|----------|----------------|-------------------------|
| DYNAMIC PERFORMANCE | | | | | |
| Data Rate (DR) per Channel (NRZ) | | DC | | 4.25 | Gbps |
| Deterministic Jitter | Data rate = 4.25 Gbps, no channel | | 20 | | ps p-p |
| Random Jitter | RMS, no channel | | 1 | | ps rms |
| Residual Deterministic Jitter with Receive Equalization | Data rate = 4.25 Gbps, 20 in. FR4, EQ boost = 12 dB | | 27 | | ps p-p |
| | Data rate = 4.25 Gbps, 30 in. FR4, EQ boost = 12 dB | | 43 | | ps p-p |
| | Data rate = 4.25 Gbps, 40 in. FR4, EQ boost = 12 dB | | 70 | | ps p-p |
| | Data rate = 4.25 Gbps, 20 in. FR4, PE boost = 4.2 dB | | 23 | | ps p-p |
| Residual Deterministic Jitter with Transmit Preemphasis | Data rate = 4.25 Gbps, 30 in. FR4, PE boost = 6 dB | | 25 | | ps p-p |
| | Data rate = 4.25 Gbps, 40 in. FR4, PE boost = 6 dB | | 35 | | ps p-p |
| Propagation Delay | Input to output, EQ boost = 12 dB | | 800 | | ps |
| Channel-to-Channel Skew | | | ± 50 | | ps |
| Switching Time | Update logic switching to 50% output data | | 100 | | ns |
| Output Rise/Fall Time | 20% to 80% | | 75 | | ps |
| INPUT CHARACTERISTICS | | | | | |
| Differential Input Voltage Swing | $V_{ICM}^1 = V_{CC} - 0.6\text{ V}$; $V_{CC} = V_{MIN}$ to V_{MAX} , $T_A = T_{MIN}$ to T_{MAX} | 200 | | 2000 | mV p-p diff |
| Input Voltage Range | Single-ended absolute voltage level, V_L | $V_{EE} + 1.1$ | | | V |
| | Single-ended absolute voltage level, V_H | | | $V_{CC} + 0.3$ | V |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Differential, PE boost = 0 dB, default output level, at dc | 600 | 800 | 900 | mV p-p diff |
| Output Voltage Range | Single-ended absolute voltage level, V_L | $V_{CC} - 1.3$ | | | V |
| | Single-ended absolute voltage level, V_H | | | $V_{CC} + 0.2$ | V |
| Per-Port Output Current | PE boost = 0 dB, default output level | | 16 | | mA |
| | PE boost = 6 dB, default output level | | 32 | | mA |
| TERMINATION CHARACTERISTICS | | | | | |
| Resistance | Single-ended, $V_{CC} = 2.7\text{ V}$ to 3.6 V , $V_{TTI} = 2.2\text{ V}$ to 3.6 V , $V_{TTO} = 2.2\text{ V}$ to 3.6 V , $T_A = T_{MIN}$ to T_{MAX} | 44 | 50 | 56 | Ω |
| Temperature Coefficient | | | 0.025 | | $\Omega/^\circ\text{C}$ |
| POWER SUPPLY | | | | | |
| Operating Range | | | | | |
| V_{CC} | $V_{EE} = 0\text{ V}$ | 2.7 | 3.3 | 3.6 | V |
| DV_{CC} | $V_{EE} = 0\text{ V}$ | 2.7 | 3.3 | 3.6 | V |
| V_{TTIE} , V_{TTIW} | $V_{EE} = 0\text{ V}$ | 1.3 | 3.3 | $V_{CC} + 0.3$ | V |
| V_{TTON} , V_{TTOS} | $V_{EE} = 0\text{ V}$ | 2.2 ² | 3.3 | $V_{CC} + 0.3$ | V |
| Supply Current | | | | | |
| I_{CC} | Outputs disabled | | 95 | 110 | mA |
| I_{DVCC} | | | 20 | 35 | mA |
| $I_{TTIE} + I_{TTIW} + I_{TTON} + I_{TTOS}$ | | | 0 | 10 | mA |
| Supply Current | | | | | |
| I_{CC} | All outputs enabled, ac-coupled I/O, 400 mV I/O swings (800 mV p-p differential), PE boost = 0 dB, 50 Ω far-end terminations | | 342 | 370 | mA |
| I_{DVCC} | | | 20 | 35 | mA |
| $I_{TTIE} + I_{TTIW} + I_{TTON} + I_{TTOS}$ | | | 256 | 280 | mA |
| Supply Current | | | | | |
| I_{CC} | All outputs enabled, ac-coupled I/O, 400 mV I/O swings (800 mV p-p differential), PE boost = 6 dB, 50 Ω far-end terminations | | 486 | 540 | mA |
| I_{DVCC} | | | 20 | 35 | mA |
| $I_{TTIE} + I_{TTIW} + I_{TTON} + I_{TTOS}$ | | | 512 | 540 | mA |

ADN4604

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|---------------------|-----------|---------------------|------|
| THERMAL CHARACTERISTICS | | | | | |
| Operating Temperature Range | | -40 | | +85 | °C |
| θ_{JA} | Still air; JEDEC 4-layer test board | | 24.9 | | °C/W |
| θ_{JB} | Still air | | 11.6 | | °C/W |
| θ_{JC} | At the exposed pad | | 0.95 | | °C/W |
| LOGIC CHARACTERISTICS | | | | | |
| Input High Voltage Threshold (V_{IH}) | $DV_{CC} = 3.3\text{ V}$ | $0.7 \times V_{CC}$ | | V_{CC} | V |
| Input Low Voltage Threshold (V_{IL}) | $DV_{CC} = 3.3\text{ V}$ | V_{EE} | | $0.3 \times V_{CC}$ | V |
| Output High Voltage (V_{OH}) | 2 k Ω pull-up resistor to DV_{CC} | | DV_{CC} | | V |
| Output Low Voltage (V_{OL}) | $I_{OL} = 3\text{ mA}$ | V_{EE} | | 0.4 | V |

¹ V_{ICM} is the input common-mode voltage.

² Minimum V_{TTO} is only applicable for a limited range of output current settings. Refer to the Power Dissipation section.

I²C TIMING SPECIFICATIONS

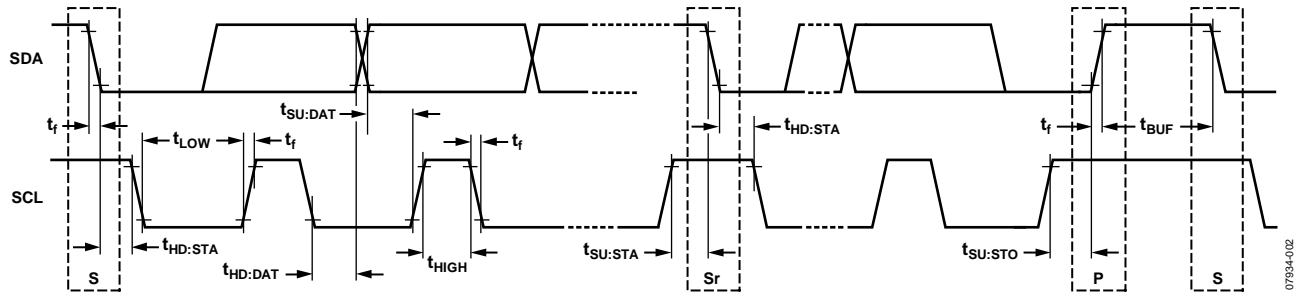


Figure 2. I²C Timing Diagram

Table 2. I²C Timing Specifications

| Parameter | Symbol | Min | Max | Unit |
|--|--------------|-----|------|---------------|
| SCL Clock Frequency | f_{SCL} | 0 | 400+ | kHz |
| Hold Time for a Start Condition | $t_{HD:STA}$ | 0.6 | | μs |
| Setup Time for a Repeated Start Condition | $t_{SU:STA}$ | 0.6 | | μs |
| Low Period of the SCL Clock | t_{LOW} | 1.3 | | μs |
| High Period of the SCL Clock | t_{HIGH} | 0.6 | | μs |
| Data Hold Time | $t_{HD:DAT}$ | 0 | | μs |
| Data Setup Time | $t_{SU:DAT}$ | 10 | | ns |
| Rise Time for Both SDA and SCL | t_r | 1 | 300 | ns |
| Fall Time for Both SDA and SCL | t_f | 1 | 300 | ns |
| Setup Time for Stop Condition | $t_{SU:STO}$ | 0.6 | | μs |
| Bus-Free Time Between a Stop Condition and a Start Condition | t_{BUF} | 1 | | ns |
| Bus Idle Time After a Reset | | 10 | | ns |
| Reset Pulse Width | | 10 | | ns |

SPI TIMING SPECIFICATIONS

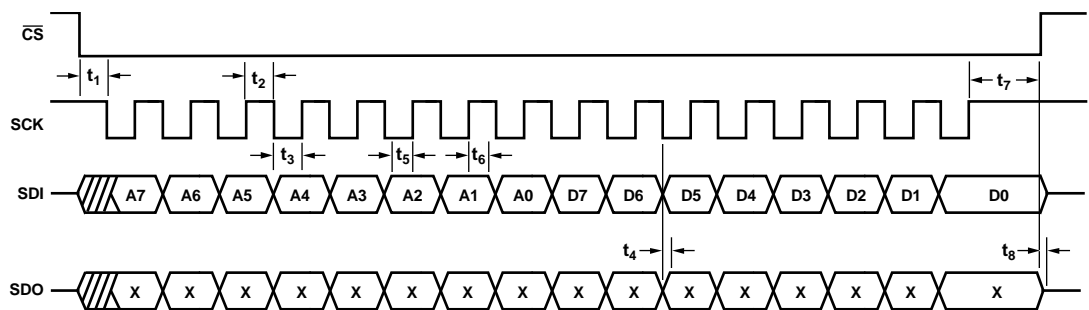


Figure 3. SPI Write Timing Diagram

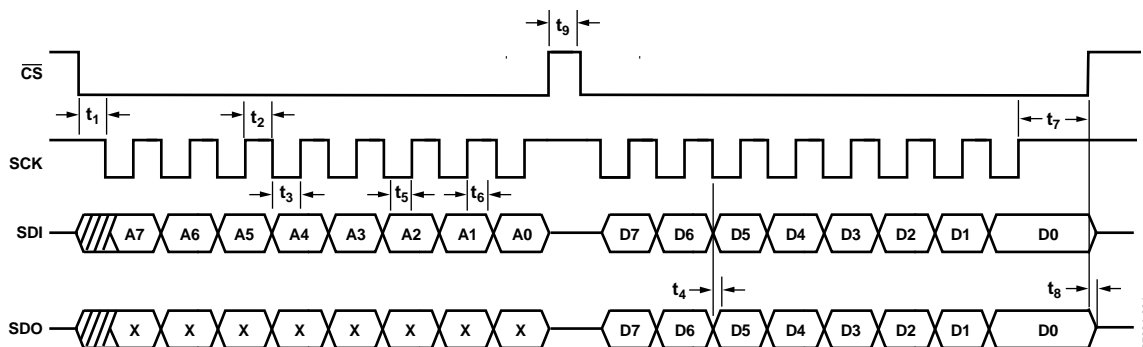


Figure 4. SPI Read Timing Diagram

Table 3. SPI Timing Specifications

| Parameter | Symbol | Min | Max | Unit |
|--|-----------|-----|-----|------|
| SCK Clock Frequency | f_{SCK} | 0 | 10 | MHz |
| \overline{CS} to SCK Setup Time | t_1 | 10 | | ns |
| SCK High Pulse Width | t_2 | 40 | | ns |
| SCK Low Pulse Width | t_3 | 40 | | ns |
| Data Access Time After SCK Falling Edge | t_4 | | 35 | ns |
| Data Setup Time Prior to SCK Rising Edge | t_5 | 20 | | ns |
| Data Hold Time After SCK Rising Edge | t_6 | 10 | | ns |
| \overline{CS} to SCK Hold Time | t_7 | 10 | | ns |
| \overline{CS} to SDO High Impedance | t_8 | | 40 | ns |
| \overline{CS} High Pulse Width | t_9 | 10 | | ns |

ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter | Rating |
|---|---|
| V _{CC} to V _{EE} | 3.7 V |
| DV _{CC} to V _{EE} | 3.7 V |
| V _{TTIE} , V _{TTIW} | V _{CC} + 0.6 V |
| V _{TTON} , V _{TTOS} | V _{CC} + 0.6 V |
| Internal Power Dissipation ¹ | 4.9 W |
| Differential Input Voltage | 2.0 V |
| Logic Input Voltage | V _{EE} – 0.3 V < V _{IN} < V _{CC} + 0.6 V |
| Storage Temperature Range | –65°C to +125°C |
| Lead Temperature Range | 300°C |
| Junction Temperature | 150°C |

¹ Internal power dissipation is for the device in free air.
T_A = 27°C; θ_{JA} = 24.9°C/W in still air.

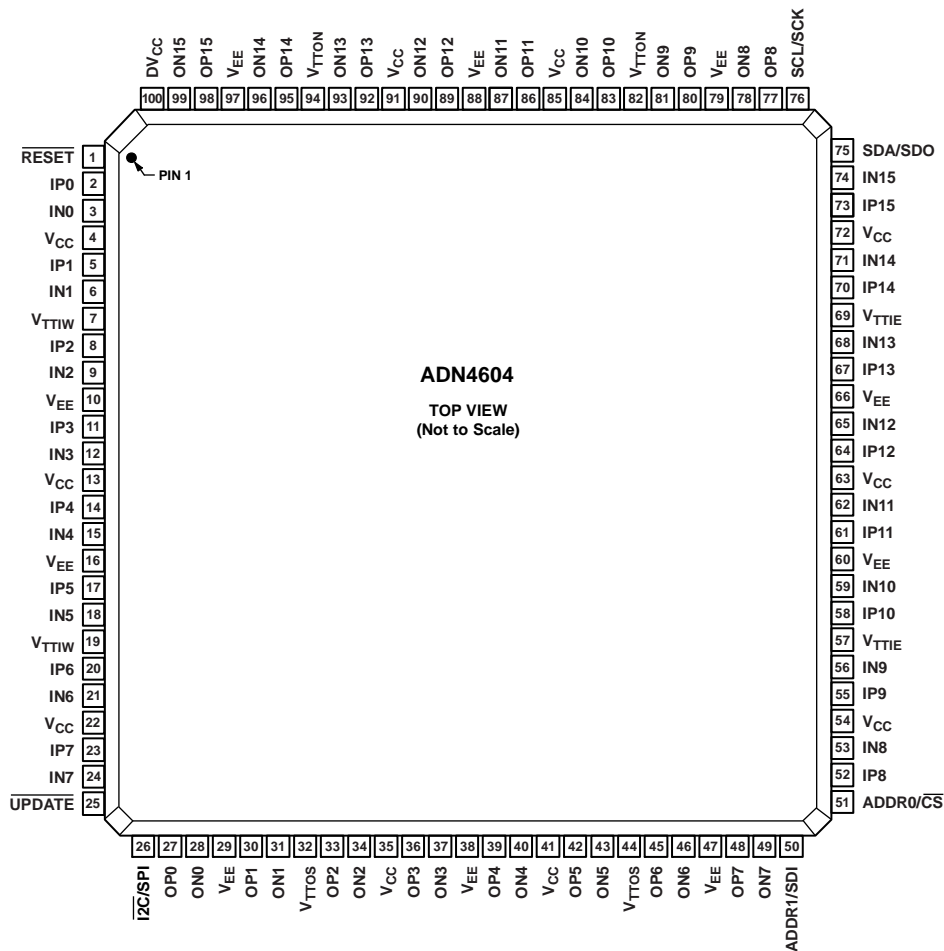
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES
1. THE ADN4604 TQFP HAS AN EXPOSED PADDLE (EPAD) ON THE UNDERSIDE OF THE PACKAGE THAT AIDS IN HEAT DISSIPATION. THE EPAD MUST BE ELECTRICALLY CONNECTED TO THE V_{EE} SUPPLY PLANE TO MEET THERMAL SPECIFICATIONS.
 2. SDA/SCL/ADDR1/0 FOR I²C OPERATION.
SCK/SDO/SDI/CS FOR SPI OPERATION.

Figure 5. Pin Configuration

07334-005

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description |
|--|-------------------------------|---------|---|
| 1 | RESET | Control | Configuration Registers Reset, Active Low. This pin is normally pulled up to DV _{CC} . |
| 2 | IP0 | Input | High Speed Input. |
| 3 | IN0 | Input | High Speed Input Complement. |
| 4, 13, 22, 35, 41, 54, 63, 72, 85, 91 | V _{CC} | Power | Positive Supply. |
| 5 | IP1 | Input | High Speed Input. |
| 6 | IN1 | Input | High Speed Input Complement. |
| 7, 19 | V _{TTIW} | Power | Input Termination Supply (West). These pins are normally tied to the V _{TTIE} pins. |
| 8 | IP2 | Input | High Speed Input. |
| 9 | IN2 | Input | High Speed Input Complement. |
| 10, 16, 29, 38, 47, 60, 66, 79, 88, 97, EPAD | V _{EE} | Power | Negative Supply. |
| 11 | IP3 | Input | High Speed Input. |
| 12 | IN3 | Input | High Speed Input Complement. |
| 14 | IP4 | Input | High Speed Input. |
| 15 | IN4 | Input | High Speed Input Complement. |
| 17 | IP5 | Input | High Speed Input. |
| 18 | IN5 | Input | High Speed Input Complement. |
| 20 | IP6 | Input | High Speed Input. |
| 21 | IN6 | Input | High Speed Input Complement. |
| 23 | IP7 | Input | High Speed Input. |
| 24 | IN7 | Input | High Speed Input Complement. |
| 25 | UPDATE | Control | Second Rank Write Enable, Active Low. This pin is normally pulled up to DV _{CC} . |
| 26 | I ² C/SPI | Control | I ² C/SPI Control Interface Selection, I ² C Active Low. |
| 27 | OP0 | Output | High Speed Output. |
| 28 | ON0 | Output | High Speed Output Complement. |
| 30 | OP1 | Output | High Speed Output. |
| 31 | ON1 | Output | High Speed Output Complement. |
| 32, 44 | V _{TTOS} | Power | Output Termination Supply (South). These pins are normally tied to the V _{TTON} pins. |
| 33 | OP2 | Output | High Speed Output. |
| 34 | ON2 | Output | High Speed Output Complement. |
| 36 | OP3 | Output | High Speed Output. |
| 37 | ON3 | Output | High Speed Output Complement. |
| 39 | OP4 | Output | High Speed Output. |
| 40 | ON4 | Output | High Speed Output Complement. |
| 42 | OP5 | Output | High Speed Output. |
| 43 | ON5 | Output | High Speed Output Complement. |
| 45 | OP6 | Output | High Speed Output. |
| 46 | ON6 | Output | High Speed Output Complement. |
| 48 | OP7 | Output | High Speed Output. |
| 49 | ON7 | Output | High Speed Output Complement. |
| 50 | ADDR1/SDI | Control | I ² C Slave Address Bit 1 (MSB) or SPI Data Input. |
| 51 | ADDR0/ $\overline{\text{CS}}$ | Control | I ² C Slave Address Bit 0 (LSB) or SPI Chip Select (Active Low). |
| 52 | IP8 | Input | High Speed Input. |
| 53 | IN8 | Input | High Speed Input Complement. |
| 55 | IP9 | Input | High Speed Input. |
| 56 | IN9 | Input | High Speed Input Complement. |

| Pin No. | Mnemonic | Type | Description |
|---------|-------------------|---------|--|
| 57, 69 | V _{TTIE} | Power | Input Termination Supply (East). These pins are normally tied to the V _{TTIW} pins. |
| 58 | IP10 | Input | High Speed Input. |
| 59 | IN10 | Input | High Speed Input Complement. |
| 61 | IP11 | Input | High Speed Input. |
| 62 | IN11 | Input | High Speed Input Complement. |
| 64 | IP12 | Input | High Speed Input. |
| 65 | IN12 | Input | High Speed Input Complement. |
| 67 | IP13 | Input | High Speed Input. |
| 68 | IN13 | Input | High Speed Input Complement. |
| 70 | IP14 | Input | High Speed Input. |
| 71 | IN14 | Input | High Speed Input Complement. |
| 73 | IP15 | Input | High Speed Input. |
| 74 | IN15 | Input | High Speed Input Complement. |
| 75 | SDA/SDO | Control | I ² C Data or SPI Data Output. |
| 76 | SCL/SCK | Control | I ² C Clock or SPI Clock. |
| 77 | OP8 | Output | High Speed Output. |
| 78 | ON8 | Output | High Speed Output Complement. |
| 80 | OP9 | Output | High Speed Output. |
| 81 | ON9 | Output | High Speed Output Complement. |
| 82, 94 | V _{TTON} | Power | Output Termination Supply (North). These pins are normally tied to the V _{TTOS} pins. |
| 83 | OP10 | Output | High Speed Output. |
| 84 | ON10 | Output | High Speed Output Complement. |
| 86 | OP11 | Output | High Speed Output. |
| 87 | ON11 | Output | High Speed Output Complement. |
| 89 | OP12 | Output | High Speed Output. |
| 90 | ON12 | Output | High Speed Output Complement. |
| 92 | OP13 | Output | High Speed Output. |
| 93 | ON13 | Output | High Speed Output Complement. |
| 95 | OP14 | Output | High Speed Output. |
| 96 | ON14 | Output | High Speed Output Complement. |
| 98 | OP15 | Output | High Speed Output. |
| 99 | ON15 | Output | High Speed Output Complement. |
| 100 | DV _{CC} | Power | Digital Positive Supply. |

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 3.3\text{ V}$, $V_{TTK} = 3.3\text{ V}$, $V_{TTOx} = 3.3\text{ V}$, $DV_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 50\ \Omega$, data rate = 4.25 Gbps, ac-coupled inputs and outputs, differential input swing = 800 mV p-p, $T_A = 27^\circ\text{C}$, unless otherwise noted.

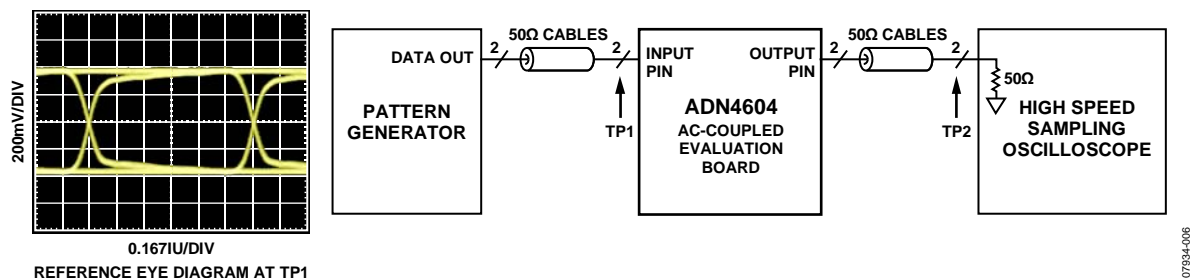


Figure 6. Standard Test Circuit

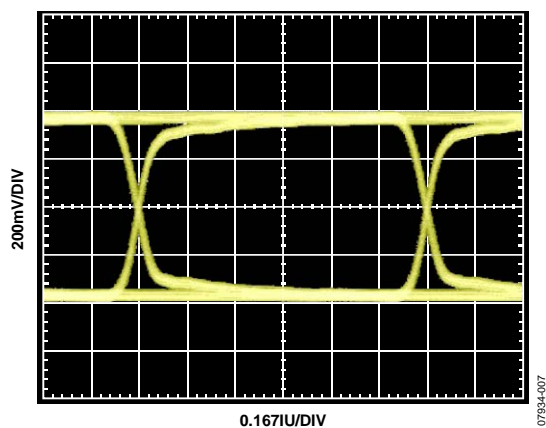


Figure 7. 3.25 Gbps Input Eye (TP1 from Figure 6)

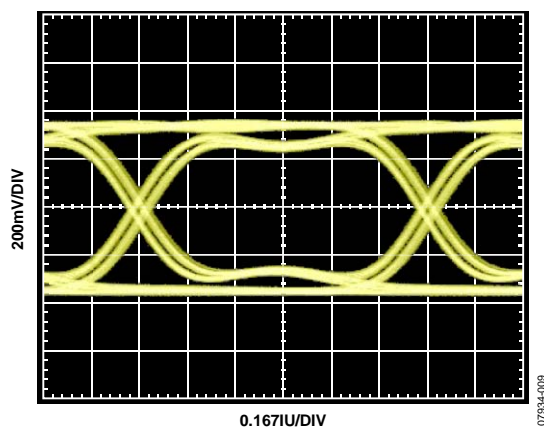


Figure 9. 3.25 Gbps Output Eye (TP2 from Figure 6)

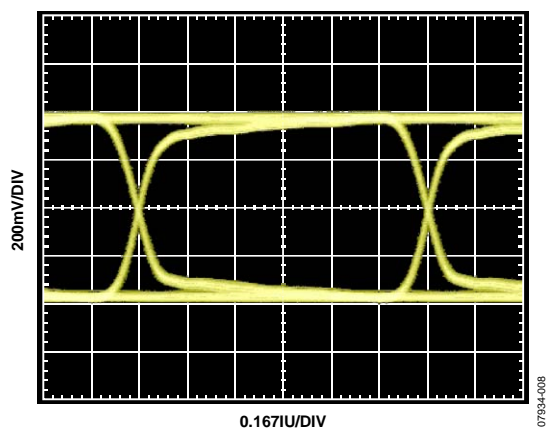


Figure 8. 4.25 Gbps Input Eye (TP1 from Figure 6)

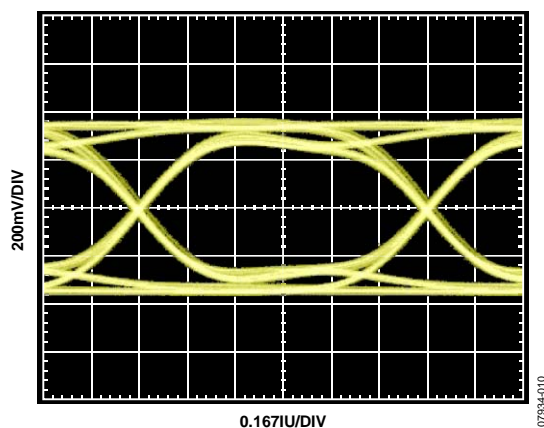


Figure 10. 4.25 Gbps Output Eye (TP2 from Figure 6)

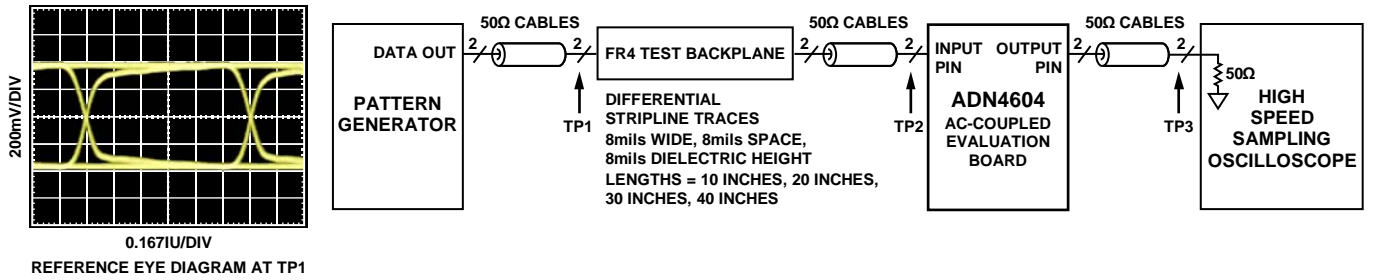


Figure 11. Equalization Test Circuit

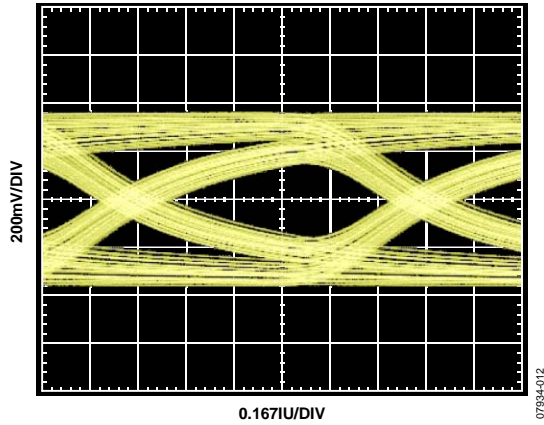


Figure 12. 4.25 Gbps Input Eye, 20-Inch FR4 Input Channel (TP2 from Figure 11)

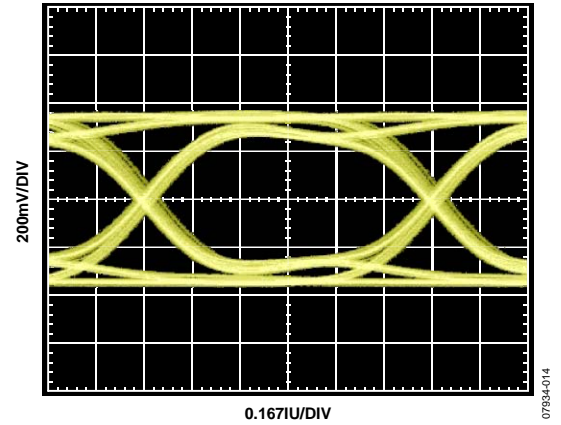


Figure 14. 4.25 Gbps Output Eye, 20-Inch FR4 Input Channel, EQ = 12 dB (TP3 from Figure 11)

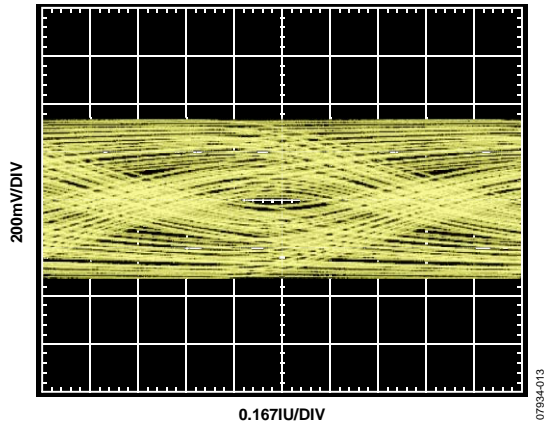


Figure 13. 4.25 Gbps Input Eye, 40-Inch FR4 Input Channel (TP2 from Figure 11)

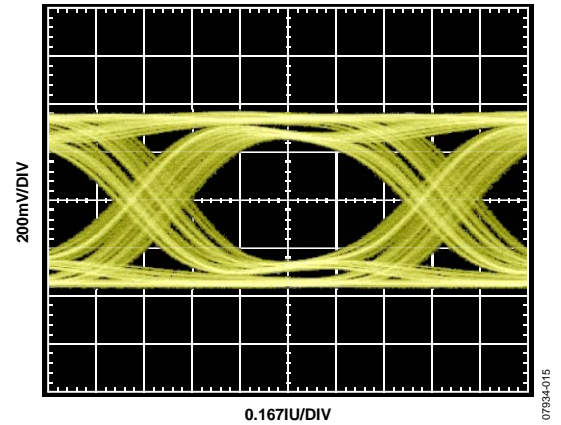
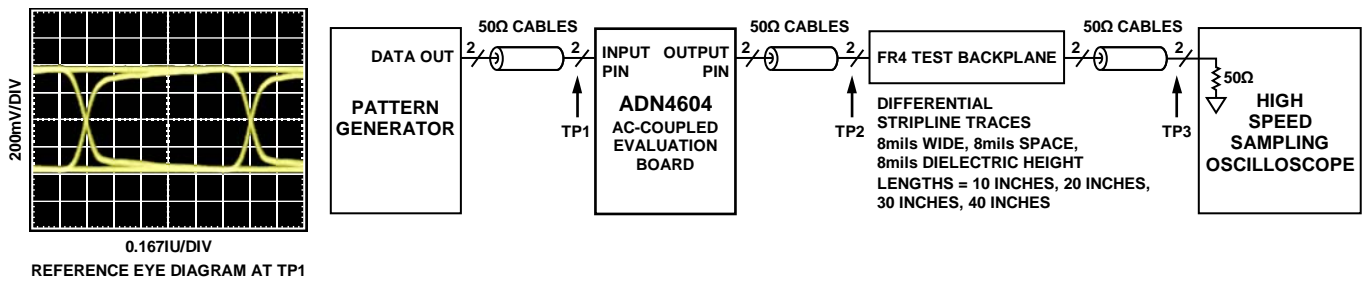


Figure 15. 4.25 Gbps Output Eye, 40-Inch FR4 Input Channel, EQ = 12 dB (TP3 from Figure 11)

ADN4604



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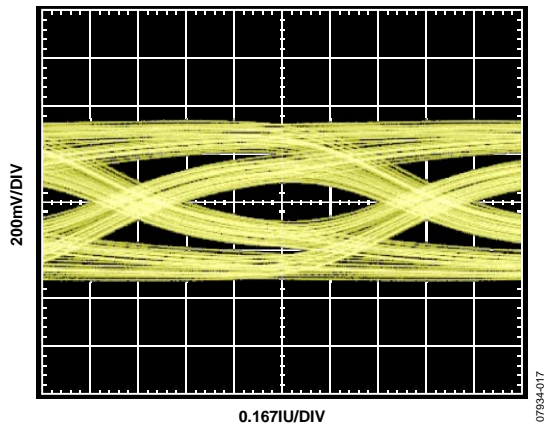


Figure 17. 4.25 Gbps Output Eye, 20-Inch FR4 Output Channel, PE = 0 dB (TP3 from Figure 16)

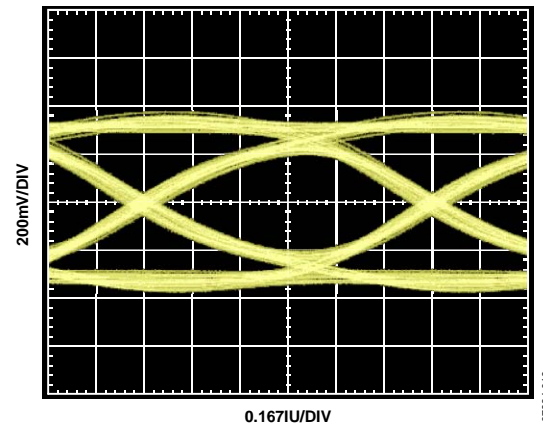


Figure 19. 4.25 Gbps Output Eye, 20-Inch FR4 Input Channel, PE = 4.2 dB (TP3 from Figure 16)

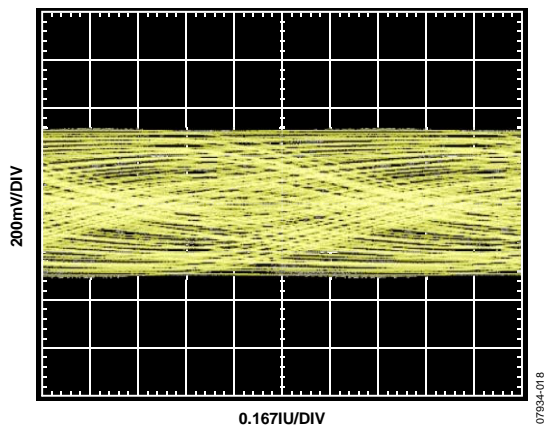


Figure 18. 4.25 Gbps Output Eye, 40-Inch FR4 Input Channel, PE = 0 dB (TP3 from Figure 16)

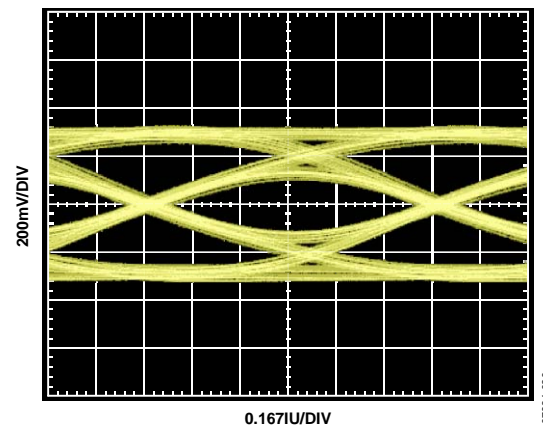


Figure 20. 4.25 Gbps Output Eye, 40-Inch FR4 Input Channel, PE = 6 dB (TP3 from Figure 16)

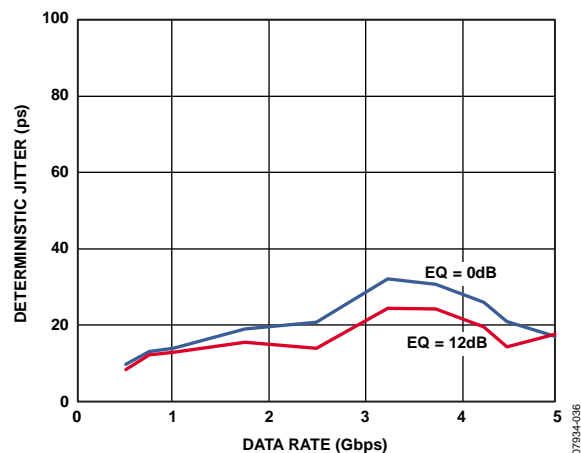


Figure 21. Deterministic Jitter vs. Data Rate

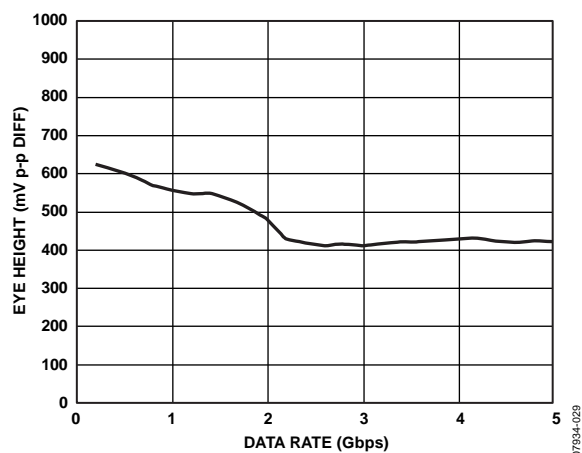


Figure 24. Eye Height vs. Data Rate

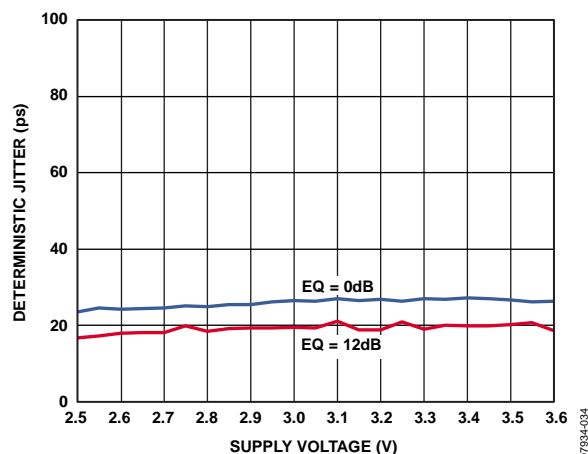


Figure 22. Deterministic Jitter vs. Supply Voltage

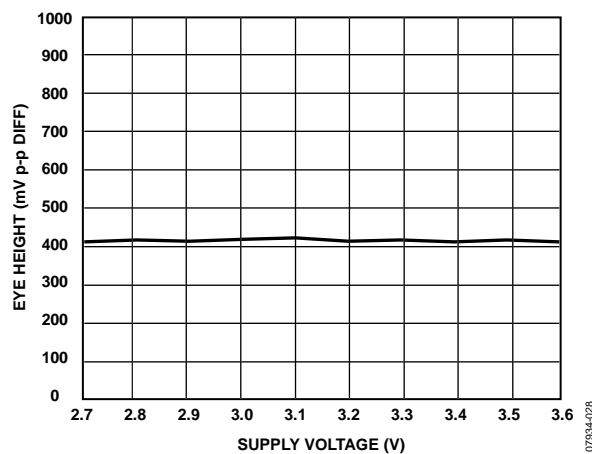


Figure 25. Eye Height vs. Supply Voltage

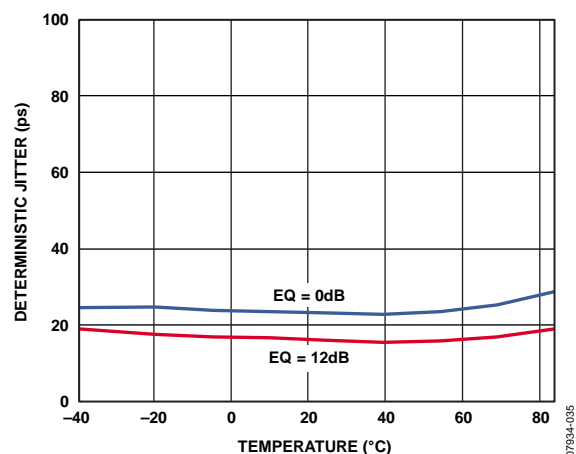


Figure 23. Deterministic Jitter vs. Temperature

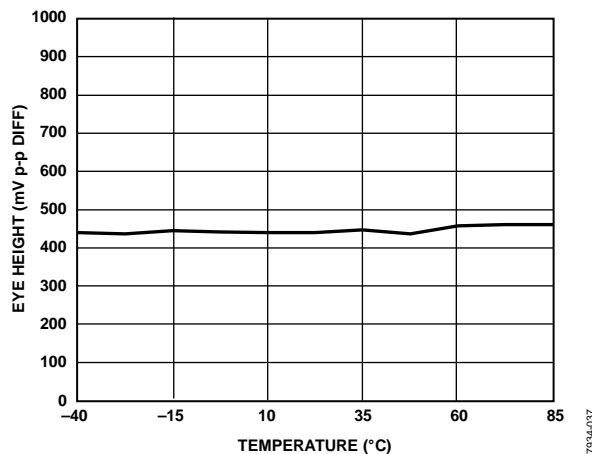


Figure 26. Eye Height vs. Temperature

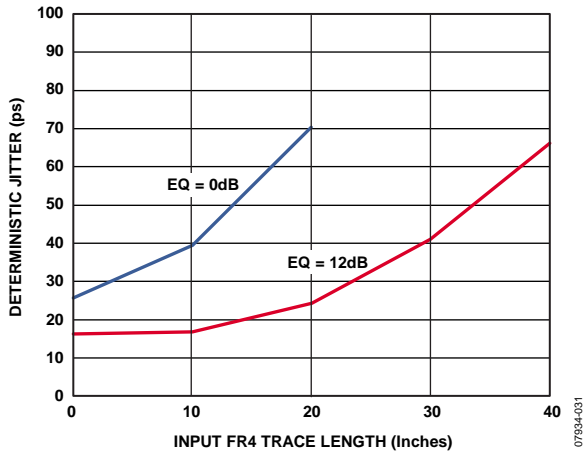


Figure 27. Deterministic Jitter vs. Input FR4 Channel Length

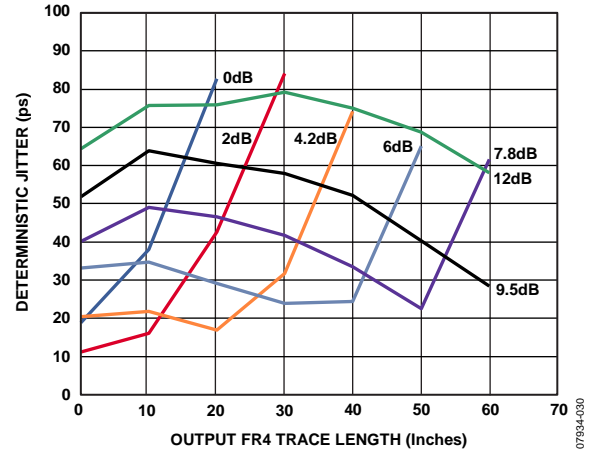


Figure 30. Deterministic Jitter vs. Output FR4 Channel Length

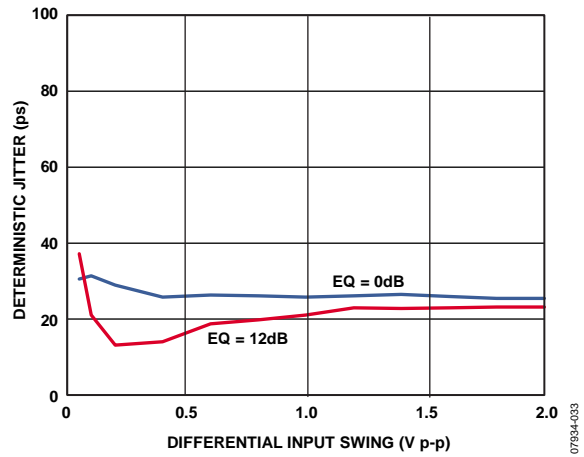


Figure 28. Deterministic Jitter vs. Differential Input Swing

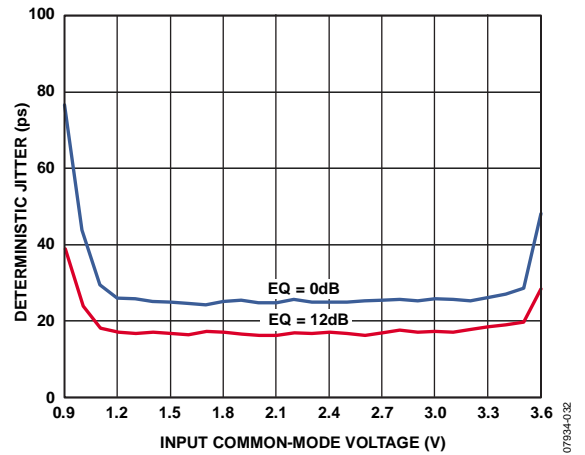


Figure 31. Deterministic Jitter vs. Input Common-Mode Voltage

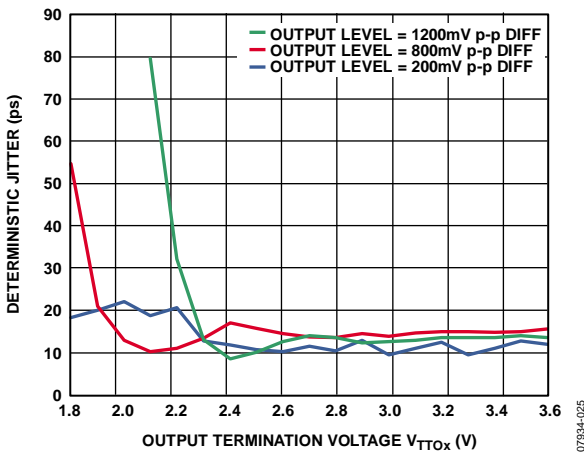


Figure 29. Deterministic Jitter vs. Output Termination Voltage (V_{TT0})

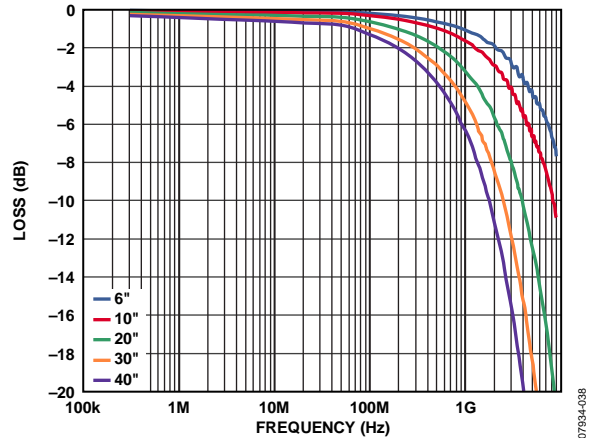


Figure 32. S21 Test Traces

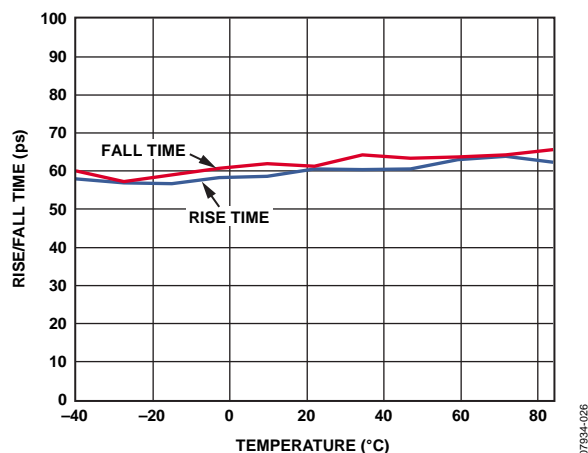


Figure 33. Rise/Fall Time vs. Temperature

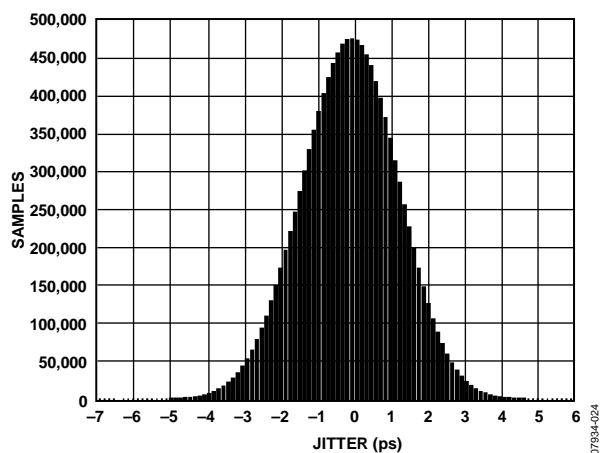


Figure 36. Random Jitter Histogram

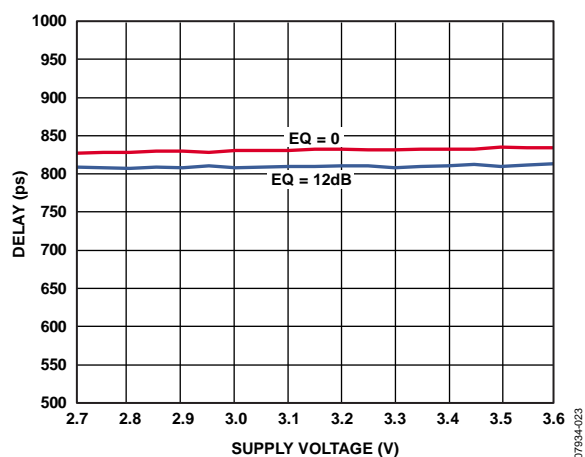


Figure 34. Propagation Delay vs. Supply Voltage

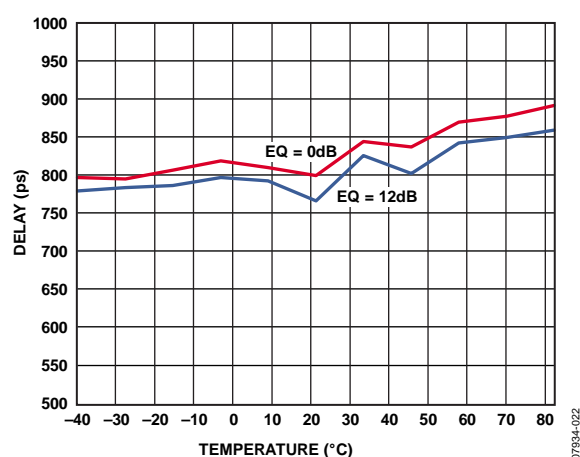


Figure 37. Propagation Delay vs. Temperature

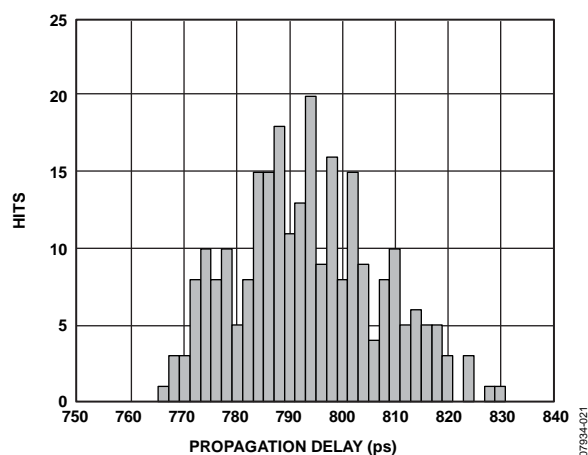


Figure 35. Propagation Delay Histogram

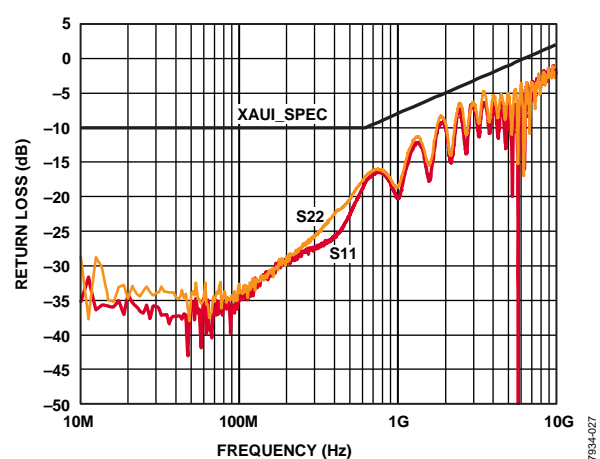


Figure 38. Return Loss (S11, S22)

THEORY OF OPERATION

INTRODUCTION

The ADN4604 is a 16 × 16, buffered, asynchronous crosspoint switch that provides input equalization, output preemphasis, and output level programming capabilities. The receivers integrate an equalizer that is optimized to compensate for typical backplane losses. The switch supports multicast and broadcast operation, allowing the ADN4604 to work in redundancy and port-replication applications. The part offers extensively programmable output levels and preemphasis settings.

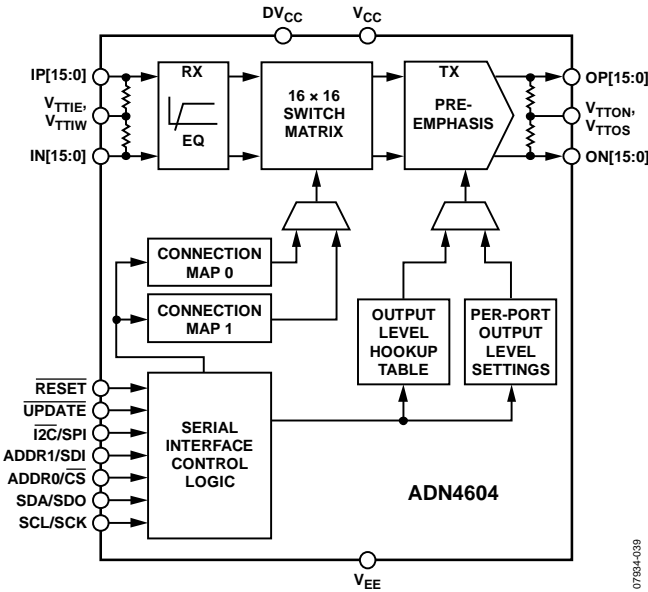


Figure 39. Block Diagram

The configuration of the crosspoint is controlled through a serial interface. This interface supports both I²C and SPI protocols, which can be selected using the I²C/SPI dedicated control pin. There are two I²C address pins available as described in Table 6.

Table 6. Serial Interface Control Modes

| Pin No. | I2C/SPI = 0 | | I2C/SPI = 1 | |
|---------|-------------|------------------------------|------------------------|-----------------|
| | Pin Name | Pin Function | Pin Name | Pin Function |
| 50 | ADDR1 | I ² C Address MSB | SDI | SPI Data Input |
| 51 | ADDR0 | I ² C Address LSB | $\overline{\text{CS}}$ | SPI Chip Select |
| 75 | SDA | I ² C Data | SDO | SPI Data Output |
| 76 | SCL | I ² C Clock | SCK | SPI Clock |

RECEIVERS

Input Structure and Input Levels

The ADN4604 receiver inputs incorporate 50 Ω termination resistors, ESD protection, and a fixed equalizer that is optimized for operation over long backplane traces. Each receive channel also provides a positive/negative (P/N) inversion function, which allows the user to swap the sign of the input signal path to eliminate the need for board-level crossovers in the receiver channel.

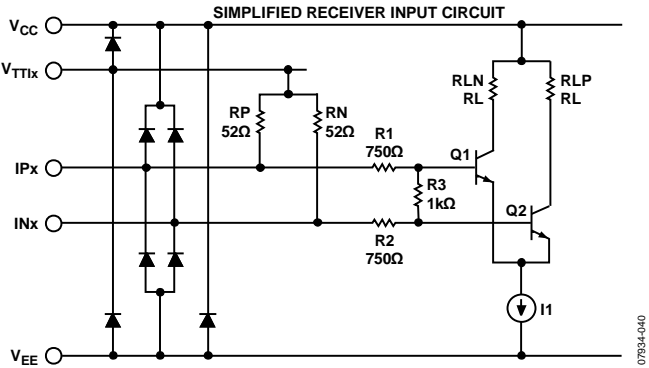


Figure 40. Simplified Input Circuit

Equalization

The ADN4604 receiver incorporates a continuous time equalizer (EQ) that provides 12 dB of high frequency boost to compensate up to 40 inches of FR4 at 4.25 Gbps. Each input has an equalizer control bit. By default, the programmable boost is set to 12 dB. The boost can be set to 0 dB by programming a Logic 0 to the respective register bit for the corresponding channel.

Table 7. Equalization Control Registers

| EQ[15:0] | Equalization Boost |
|----------|--------------------|
| 0 | 0 dB |
| 1 | 12 dB (default) |

Lane Inversion

The receiver P/N inversion is a feature intended to allow the user to implement the equivalent of a board-level crossover in a much smaller area and without additional via impedance discontinuities that degrade the high frequency integrity of the signal path. The P/N inversion is available independently for each of the 16 input channels and is controlled by writing to the SIGN bit of the RX control registers (Addresses 0x12 and Address 0x13). Note that using this feature to account for signal inversions downstream of the receiver requires additional attention when switching connectivity.

Table 8. Signal Path Polarity Control

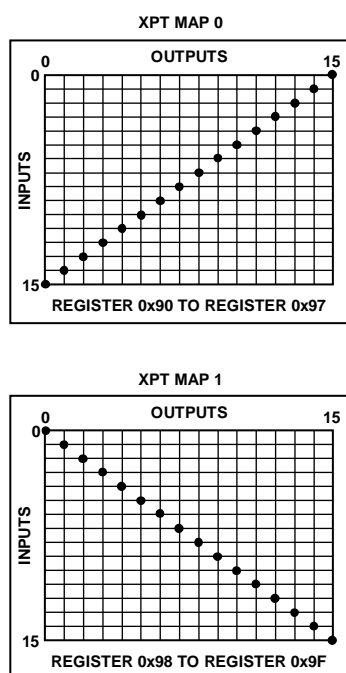
| SIGN[15:0] | Signal Path Polarity |
|------------|------------------------|
| 0 | Noninverting (default) |
| 1 | Inverting |

SWITCH CORE

The ADN4604 switch core is a fully nonblocking 16×16 array that allows multicast and broadcast configurations. The configuration of the switch core is programmed through the serial control interface. The crosspoint configuration map controls the connectivity of the switch core. The crosspoint configuration map consists of a double-rank register architecture where each rank consists of an 8-byte configuration map as shown in Figure 41. The second rank registers contain the current state of the crosspoint. The first rank registers contain the next state. Each entry in the connection map stores four bits per output, which indicates which of the 16 inputs are connected to a given output. An entire connectivity matrix can be programmed at once by passing data from the first rank registers into the second rank registers.

The first rank registers are two separate volatile 8-byte memory banks which store connection configurations for the crosspoint. Map 0 is the default map and is located at Address 0x90 to Address 0x97. By default, Map 0 contains a diagonal connection configuration whereby Input 15 is connected to Output 0, Input 14 to Output 1, Input 13 to Output 2, and so on. Similarly, by default, Map 1 contains the opposite diagonal connection configuration where Input 0 is connected to output 0, Input 1 to Output 1, and so on. Both maps are read/write accessible registers. The active map is selected by writing to the XPT table select register (Address 0x81).

FIRST RANK REGISTERS



SECOND RANK REGISTERS

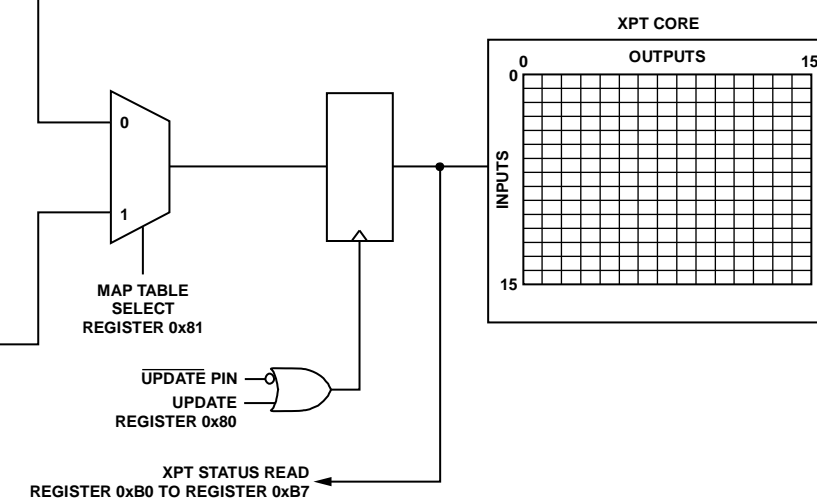


Figure 41. Crosspoint Connection Map Block Diagram

The crosspoint is configured by addressing the register assigned to the desired output and writing the desired connection data into the first rank of latches in either Map 0 or Map 1. The connection data is equivalent to the binary coded value of the input number. This process is repeated until each of the desired connections is programmed.

In situations where multiple outputs are to be programmed to a single input, a broadcast command is available. A broadcast command is issued by writing the binary value of the desired input to the XPT broadcast register (Address 0x82). The broadcast is applied to the selected map as selected in the map table select register (Address 0x81).

All output connections are updated simultaneously by passing the data from the first rank of latches into the second rank by writing 0x01 to the XPT update register (Address 0x80). This is a write-only register. Alternatively, the **UPDATE** pin can be strobed low. Otherwise, this pin should be left high.

The current state of the crosspoint connectivity is available by reading the XPT status registers (Address 0xB0 to Address 0xB7). Register descriptions for the Map 0, Map 1 and XPT status registers are provided in Table 9. A complete register map is provided in Table 18.

ADN4604

Table 9. XPT Control Registers

| Register Name | Address | Bit | Bit Name | Description | Default |
|---------------------|---------|-----|------------------|---|---------|
| Update | 0x80 | 0 | UPDATE | Updates XPT switch core (active high, write only) | N/A |
| Map Table Select | 0x81 | 0 | MAP TABLE SELECT | 0: Map 0 is selected 1: Map 1 is selected | 0x00 |
| XPT Broadcast | 0x82 | 3:0 | BROADCAST[3:0] | All outputs connection assignment, write only | N/A |
| XPT Map 0 Control 0 | 0x90 | 7:4 | OUT1[3:0] | Output 1 connection assignment | 0xEF |
| | | 3:0 | OUT0[3:0] | Output 0 connection assignment | |
| XPT Map 0 Control 1 | 0x91 | 7:4 | OUT3[3:0] | Output 3 connection assignment | 0xCD |
| | | 3:0 | OUT2[3:0] | Output 2 connection assignment | |
| XPT Map 0 Control 2 | 0x92 | 7:4 | OUT5[3:0] | Output 5 connection assignment | 0xAB |
| | | 3:0 | OUT4[3:0] | Output 4 connection assignment | |
| XPT Map 0 Control 3 | 0x93 | 7:4 | OUT7[3:0] | Output 7 connection assignment | 0x89 |
| | | 3:0 | OUT6[3:0] | Output 6 connection assignment | |
| XPT Map 0 Control 4 | 0x94 | 7:4 | OUT9[3:0] | Output 9 connection assignment | 0x67 |
| | | 3:0 | OUT8[3:0] | Output 8 connection assignment | |
| XPT Map 0 Control 5 | 0x95 | 7:4 | OUT11[3:0] | Output 11 connection assignment | 0x45 |
| | | 3:0 | OUT10[3:0] | Output 10 connection assignment | |
| XPT Map 0 Control 6 | 0x96 | 7:4 | OUT13[3:0] | Output 13 connection assignment | 0x23 |
| | | 3:0 | OUT12[3:0] | Output 12 connection assignment | |
| XPT Map 0 Control 7 | 0x97 | 7:4 | OUT15[3:0] | Output 15 connection assignment | 0x01 |
| | | 3:0 | OUT14[3:0] | Output 14 connection assignment | |
| XPT Map 1 Control 0 | 0x98 | 7:4 | OUT1[3:0] | Output 1 connection assignment | 0x10 |
| | | 3:0 | OUT0[3:0] | Output 0 connection assignment | |
| XPT Map 1 Control 1 | 0x99 | 7:4 | OUT3[3:0] | Output 3 connection assignment | 0x32 |
| | | 3:0 | OUT2[3:0] | Output 2 connection assignment | |
| XPT Map 1 Control 2 | 0x9A | 7:4 | OUT5[3:0] | Output 5 connection assignment | 0x54 |
| | | 3:0 | OUT4[3:0] | Output 4 connection assignment | |
| XPT Map 1 Control 3 | 0x9B | 7:4 | OUT7[3:0] | Output 7 connection assignment | 0x76 |
| | | 3:0 | OUT6[3:0] | Output 6 connection assignment | |
| XPT Map 1 Control 4 | 0x9C | 7:4 | OUT9[3:0] | Output 9 connection assignment | 0x98 |
| | | 3:0 | OUT8[3:0] | Output 8 connection assignment | |
| XPT Map 1 Control 5 | 0x9D | 7:4 | OUT11[3:0] | Output 11 connection assignment | 0xBA |
| | | 3:0 | OUT10[3:0] | Output 10 connection assignment | |
| XPT Map 1 Control 6 | 0x9E | 7:4 | OUT13[3:0] | Output 13 connection assignment | 0xDC |
| | | 3:0 | OUT12[3:0] | Output 12 connection assignment | |
| XPT Map 1 Control 7 | 0x9F | 7:4 | OUT15[3:0] | Output 15 connection assignment | 0xFE |
| | | 3:0 | OUT14[3:0] | Output 14 connection assignment | |
| XPT Status 0 | 0xB0 | 7:4 | OUT1[3:0] | Output 1 connection status, read only | 0xEF |
| | | 3:0 | OUT0[3:0] | Output 0 connection status, read only | |
| XPT Status 1 | 0xB1 | 7:4 | OUT3[3:0] | Output 3 connection status, read only | 0xCD |
| | | 3:0 | OUT2[3:0] | Output 2 connection status, read only | |
| XPT Status 2 | 0xB2 | 7:4 | OUT5[3:0] | Output 5 connection status, read only | 0xAB |
| | | 3:0 | OUT4[3:0] | Output 4 connection status, read only | |
| XPT Status 3 | 0xB3 | 7:4 | OUT7[3:0] | Output 7 connection status, read only | 0x89 |
| | | 3:0 | OUT6[3:0] | Output 6 connection status, read only | |
| XPT Status 4 | 0xB4 | 7:4 | OUT9[3:0] | Output 9 connection status, read only | 0x67 |
| | | 3:0 | OUT8[3:0] | Output 8 connection status, read only | |
| XPT Status 5 | 0xB5 | 7:4 | OUT11[3:0] | Output 11 connection status, read only | 0x45 |
| | | 3:0 | OUT10[3:0] | Output 10 connection status, read only | |
| XPT Status 6 | 0xB6 | 7:4 | OUT13[3:0] | Output 13 connection status, read only | 0x23 |
| | | 3:0 | OUT12[3:0] | Output 12 connection status, read only | |
| XPT Status 7 | 0xB7 | 7:4 | OUT15[3:0] | Output 15 connection status, read only | 0x01 |
| | | 3:0 | OUT14[3:0] | Output 14 connection status, read only | |

TRANSMITTERS

Output Structure and Output Levels

The ADN4604 transmitter outputs incorporate 50 Ω termination resistors, ESD protection, and output current switches. Each channel provides independent control of both the absolute output level and the preemphasis output level. Note that the choice of output level affects the output common-mode level.

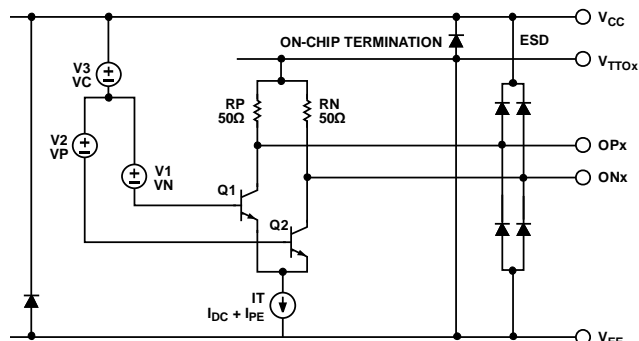


Figure 42. Simplified TX Output Circuit

Preemphasis

Transmission line attenuation can be equalized at the transmitter using preemphasis. The transmit equalizer setting can be chosen by matching the channel loss to the amount of boost provided by the preemphasis.

Basic Settings

In the basic mode of operation, predefined preemphasis settings are available through a lookup table. Each table entry requires two bytes of memory. The amount of preemphasis provided is independent of the full-scale current output. Transmitter preemphasis levels, as well as dc output levels, can be set through the serial control interface. The output level and amount of preemphasis can be independently programmed through advanced registers. By default, however, the total output amplitude and preemphasis setting space is reduced to a single table of basic settings that provides eight levels of output equalization to ease programming for typical FR4 channels.

Table 10 summarizes the absolute output level, preemphasis level, and high frequency boost for control setting. The full resolution of eight settings is available through the serial interface by writing to Bits[2:0] (the TX PE[2:0] bits) of the Basic TX Control registers shown in Table 11. A single setting is programmed to all outputs simultaneously by writing to the 0x18 broadcast address.

The TX has four possible output enable states (disabled, standby, squelched, and enabled) controlled by the TX EN[1:0] bits as shown in Table 11. Disabled is the lowest power-down state. When squelched, the output voltage at both P and N outputs will be the common-mode voltage as defined by the output current settings. In standby, the output level of both P and N outputs will be pulled up to the termination supply (V_{TT0} or V_{TT0S}).

The TX CTL SELECT bit (Bit 6) in the TX[15:0] basic control register determines whether the preemphasis and output current controls for the channel of interest are selected from the predefined lookup table or directly from the TX[15:0] Drive Control[1:0] registers (per channel). Figure 43 is an illustration of the TX control circuit. Setting the TX CTL SELECT bit low (default setting) selects preemphasis control from the predefined, optimized lookup table (Address 0x60 to Address 0x6F).

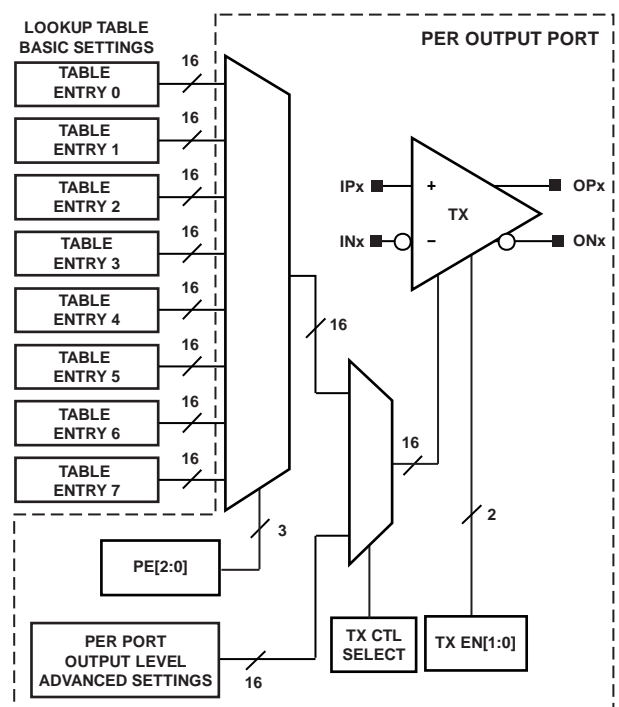


Figure 43. Transmitter Control Block Diagram

In applications where the default preemphasis settings in the lookup table are not sufficient, the lookup table entries can be modified by programming the TX lookup table registers (0x60 to 0x6F) shown in Table 12. In applications where the eight table entries are insufficient, each output can be programmed individually.

Table 10. Preemphasis Boost and Overshoot vs. Setting

| PE Setting | Main Tap Current (mA) | Delayed Tap Current (mA) | Boost (dB) | Overshoot (%) | DC Swing (mV p-p) |
|------------|-----------------------|--------------------------|------------|---------------|-------------------|
| 0 | 16 | 0 | 0.0 | 0 | 800 |
| 1 | 16 | 2 | 2.0 | 25 | 800 |
| 2 | 16 | 5 | 4.2 | 62.5 | 800 |
| 3 | 16 | 8 | 6.0 | 100 | 800 |
| 4 | 11 | 8 | 7.8 | 145 | 550 |
| 5 | 8 | 8 | 9.5 | 200 | 400 |
| 6 | 4 | 6 | 12.0 | 300 | 300 |
| 7 | 4 | 6 | 12.0 | 300 | 300 |

ADN4604

Table 11 displays the TX Basic Control register. The TX Basic Control register consists of one byte (8 bits) for each of the 16 output channels. Each TX Basic Control register has the same functionality. The mapping of register address to output channel is shown in the first column.

Table 11. TX Basic Control Register

| Address: Channel | Default | Register Name | Bit | Bit Name | Description |
|---|---------|------------------|----------------------------------|--|--|
| 0x18: Broadcast, 0x20: Output 0, 0x21: Output 1, 0x22: Output 2, 0x23: Output 3, 0x24: Output 4, 0x25: Output 5, 0x26: Output 6, 0x27: Output 7, 0x28: Output 8, 0x29: Output 9, 0x2A: Output 10, 0x2B: Output 11, 0x2C: Output 12, 0x2D: Output 13, 0x2E: Output 14, 0x2F: Output 15 | 0x00 | TX basic control | 6 5:4 3 2:0 | TX CTL SELECT TX EN[1:0] Reserved PE[2:0] | 0: PE and output level control is derived from common lookup table 1: PE and output level control is derived from per port drive control registers 00: TX disabled, lowest power state 01: TX standby. 10: TX squelched. 11: TX enabled Reserved. Set to 0. If TX CTL SELECT = 0, see Table 10 000: Table Entry 0 001: Table Entry 1 010: Table Entry 2 011: Table Entry 3 100: Table Entry 4 101: Table Entry 5 110: Table Entry 6 111: Table Entry 7 If TX CTL SELECT = 1, PE[2:0] are ignored |

Table 12 displays the TX lookup table register. The TX lookup table register consists of two bytes (16 bits) for each of the eight possible table entries selected by the PE[2:0] field in Table 11. The mapping of table entry to register address is shown in the first column. By default, the TX Lookup Table register contains the preemphasis settings listed in Table 10, however, these values can be changed for a flexible selection of output levels and preemphasis boosts. Table 13 lists a variety of possible output level and preemphasis boost settings and the corresponding TX Drive 0 and TX Drive 1 codes.

Table 12. TX Lookup Table Registers

| Address: Channel | Default | Register Name | Bit | Bit Name | Description |
|--|--|----------------------------|------------------------------|--|--|
| 0x60: Table Entry 0 0x62: Table Entry 1 0x64: Table Entry 2 0x66: Table Entry 3 0x68: Table Entry 4 0x6A: Table Entry 5 0x6C: Table Entry 6 0x6E: Table Entry 7 | 0xFF 0xFF 0xFF 0xFF 0xDC 0xBB 0x99 0x99 | TX Lookup Table Drive 0 | 7 6:4 3 2:0 | DRV EN1 DRV LV1[2:0] DRV EN0 DRV LV0[2:0] | 0: Driver 1 disabled 1: Driver 1 enabled Driver 1 current = decimal(DRV LV1[2:0]) + 1 0: Driver 0 disabled 1: Driver 0 enabled Driver 0 current = decimal(DRV LV0[2:0]) + 1 |
| 0x61: Table Entry 0 0x63: Table Entry 1 0x65: Table Entry 2 0x67: Table Entry 3 0x69: Table Entry 4 0x6B: Table Entry 5 0x6D: Table Entry 6 0x6F: Table Entry 7 | 0x00 0x99 0xCC 0xFF 0xFF 0xFF 0xDD 0xDD | TX Lookup Table Drive 1 | 7 6:4 3 2:0 | DRV END DRV LVD[2:0] DRV EN2 DRV LV2[2:0] | 0: Driver D disabled 1: Driver D enabled Driver D Current = decimal(DRV LVD[2:0]) + 1 0: Driver 2 disabled 1: Driver 2 enabled Driver 2 current = decimal(DRV LV2[2:0]) + 1 |

Advanced Settings

In addition to the basic settings provided in the TX basic control registers, advanced settings are available in TX Drive 0 Control and TX Drive 1 Control registers (Address 0x30 to Address 0x4F). The advanced settings are useful in applications where each output requires an individually programmed preemphasis or output level setting beyond what is available in the lookup table in basic mode. To enable these advanced settings, set the TX CTL SELECT bit in the TX basic control register to a logic high. Next, program the TX Drive 0 control and Drive 1 control registers (Address 0x30 to Address 0x4F) to the desired output level and boost values. A subset of possible settings is provided in Table 13. An expanded list of available settings is shown in Table 19 in the Applications Information section. These advanced settings can also be used to modify the TX lookup table settings (Address 0x60 to Address 0x6F). The advanced settings register map is shown in Table 15.

The preemphasis boost equation follows.

$$\text{Gain[dB]} = 20 \times \log_{10} \left(1 + \frac{V_{SW-PE} - V_{SW-DC}}{V_{SW-DC}} \right) \quad (1)$$

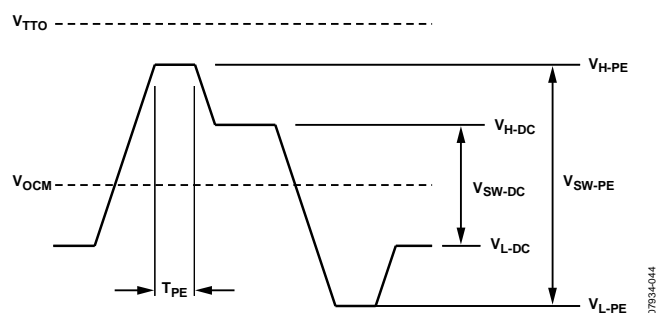


Figure 44. Signal Level Definitions

Table 13. TX Preemphasis and Output Swing Advanced Settings

| Single-Ended Output Levels and PE Boost | | | | Register Settings | | Output Current |
|---|--------------------------------------|------------|---------|-------------------|------------|------------------------------------|
| V _{SW-DC} ¹ (mV) | V _{SW-PE} ¹ (mV) | PE Boost % | PE (dB) | TX Drive 0 | TX Drive 1 | I _{TTO} ¹ (mA) |
| 200 | 200 | 0.00 | 0.00 | 0xBB | 0x00 | 8 |
| 200 | 300 | 50.00 | 3.52 | 0xBB | 0x99 | 12 |
| 200 | 350 | 75.00 | 4.86 | 0xBB | 0xAA | 14 |
| 200 | 400 | 100.00 | 6.02 | 0xBB | 0xBB | 16 |
| 200 | 450 | 125.00 | 7.04 | 0xBB | 0xCC | 18 |
| 200 | 500 | 150.00 | 7.96 | 0xBB | 0xDD | 20 |
| 200 | 600 | 200.00 | 9.54 | 0xBB | 0xFF | 24 |
| 300 | 300 | 0.00 | 0.00 | 0xDD | 0x00 | 12 |
| 300 | 400 | 33.33 | 2.50 | 0xDD | 0x99 | 16 |
| 300 | 450 | 50.00 | 3.52 | 0xDD | 0xAA | 18 |
| 300 | 500 | 66.67 | 4.44 | 0xDD | 0xBB | 20 |
| 300 | 550 | 83.33 | 5.26 | 0xDD | 0xCC | 22 |
| 300 | 600 | 100.00 | 6.02 | 0xDD | 0xDD | 24 |
| 300 | 700 | 133.33 | 7.36 | 0xDD | 0xFF | 28 |
| 400 | 400 | 0.00 | 0.00 | 0xFF | 0x00 | 16 |
| 400 | 500 | 25.00 | 1.94 | 0xFF | 0x99 | 20 |
| 400 | 550 | 37.50 | 2.77 | 0xFF | 0xAA | 22 |
| 400 | 600 | 50.00 | 3.52 | 0xFF | 0xBB | 24 |
| 400 | 650 | 62.50 | 4.22 | 0xFF | 0xCC | 26 |
| 400 | 700 | 75.00 | 4.86 | 0xFF | 0xDD | 28 |
| 400 | 800 | 100.00 | 6.02 | 0xFF | 0xFF | 32 |
| 500 | 500 | 0.00 | 0.00 | 0xFF | 0x0B | 20 |
| 600 | 600 | 0.00 | 0.00 | 0xFF | 0x0F | 24 |

¹ Symbol definitions are shown in Table 14.

Table 14. Symbol Definitions

| Symbol | Formula | Definition |
|------------------------------|---|---|
| I _{DC} | Programmable | Output current that sets output level |
| I _{PE} | Programmable | Output current for PE delayed tap |
| I _{TTO} | I _{DC} + I _{PE} | Total transmitter output current |
| T _{PE} | | Preemphasis pulse width |
| V _{DPP-DC} | 25 Ω × I _{DC} × 2 | Peak-to-peak differential voltage swing of non-preemphasized waveform |
| V _{DPP-PE} | 25 Ω × I _{TTO} × 2 | Peak-to-peak differential voltage swing of preemphasized waveform |
| V _{SW-DC} | V _{DPP-DC} /2 = V _{H-DC} - V _{L-DC} | DC single-ended voltage swing |
| V _{SW-PE} | V _{DPP-PE} /2 = V _{H-PE} - V _{L-PE} | Preemphasized single-ended voltage swing |
| ΔV _{OCM_DC-COUPLED} | 25 Ω × I _{TTO} /2 | Output common-mode shift, dc-coupled outputs |
| ΔV _{OCM_AC-COUPLED} | 50 Ω × I _{TTO} /2 | Output common-mode shift, ac-coupled outputs |
| V _{OCM} | V _{TTO} - ΔV _{OCM} = (V _{H-DC} + V _{L-DC})/2 | Output common-mode voltage |
| V _{H-DC} | V _{TTO} - ΔV _{OCM} + V _{DPP-DC} /2 | DC single-ended output high voltage |
| V _{L-DC} | V _{TTO} - ΔV _{OCM} - V _{DPP-DC} /2 | DC single-ended output low voltage |
| V _{H-PE} | V _{TTO} - ΔV _{OCM} + V _{DPP-PE} /2 | Maximum single-ended output voltage |
| V _{L-PE} | V _{TTO} - ΔV _{OCM} - V _{DPP-PE} /2 | Minimum single-ended output voltage |
| V _{TTO} | | Output termination voltage |

ADN4604

Table 15 displays the TX advanced control registers. The TX advanced control registers consist of two bytes (16 bits) for each of the 16 output channels. The mapping of register address to output channel is shown in the first column. The TX advanced control registers provides ultimate flexibility of per port output level and preemphasis boost. Table 13 lists a variety of possible output levels and preemphasis boost settings and the corresponding TX Drive 0 and TX Drive 1 codes.

Table 15. TX Advanced Control Registers

| Address: Channel | Default | Register Name | Bit | Bit Name | Description |
|---|---------|--------------------|------------------------------|--|--|
| 0x30: Output 0, 0x32: Output 1, 0x34: Output 2, 0x36: Output 3, 0x38: Output 4, 0x3A: Output 5, 0x3C: Output 6, 0x3E: Output 7, 0x40: Output 8, 0x42: Output 9, 0x44: Output 10, 0x46: Output 11, 0x48: Output 12, 0x4A: Output 13, 0x4C: Output 14, 0x4E: Output 15 | 0xFF | TX Drive 0 control | 7 6:4 3 2:0 | DRV EN1 DRV LV1[2:0] DRV EN0 DRV LV0[2:0] | 0: Driver 1 disabled 1: Driver 1 enabled Driver 1 current = decimal(DRV LV1[2:0]) + 1 0: Driver 0 disabled 1: Driver 0 enabled Driver 0 current = decimal(DRV LV0[2:0]) + 1 |
| 0x31: Output 0, 0x33: Output 1, 0x35: Output 2, 0x37: Output 3, 0x39: Output 4, 0x3B: Output 5, 0x3D: Output 6, 0x3F: Output 7, 0x41: Output 8, 0x43: Output 9, 0x45: Output 10, 0x47: Output 11, 0x49: Output 12, 0x4B: Output 13, 0x4D: Output 14, 0x4F: Output 15 | 0x00 | TX Drive 1 control | 7 6:4 3 2:0 | DRV END DRV LVD[2:0] DRV EN2 DRV LV2[2:0] | 0: Driver D disabled 1: Driver D enabled Driver D current = decimal(DRV LVD[2:0]) + 1 0: Driver 2 disabled 1: Driver 2 enabled Driver 2 current = decimal(DRV LV2[2:0]) + 1 |

I²C SERIAL CONTROL INTERFACE

The ADN4604 register set is controlled through a 2-wire I²C interface. The ADN4604 acts only as an I²C slave device. Therefore, the I²C bus in the system needs to include an I²C master to configure the ADN4604 and other I²C devices that may be on the bus.

The ADN4604 I²C interface can be run in the standard (100 kHz) and fast (400 kHz) modes. The SDA line only changes value when the SCL pin is low with two exceptions. To indicate the beginning or continuation of a transfer, the SDA pin is driven low while the SCL pin is high; to indicate the end of a transfer, the SDA line is driven high while the SCL line is high. Therefore, it is important to control the SCL clock to toggle only when the SDA line is stable unless indicating a start, repeated start, or stop condition.

Table 17. I²C Device Address Assignment

| ADDR1 Pin | ADDR0 Pin | I ² C Device Address |
|-----------|-----------|---------------------------------|
| 0 | 0 | 0x90 |
| 0 | 1 | 0x92 |
| 1 | 0 | 0x94 |
| 1 | 1 | 0x96 |

RESET

On initial power-up, or at any point in operation, the ADN4604 register set can be restored to the default values by pulling the **RESET** pin to low according to the specification in Table 2. During normal operation, however, the **RESET** pin must be pulled up to DV_{CC}. A software reset is available by writing the value 0x01 to the Reset register at Address 0x00. This register is write only.

I²C DATA WRITE

To write data to the ADN4604 register set, a microcontroller, or any other I²C master, must send the appropriate control signals to the ADN4604 slave device. The steps to be followed are listed below; the signals are controlled by the I²C master, unless otherwise specified. A diagram of the procedure is shown in Figure 46.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the ADN4604 part address (seven bits) whose upper four bits are the static value b10010 and whose lower three bits are controlled by the input pins I2C_A[1:0]. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the ADN4604 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the ADN4604 to acknowledge the request.
7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the ADN4604 to acknowledge the request.
9. Do one or more of the following:
 - a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.
 - b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the write procedure to perform a write.
 - c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
 - d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of the read procedure (in the I2C Data Read section) to perform a read from the same address set in Step 5.

The ADN4604 write process is shown in Figure 46. The SCL signal is shown along with a general write operation and a specific example. In the example, data 0x92 is written to Address 0x6D of an ADN4604 part with a part address of 0x4B. It is important to note that the SDA line only changes when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, Step 1 and Step 9 in this case.

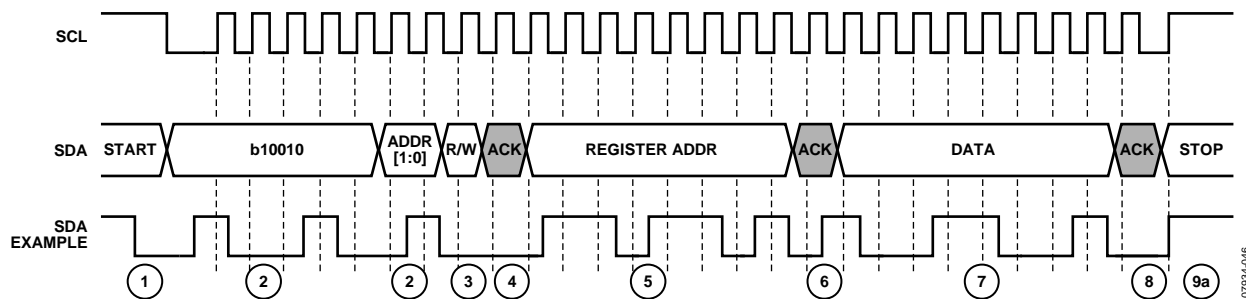


Figure 46. I²C Write Diagram

I²C DATA READ

To read data from the ADN4604 register set, a microcontroller, or any other I²C master must send the appropriate control signals to the ADN4604 slave device. The steps are listed below; the signals are controlled by the I²C master, unless otherwise specified. A diagram of the procedure is shown in Figure 47.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the ADN4604 part address (seven bits) whose upper five bits are the static value b10010 and whose lower two bits are controlled by the input pins ADDR1 and ADDR0. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the ADN4604 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first. The register address is kept in memory in the ADN4604 until the part is reset or the register address is written over with the same procedure (Step 1 to Step 6).
6. Wait for the ADN4604 to acknowledge the request.
7. Send a repeated start condition (while holding the SCL line high, pull the SDA line low).
8. Send the ADN4604 part address (seven bits) whose upper five bits are the static value b10010 and whose lower two bits are controlled by the input pins ADDR1 and ADDR0. This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the ADN4604 to acknowledge the request.
11. The ADN4604 then serially transfers the data (eight bits) held in the register indicated by the address set in Step 5.
12. Acknowledge the data.

13. Do one or more of the following:

- a. Send a stop condition (while holding the SCL line high pull the SDA line high) and release control of the bus.
- b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the write procedure (see the I²C Data Write section) to perform a write.
- c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
- d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

The ADN4604 read process is shown in Figure 47. The SCL signal is shown along with a general read operation and a specific example. In the example, Data 0x49 is read from Address 0x6D of an ADN4604 part with a part address of 0x4B. The part address is seven bits wide and is composed of the ADN4604 static upper five bits (b10010) and the pin program-mable lower two bits (ADDR1 and ADDR0). In this example, the ADDR1 and ADDR0 bits are set to b01. In Figure 47, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the ADN4604 slave. As for the SDA line, the data in the shaded polygons is driven by the ADN4604, whereas the data in the nonshaded polygons is driven by the I²C master. The end phase case shown is that of 13a.

Note that the SDA line only changes when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, as in Step 1, Step 7, and Step 13. In Figure 47, A is the same as ACK in Figure 46. Equally, Sr represents a repeated start where the SDA line is brought high before SCL is raised. SDA is then dropped while SCL is still high.

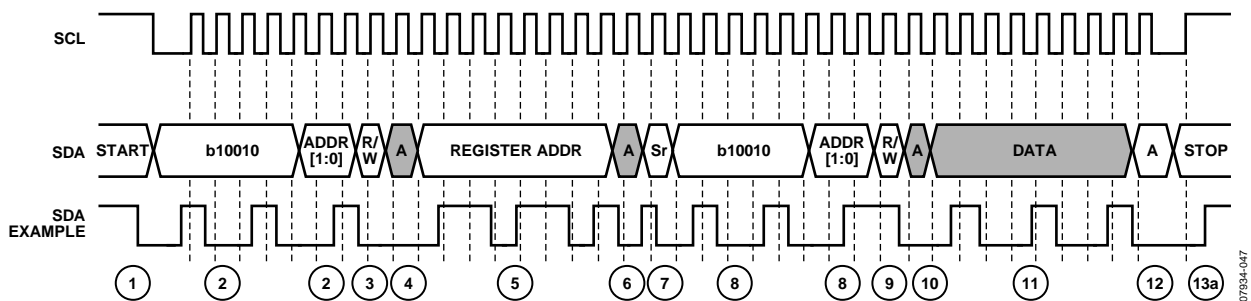


Figure 47. I²C Read Diagram

SPI SERIAL CONTROL INTERFACE

The SPI serial interface of the ADN4604 consists of four wires: \overline{CS} , SCK, SDI, and SDO. \overline{CS} is used to select the device when more than one device is connected to the serial clock and data lines. \overline{CS} is also used to distinguish between read and write commands (see Figure 48). SCK is used to clock data in and out of the part. Data can either contain eight bits of register address or data.

The SDI line is used to write to the registers, and the SDO line is used to read data back from the registers. Data on SDI is clocked on the rising edge of SCK. Data on SDO changes on the falling edge of SCK. The recommended pull-up resistor value is between 500 Ω and 1 k Ω . Strong pull-ups are needed when serial clock speeds that are close to the maximum limit are used or when the SPI interface lines are experiencing large capacitive loading. Larger resistor values can be used for pull-up resistors when the serial clock speed is reduced.

The part operates in slave mode and requires an externally applied serial clock to the SCLK input. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

Write Operation

Figure 48 shows the diagram for a write operation to the ADN4604. Data is clocked into the registers on the rising edge of SCK. When the \overline{CS} line is high, the SDI and SDO lines are in

three-state mode. Only when the \overline{CS} goes from high to low does the part accept any data on the SDI line. To allow continuous writes, the address pointer register auto-increments by one without having to load the address pointer register each time. Subsequent data bytes are written into sequential registers. Note that not all registers in the 256-byte address space exist and not all registers are writable. Zeroes should be entered for nonexisting address fields when implementing a continuous write operation. Address 0xD0 to Address 0xEF are reserved and should not be overwritten. A continuous write sequence is shown in Figure 49.

Read Operation

Figure 48 shows the diagram for a write operation to the ADN4604. To read back from a register, first write to the address pointer register with the desired starting address. A read command is distinguished from a write command by the occurrence of \overline{CS} going high after the address pointer is written. Subsequent clock cycles with \overline{CS} asserted low stream data starting from the desired register address onto SDO, MSB first. SDO changes on the falling edge of SCK.

Multiple data reads are possible in SPI interface mode as the address pointer register is auto-incremented. A continuous read sequence is shown in Figure 50.

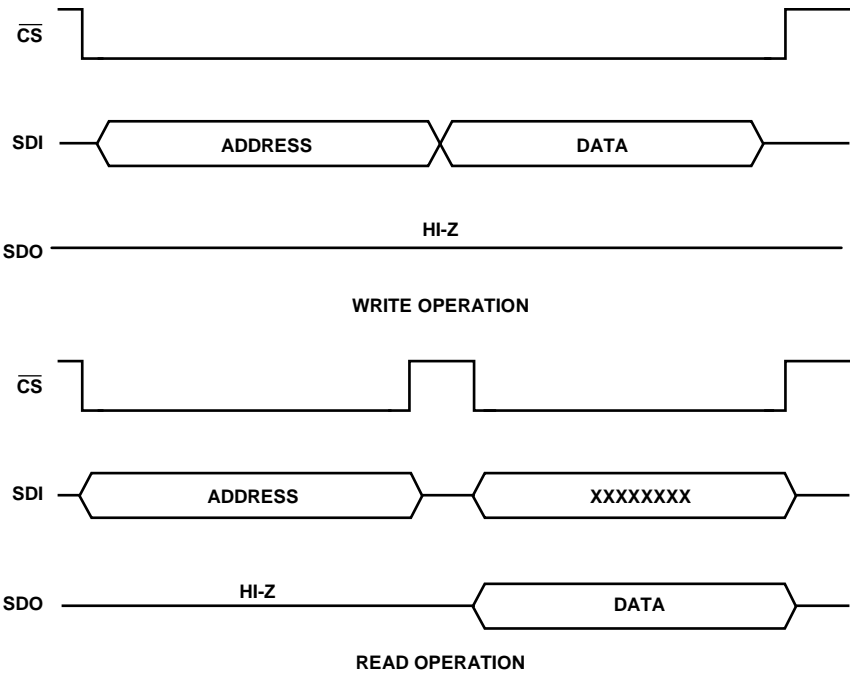


Figure 48. SPI—Correct Use of \overline{CS} During SPI Communications

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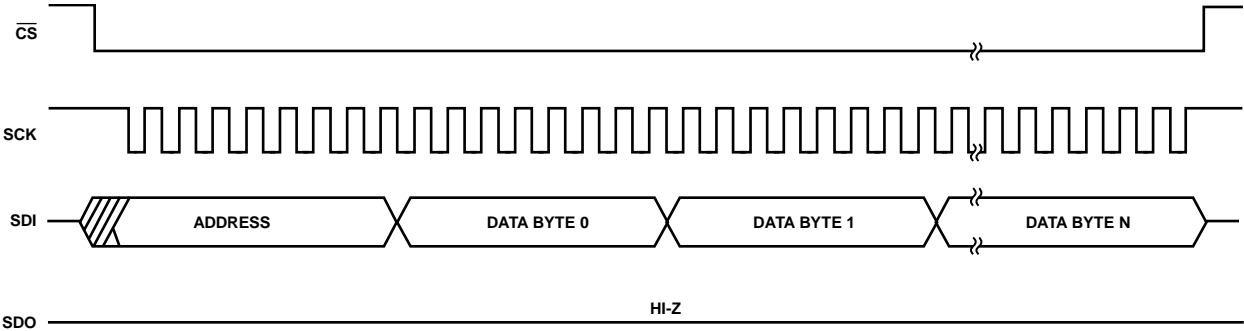


Figure 49. SPI Continuous Write Sequence

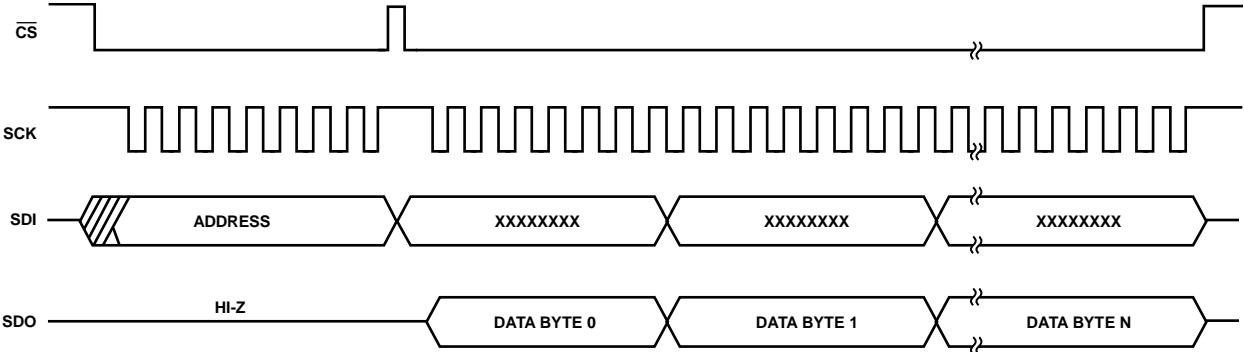


Figure 50. SPI Continuous Read Sequence

REGISTER MAP

Registers repeated per port or per table entry are grouped together. Register address mapping is shown in the first column.

Table 18. Register Map

| Address: Channel | Default | Register Name | Bit | Bit Name | Description |
|------------------|---------|-----------------|-----|----------|--|
| 0x00 | N/A | RESET | 0 | Reset | Software reset. Write only. |
| 0x10 | 0xFF | RX EQ Control 0 | 7 | EQ[7] | Equalizer boost control for input 7 0: 0 dB 1: 12 dB |
| | | | 6 | EQ[6] | Equalizer boost control for Input 6 |
| | | | 5 | EQ[5] | Equalizer boost control for Input 5 |
| | | | 4 | EQ[4] | Equalizer boost control for Input 4 |
| | | | 3 | EQ[3] | Equalizer boost control for Input 3 |
| | | | 2 | EQ[2] | Equalizer boost control for Input 2 |
| | | | 1 | EQ[1] | Equalizer boost control for Input 1 |
| | | | 0 | EQ[0] | Equalizer boost control for Input 0 |
| 0x11 | 0xFF | RX EQ Control 1 | 15 | EQ[15] | Equalizer boost control for Input 15 0: 0 dB 1: 12 dB |
| | | | 14 | EQ[14] | Equalizer boost control for Input 14 |
| | | | 13 | EQ[13] | Equalizer boost control for Input 13 |
| | | | 12 | EQ[12] | Equalizer boost control for Input 12 |
| | | | 11 | EQ[11] | Equalizer boost control for Input 11 |
| | | | 10 | EQ[10] | Equalizer boost control for Input 10 |
| | | | 9 | EQ[9] | Equalizer boost control for Input 9 |
| | | | 8 | EQ[8] | Equalizer boost control for Input 8 |
| 0x12 | 0x00 | RX Control 0 | 7 | SIGN[7] | Signal path polarity inversion for Input 7 0: Noninverting 1: Inverting |
| | | | 6 | SIGN[6] | Signal path polarity inversion for Input 6 |
| | | | 5 | SIGN[5] | Signal path polarity inversion for Input 5 |
| | | | 4 | SIGN[4] | Signal path polarity inversion for Input 4 |
| | | | 3 | SIGN[3] | Signal path polarity inversion for Input 3 |
| | | | 2 | SIGN[2] | Signal path polarity inversion for Input 2 |
| | | | 1 | SIGN[1] | Signal path polarity inversion for Input 1 |
| | | | 0 | SIGN[0] | Signal path polarity inversion for Input 0 |
| 0x13 | 0x00 | RX Control 1 | 15 | SIGN[15] | Signal path polarity inversion for Input 15 0: Noninverting 1: Inverting |
| | | | 14 | SIGN[14] | Signal path polarity inversion for Input 14 |
| | | | 13 | SIGN[13] | Signal path polarity inversion for Input 13 |
| | | | 12 | SIGN[12] | Signal path polarity inversion for Input 12 |
| | | | 11 | SIGN[11] | Signal path polarity inversion for Input 11 |
| | | | 10 | SIGN[10] | Signal path polarity inversion for Input 10 |
| | | | 9 | SIGN[9] | Signal path polarity inversion for Input 9 |
| | | | 8 | SIGN[8] | Signal path polarity inversion for Input 8 |

| Address: Channel | Default | Register Name | Bit | Bit Name | Description |
|---|--|--------------------|------------------------------|--|---|
| 0x18: Broadcast, 0x20: Output 0, 0x21: Output 1, 0x22: Output 2, 0x23: Output 3, 0x24: Output 4, 0x25: Output 5, 0x26: Output 6, 0x27: Output 7, 0x28: Output 8, 0x29: Output 9, 0x2A: Output 10, 0x2B: Output 11, 0x2C: Output 12, 0x2D: Output 13, 0x2E: Output 14, 0x2F: Output 15 | 0x00 | TX basic control | 6 5:4 3 2:0 | TX CTL SELECT TX EN[1:0] Reserved PE[2:0] | 0: PE and output level control is derived from common lookup table 1: PE and output level control is derived from per port drive control registers 00: TX disabled, lowest power state 01: TX standby 10: TX squelched 11: TX enabled Reserved. Set to 0. If TX CTL SELECT = 0, see Table 10 Selected table entry = decimal(PE[2:0]) If TX CTL SELECT = 1, PE[2:0] are ignored |
| 0x30: Output 0, 0x32: Output 1, 0x34: Output 2, 0x36: Output 3, 0x38: Output 4, 0x3A: Output 5, 0x3C: Output 6, 0x3E: Output 7, 0x40: Output 8, 0x42: Output 9, 0x44: Output 10, 0x46: Output 11, 0x48: Output 12, 0x4A: Output 13, 0x4C: Output 14, 0x4E: Output 15 | 0xFF | TX Drive 0 control | 7 6:4 3 2:0 | DRV EN1 DRV LV1[2:0] DRV EN0 DRV LV0[2:0] | 0: Driver 1 disabled 1: Driver 1 enabled Driver 1 current = decimal(DRV LV1[2:0]) + 1 0: Driver 0 disabled 1: Driver 0 enabled Driver 0 current = decimal(DRV LV0[2:0]) + 1 |
| 0x31: Output 0, 0x33: Output 1, 0x35: Output 2, 0x37: Output 3, 0x39: Output 4, 0x3B: Output 5, 0x3D: Output 6, 0x3F: Output 7, 0x41: Output 8, 0x43: Output 9, 0x45: Output 10, 0x47: Output 11, 0x49: Output 12, 0x4B: Output 13, 0x4D: Output 14, 0x4F: Output 15 | 0x00 | TX Drive 1 control | 7 6:4 3 2:0 | DRV END DRV LVD[2:0] DRV EN2 DRV LV2[2:0] | 0: Driver D disabled 1: Driver D enabled Driver D current = decimal(DRV LVD[2:0]) + 1 0: Driver 2 disabled 1: Driver 2 enabled Driver 2 current = decimal(DRV LV2[2:0]) + 1 |
| 0x60: Table Entry 0 0x62: Table Entry 1 0x64: Table Entry 2 0x66: Table Entry 3 0x68: Table Entry 4 0x6A: Table Entry 5 0x6C: Table Entry 6 0x6E: Table Entry 7 | 0xFF 0xFF 0xFF 0xFF 0xDC 0xBB 0x99 0x99 | TX Lookup Table 0 | 7 6:4 3 2:0 | DRV EN1 DRV LV1[2:0] DRV EN0 DRV LV0[2:0] | 0: Driver 1 disabled 1: Driver 1 enabled Driver 1 current = decimal(DRV LV1[2:0]) + 1 0: Driver 0 disabled 1: Driver 0 enabled Driver 0 current = decimal(DRV LV0[2:0]) + 1 |

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| Address: Channel | Default | Register Name | Bit | Bit Name | Description |
|---------------------|------------|---------------------|------------|--------------------------|--|
| 0x61: Table Entry 0 | 0x00 | TX Lookup Table 1 | 7 | DRV END | 0: Driver D disabled 1: Driver D enabled |
| 0x63: Table Entry 1 | 0x99 | | 6:4 | DRV LVD[2:0] | Driver D current = decimal(DRV LVD[2:0]) + 1 |
| 0x65: Table Entry 2 | 0xCC | | | | |
| 0x67: Table Entry 3 | 0xFF | | 3 | DRV EN2 | 0: Driver 2 disabled 1: Driver 2 enabled |
| 0x69: Table Entry 4 | 0xFF | | | | |
| 0x6B: Table Entry 5 | 0xFF | | 2:0 | DRV LV2[2:0] | Driver 2 current = decimal(DRV LV2[2:0]) + 1 |
| 0x6D: Table Entry 6 | 0xDD | | | | |
| 0x6F: Table Entry 7 | 0xDD | | | | |
| 0x80 | Write only | Update | 0 | UPDATE | Updates XPT switch core (active high, write only) |
| 0x81 | 0x00 | Map table select | 0 | MAP TABLE SELECT | 0: Map 0 is selected 1: Map 1 is selected |
| 0x82 | Write only | XPT broadcast | 3:0 | BROADCAST[3:0] | All outputs connection assignment |
| 0x90 | 0xEF | XPT Map 0 Control 0 | 7:4 3:0 | OUT1[3:0] OUT0[3:0] | Output 1 connection assignment Output 0 connection assignment |
| 0x91 | 0xCD | XPT Map 0 Control 1 | 7:4 3:0 | OUT3[3:0] OUT2[3:0] | Output 3 connection assignment Output 2 connection assignment |
| 0x92 | 0xAB | XPT Map 0 Control 2 | 7:4 3:0 | OUT5[3:0] OUT4[3:0] | Output 5 connection assignment Output 4 connection assignment |
| 0x93 | 0x89 | XPT Map 0 Control 3 | 7:4 3:0 | OUT7[3:0] OUT6[3:0] | Output 7 connection assignment Output 6 connection assignment |
| 0x94 | 0x67 | XPT Map 0 Control 4 | 7:4 3:0 | OUT9[3:0] OUT8[3:0] | Output 9 connection assignment Output 8 connection assignment |
| 0x95 | 0x45 | XPT Map 0 Control 5 | 7:4 3:0 | OUT11[3:0] OUT10[3:0] | Output 11 connection assignment Output 10 connection assignment |
| 0x96 | 0x23 | XPT Map 0 Control 6 | 7:4 3:0 | OUT13[3:0] OUT12[3:0] | Output 13 connection assignment Output 12 connection assignment |
| 0x97 | 0x01 | XPT Map 0 Control 7 | 7:4 3:0 | OUT15[3:0] OUT14[3:0] | Output 15 connection assignment Output 14 connection assignment |
| 0x98 | 0x10 | XPT Map 1 Control 0 | 7:4 3:0 | OUT1[3:0] OUT0[3:0] | Output 1 connection assignment Output 0 connection assignment |
| 0x99 | 0x32 | XPT Map 1 Control 1 | 7:4 3:0 | OUT3[3:0] OUT2[3:0] | Output 3 connection assignment Output 2 connection assignment |
| 0x9A | 0x54 | XPT Map 1 Control 2 | 7:4 3:0 | OUT5[3:0] OUT4[3:0] | Output 5 connection assignment Output 4 connection assignment |
| 0x9B | 0x76 | XPT Map 1 Control 3 | 7:4 3:0 | OUT7[3:0] OUT6[3:0] | Output 7 connection assignment Output 6 connection assignment |
| 0x9C | 0x98 | XPT Map 1 Control 4 | 7:4 3:0 | OUT9[3:0] OUT8[3:0] | Output 9 connection assignment Output 8 connection assignment |
| 0x9D | 0xBA | XPT Map 1 Control 5 | 7:4 3:0 | OUT11[3:0] OUT10[3:0] | Output 11 connection assignment Output 10 connection assignment |
| 0x9E | 0xDC | XPT Map 1 Control 6 | 7:4 3:0 | OUT13[3:0] OUT12[3:0] | Output 13 connection assignment Output 12 connection assignment |
| 0x9F | 0xFE | XPT Map 1 Control 7 | 7:4 3:0 | OUT15[3:0] OUT14[3:0] | Output 15 connection assignment Output 14 connection assignment |

| Address: Channel | Default | Register Name | Bit | Bit Name | Description |
|------------------|---------|---------------------|-----|------------|---|
| 0xB0 | 0xEF | XPT Status 0 | 7:4 | OUT1[3:0] | Output 1 connection status |
| | | | 3:0 | OUT0[3:0] | Output 0 connection status |
| 0xB1 | 0xCD | XPT Status 1 | 7:4 | OUT3[3:0] | Output 3 connection status |
| | | | 3:0 | OUT2[3:0] | Output 2 connection status |
| 0xB2 | 0xAB | XPT Status 2 | 7:4 | OUT5[3:0] | Output 5 connection status |
| | | | 3:0 | OUT4[3:0] | Output 4 connection status |
| 0xB3 | 0x89 | XPT Status 3 | 7:4 | OUT7[3:0] | Output 7 connection status |
| | | | 3:0 | OUT6[3:0] | Output 6 connection status |
| 0xB4 | 0x67 | XPT Status 4 | 7:4 | OUT9[3:0] | Output 9 connection status |
| | | | 3:0 | OUT8[3:0] | Output 8 connection status |
| 0xB5 | 0x45 | XPT Status 5 | 7:4 | OUT11[3:0] | Output 11 connection status |
| | | | 3:0 | OUT10[3:0] | Output 10 connection status |
| 0xB6 | 0x23 | XPT Status 6 | 7:4 | OUT13[3:0] | Output 13 connection status |
| | | | 3:0 | OUT12[3:0] | Output 12 connection status |
| 0xB7 | 0x01 | XPT Status 7 | 7:4 | OUT15[3:0] | Output 15 connection status |
| | | | 3:0 | OUT14[3:0] | Output 14 connection status |
| 0xF0 | 0x00 | Termination control | 3 | TXN_TERM | Output[15:8] (North) termination control 0: Terminations enabled 1: Terminations disabled |
| | | | 2 | TXS_TERM | Output[7:0] (South) termination control |
| | | | 1 | RXE_TERM | Input[15:8] (East) termination control |
| | | | 0 | RXW_TERM | Input[7:0] (West) termination control |
| 0xFE | | Revision | 7:0 | REV[7:0] | Read-only |
| 0xFF | 0x04 | Device ID | 7:0 | ID[7:0] | Read-only |

APPLICATIONS INFORMATION

The ADN4604 is an asynchronous and protocol agnostic digital switch and, therefore, is applicable to a wide range of applications including network routing and digital video switching. The ADN4604 supports the data rates and signaling levels of HDMI®, DVI®, DisplayPort and SD-, HD-, and 3G-SDI digital video. The ADN4604 can be used to create matrix switches. An example block diagram of a 16 × 16 matrix switch is shown in

Figure 51. Since HDMI, DVI, and DisplayPort are quad lane protocols, four ADN4604s are used to create a full 16 × 16 matrix switch. Smaller arrays, such as 4 × 4 and 8 × 8, require one and two ADN4604 devices, respectively. Proper high speed PCB design techniques should be used to maintain the signal integrity of the high data rate signals. It is important to minimize the lane-to-lane skew and crosstalk in these applications.

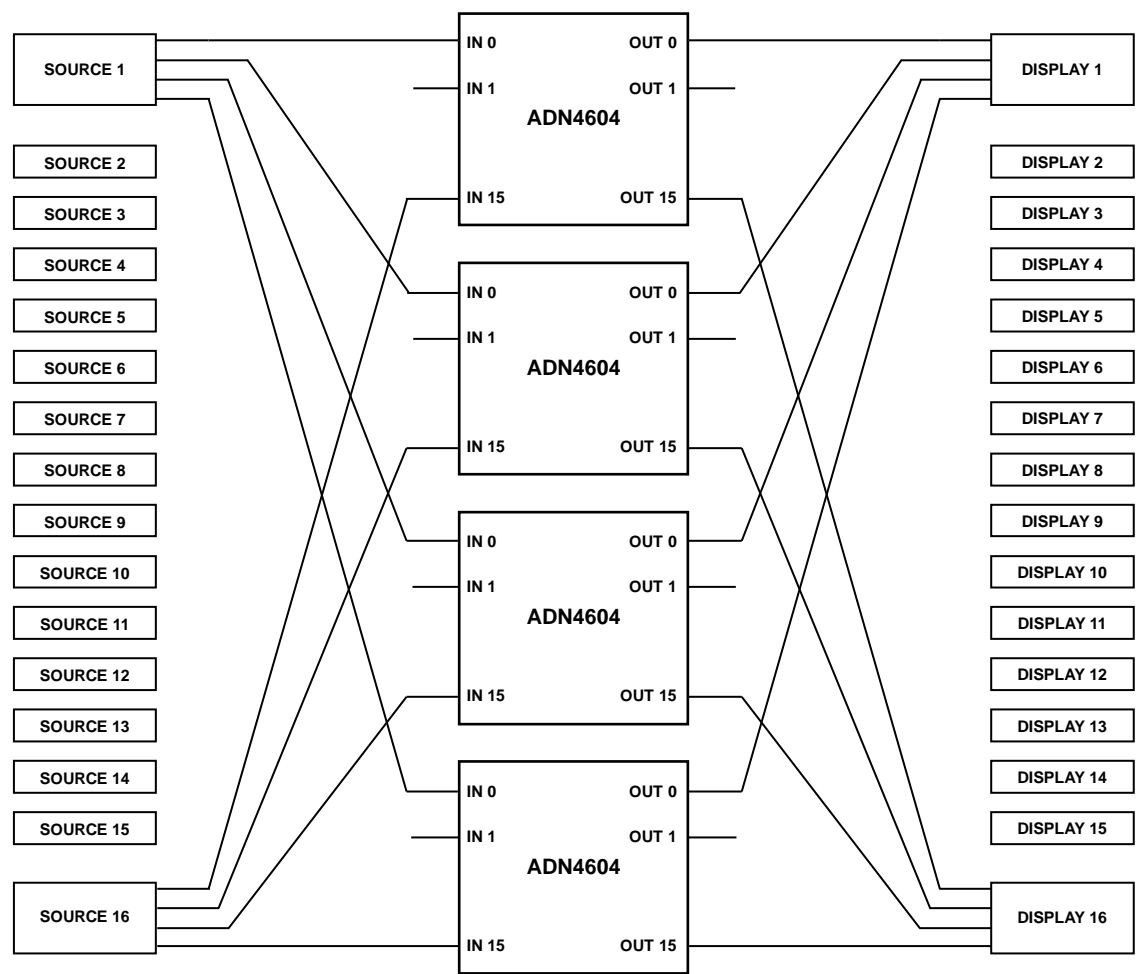


Figure 51. ADN4604 Digital Video (DVI, HDMI, DisplayPort) Matrix Switch Block Diagram

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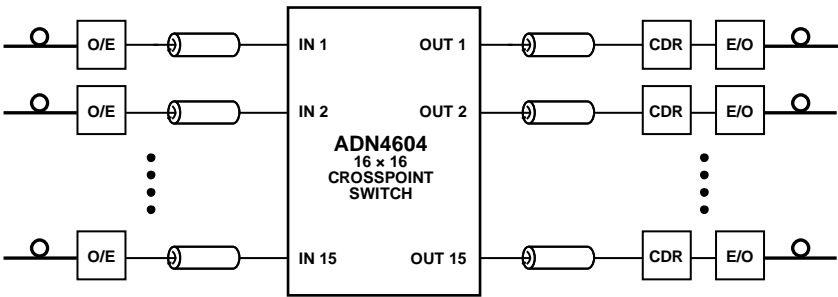


Figure 52. ADN4604 Networking Switch Application Block Diagram

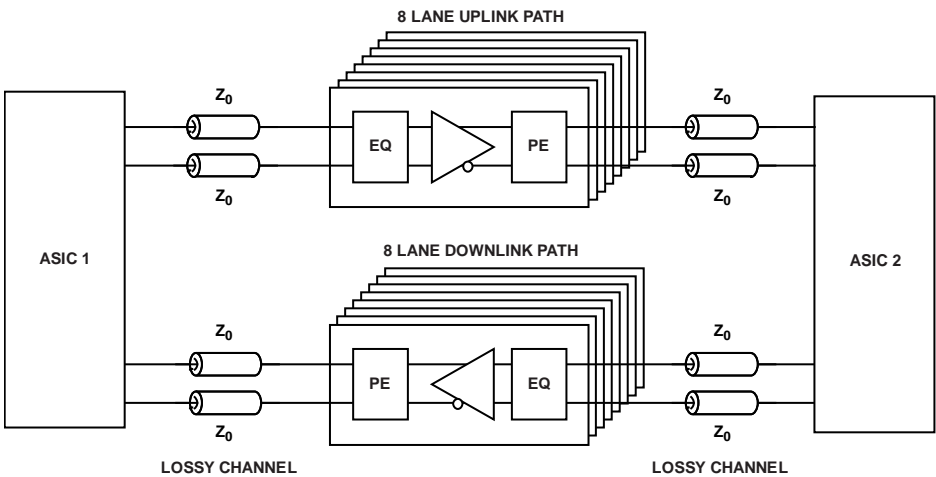


Figure 53. Multi-Lane Signal Conditioning Application Diagram

ADN4604

SUPPLY SEQUENCING

Ideally, all power supplies should be brought up to the appropriate levels simultaneously (power supply requirements are set by the supply limits in Table 1 and the absolute maximum ratings listed in Table 4). If the power supplies to the ADN4604 are brought up separately, the supply power-up sequence is as follows: DV_{CC} powered first, followed by V_{CC} , and, last the termination supplies (V_{TTIE} , V_{TTIW} , V_{TTON} , and V_{TTOS}). The power-down sequence is reversed with termination supplies being powered off first. The termination supplies contain ESD protection diodes to the V_{CC} power domain. To avoid a sustained high current condition in these devices ($I_{SUSTAINED} < 100$ mA), the V_{TTI} and V_{TTO} supplies should be powered on after V_{CC} and should be powered off before V_{CC} .

If the system power supplies have a high impedance in the powered off state, then supply sequencing is not required provided the following limits are observed:

- Peak current from V_{TTIx} or V_{TTOx} to $V_{CC} < 200$ mA
- Sustained current from V_{TTIx} or V_{TTOx} to $V_{CC} < 100$ mA

POWER DISSIPATION

The power dissipation of the ADN4604 depends on the supply voltages, I/O coupling type, and device configuration. The input termination resistors dissipate power depending on the differential input swing and common-mode voltage. When ac-coupled, the common-mode voltage is equal to the termination supply voltage (V_{TTIE} or V_{TTIW}). While the current drawn from the input termination supply is effectively zero, there is still power and heat dissipated in the termination resistors as a result of the differential signal swing. The core supply current and output termination current are strongly dependent on device configuration, such as the number of channels enabled, output level setting, and output preemphasis setting.

In high ambient temperature operating conditions, it is important to avoid exceeding the maximum junction temperature of the device. Limiting the total power dissipation can be achieved by the following:

- Reducing the output swing

- Reducing the preemphasis level
- Decreasing the supply voltages within the allowable ranges defined in Table 1
- Disabling unused channels

Alternatively, the thermal resistance can be reduced by

- Adding an external heat-sink
- Increasing the airflow

Refer to the Printed Circuit Board (PCB) Layout Guidelines section for recommendations for proper thermal stencil layout and fabrication.

OUTPUT COMPLIANCE

In low voltage applications, users must pay careful attention to both the differential and common-mode signal level. The choice of output voltage swing, preemphasis setting, supply voltages (V_{CC} and V_{TTO}), and output coupling (ac or dc) affect peak and settled single-ended voltage swings and the common-mode shift measured across the output termination resistors. These choices also affect output current and, consequently, power consumption. Table 19 shows the change in output common mode ($\Delta V_{OCM} = V_{CC} - V_{OCM}$) with output level and preemphasis setting. Single-ended output levels are calculated for V_{TTO} supplies of 3.3 V and 2.5 V to illustrate practical challenges of reducing the supply voltage. The minimum V_L (min V_L) cannot be below the absolute minimum level specified in Table 1. The combinations of output level, preemphasis, supply voltage, and output coupling for which the minimum V_L specification is violated are listed as N/A in Table 1.

Since the absolute minimum output voltage specified in Table 1 is relative to V_{CC} , decreasing V_{CC} is required to maintain the output levels within the specified limits when lower output termination voltages are required. V_{TTO} voltages as low as 1.8 V are allowable for output swings less than or equal to 400 mV (single-ended). Figure 54 illustrates an application where the ADN4604 is used as a dc-coupled level translator to interface a 3.3 V CML driver to an ASIC with 1.8 V I/Os. The diode in series with V_{CC} reduces the voltage at V_{CC} for improved output compliance.

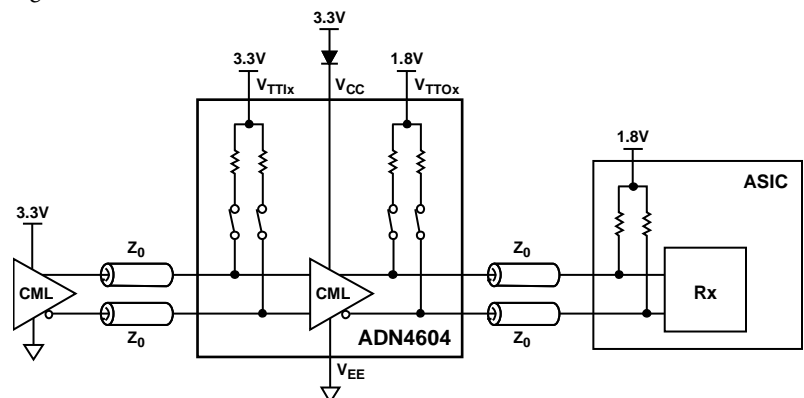


Figure 54. DC-Coupled Level Translator Application Circuit

Table 19. Output Voltage Range and Output Common-Mode Shift vs. Output Level and PE Setting

| Single-Ended Output Levels and PE Boost | | | | Register Settings | | Output Current | AC-Coupled Outputs | | | | | | DC-Coupled Outputs | | | | | |
|---|---|------------|---------|-------------------|------------|---------------------------------------|--|---------------------------------------|---|---------------------------------------|--|--|---|---------------------------------------|---------------------------------------|---------------------------------------|--|--|
| | | | | | | | V _{CC} = V _{TTO} = 3.3 V | | V _{CC} = 2.7 V V _{TTO} = 2.5 V | | V _{CC} = V _{TTO} = 3.3 V | | V _{CC} = 2.7 V V _{TTO} = 2.5 V | | | | | |
| V _{SW-DC} ¹ (mV) | V _{SW-PE} ¹ (mV) | PE Boost % | PE (dB) | TX Drive 0 | TX Drive 1 | I _{TTO} ¹ (mA) | ΔV _{OCM} ¹ (mV) | V _{H-PE} ¹ (V) | V _{L-PE} ¹ (V) | V _{H-PE} ¹ (V) | V _{L-PE} ¹ (V) | ΔV _{OCM} ¹ (mV) | V _{H-DC} ¹ (V) | V _{L-DC} ¹ (V) | V _{H-PE} ¹ (V) | V _{L-PE} ¹ (V) | | |
| 100 | 100 | 0.00 | 0.00 | 0x99 | 0x00 | 4 | 100 | 3.25 | 3.15 | 2.45 | 2.35 | 50 | 3.3 | 3.2 | 2.5 | 2.4 | | |
| 100 | 150 | 50.00 | 3.52 | 0x99 | 0x88 | 6 | 150 | 3.225 | 3.075 | 2.425 | 2.275 | 75 | 3.3 | 3.15 | 2.5 | 2.35 | | |
| 100 | 200 | 100.00 | 6.02 | 0x99 | 0x99 | 8 | 200 | 3.2 | 3 | 2.4 | 2.2 | 100 | 3.3 | 3.1 | 2.5 | 2.3 | | |
| 100 | 250 | 150.00 | 7.96 | 0x99 | 0xAA | 10 | 250 | 3.175 | 2.925 | 2.375 | 2.125 | 125 | 3.3 | 3.05 | 2.5 | 2.25 | | |
| 100 | 300 | 200.00 | 9.54 | 0x99 | 0xBB | 12 | 300 | 3.15 | 2.85 | 2.35 | 2.05 | 150 | 3.3 | 3 | 2.5 | 2.2 | | |
| 100 | 350 | 250.00 | 10.88 | 0x99 | 0xCC | 14 | 350 | 3.125 | 2.775 | 2.325 | 1.975 | 175 | 3.3 | 2.95 | 2.5 | 2.15 | | |
| 100 | 400 | 300.00 | 12.04 | 0x99 | 0xDD | 16 | 400 | 3.1 | 2.7 | 2.3 | 1.9 | 200 | 3.3 | 2.9 | 2.5 | 2.1 | | |
| 100 | 450 | 350.00 | 13.06 | 0x99 | 0xEE | 18 | 450 | 3.075 | 2.625 | 2.275 | 1.825 | 225 | 3.3 | 2.85 | 2.5 | 2.05 | | |
| 100 | 500 | 400.00 | 13.98 | 0x99 | 0xFF | 20 | 500 | 3.05 | 2.55 | 2.25 | 1.75 | 250 | 3.3 | 2.8 | 2.5 | 2 | | |
| 200 | 200 | 0.00 | 0.00 | 0xBB | 0x00 | 8 | 200 | 3.2 | 3 | 2.4 | 2.2 | 100 | 3.3 | 3.1 | 2.5 | 2.3 | | |
| 200 | 250 | 25.00 | 1.94 | 0xBB | 0x88 | 10 | 250 | 3.175 | 2.925 | 2.375 | 2.125 | 125 | 3.3 | 3.05 | 2.5 | 2.25 | | |
| 200 | 300 | 50.00 | 3.52 | 0xBB | 0x99 | 12 | 300 | 3.15 | 2.85 | 2.35 | 2.05 | 150 | 3.3 | 3 | 2.5 | 2.2 | | |
| 200 | 350 | 75.00 | 4.86 | 0xBB | 0xAA | 14 | 350 | 3.125 | 2.775 | 2.325 | 1.975 | 175 | 3.3 | 2.95 | 2.5 | 2.15 | | |
| 200 | 400 | 100.00 | 6.02 | 0xBB | 0xBB | 16 | 400 | 3.1 | 2.7 | 2.3 | 1.9 | 200 | 3.3 | 2.9 | 2.5 | 2.1 | | |
| 200 | 450 | 125.00 | 7.04 | 0xBB | 0xCC | 18 | 450 | 3.075 | 2.625 | 2.275 | 1.825 | 225 | 3.3 | 2.85 | 2.5 | 2.05 | | |
| 200 | 500 | 150.00 | 7.96 | 0xBB | 0xDD | 20 | 500 | 3.05 | 2.55 | 2.25 | 1.75 | 250 | 3.3 | 2.8 | 2.5 | 2 | | |
| 200 | 550 | 175.00 | 8.79 | 0xBB | 0xEE | 22 | 550 | 3.025 | 2.475 | 2.225 | 1.675 | 275 | 3.3 | 2.75 | 2.5 | 1.95 | | |
| 200 | 600 | 200.00 | 9.54 | 0xBB | 0xFF | 24 | 600 | 3 | 2.4 | 2.2 | 1.6 | 300 | 3.3 | 2.7 | 2.5 | 1.9 | | |
| 300 | 300 | 0.00 | 0.00 | 0xDD | 0x00 | 12 | 300 | 3.15 | 2.85 | 2.35 | 2.05 | 150 | 3.3 | 3 | 2.5 | 2.2 | | |
| 300 | 350 | 16.67 | 1.34 | 0xDD | 0x88 | 14 | 350 | 3.125 | 2.775 | 2.325 | 1.975 | 175 | 3.3 | 2.95 | 2.5 | 2.15 | | |
| 300 | 400 | 33.33 | 2.50 | 0xDD | 0x99 | 16 | 400 | 3.1 | 2.7 | 2.3 | 1.9 | 200 | 3.3 | 2.9 | 2.5 | 2.1 | | |
| 300 | 450 | 50.00 | 3.52 | 0xDD | 0xAA | 18 | 450 | 3.075 | 2.625 | 2.275 | 1.825 | 225 | 3.3 | 2.85 | 2.5 | 2.05 | | |
| 300 | 500 | 66.67 | 4.44 | 0xDD | 0xBB | 20 | 500 | 3.05 | 2.55 | 2.25 | 1.75 | 250 | 3.3 | 2.8 | 2.5 | 2 | | |
| 300 | 550 | 83.33 | 5.26 | 0xDD | 0xCC | 22 | 550 | 3.025 | 2.475 | 2.225 | 1.675 | 275 | 3.3 | 2.75 | 2.5 | 1.95 | | |
| 300 | 600 | 100.00 | 6.02 | 0xDD | 0xDD | 24 | 600 | 3 | 2.4 | 2.2 | 1.6 | 300 | 3.3 | 2.7 | 2.5 | 1.9 | | |
| 300 | 650 | 116.67 | 6.72 | 0xDD | 0xEE | 26 | 650 | 2.975 | 2.325 | 2.175 | 1.525 | 325 | 3.3 | 2.65 | 2.5 | 1.85 | | |
| 300 | 700 | 133.33 | 7.36 | 0xDD | 0xFF | 28 | 700 | 2.95 | 2.25 | 2.15 | 1.45 | 350 | 3.3 | 2.6 | 2.5 | 1.8 | | |
| 400 | 400 | 0.00 | 0.00 | 0xFF | 0x00 | 16 | 400 | 3.1 | 2.7 | 2.3 | 1.9 | 200 | 3.3 | 2.9 | 2.5 | 2.1 | | |
| 400 | 450 | 12.50 | 1.02 | 0xFF | 0x88 | 18 | 450 | 3.075 | 2.625 | 2.275 | 1.825 | 225 | 3.3 | 2.85 | 2.5 | 2.05 | | |
| 400 | 500 | 25.00 | 1.94 | 0xFF | 0x99 | 20 | 500 | 3.05 | 2.55 | 2.25 | 1.75 | 250 | 3.3 | 2.8 | 2.5 | 2 | | |
| 400 | 550 | 37.50 | 2.77 | 0xFF | 0xAA | 22 | 550 | 3.025 | 2.475 | 2.225 | 1.675 | 275 | 3.3 | 2.75 | 2.5 | 1.95 | | |
| 400 | 600 | 50.00 | 3.52 | 0xFF | 0xBB | 24 | 600 | 3 | 2.4 | 2.2 | 1.6 | 300 | 3.3 | 2.7 | 2.5 | 1.9 | | |
| 400 | 650 | 62.50 | 4.22 | 0xFF | 0xCC | 26 | 650 | 2.975 | 2.325 | 2.175 | 1.525 | 325 | 3.3 | 2.65 | 2.5 | 1.85 | | |
| 400 | 700 | 75.00 | 4.86 | 0xFF | 0xDD | 28 | 700 | 2.95 | 2.25 | 2.15 | 1.45 | 350 | 3.3 | 2.6 | 2.5 | 1.8 | | |
| 400 | 750 | 87.50 | 5.46 | 0xFF | 0xEE | 30 | 750 | 2.925 | 2.175 | N/A ² | N/A ² | 375 | 3.3 | 2.55 | 2.5 | 1.75 | | |
| 400 | 800 | 100.00 | 6.02 | 0xFF | 0xFF | 32 | 800 | 2.9 | 2.1 | N/A ² | N/A ² | 400 | 3.3 | 2.5 | 2.5 | 1.7 | | |
| 450 | 450 | 0.00 | 0.00 | 0xFF | 0x09 | 18 | 450 | 3.075 | 2.625 | 2.275 | 1.825 | 225 | 3.3 | 2.85 | 2.5 | 2.05 | | |
| 450 | 650 | 44.44 | 3.19 | 0xFF | 0xBD | 26 | 650 | 2.975 | 2.325 | 2.175 | 1.525 | 325 | 3.3 | 2.65 | 2.5 | 1.85 | | |
| 500 | 500 | 0.00 | 0.00 | 0xFF | 0x0B | 20 | 500 | 3.05 | 2.55 | N/A ² | N/A ² | 250 | 3.3 | 2.8 | 2.5 | 2 | | |
| 500 | 700 | 40.00 | 2.92 | 0xFF | 0xBF | 28 | 700 | 2.95 | 2.25 | 2.15 | 1.45 | 350 | 3.3 | 2.6 | 2.5 | 1.8 | | |
| 550 | 550 | 0.00 | 0.00 | 0xFF | 0x0D | 22 | 550 | 3.025 | 2.475 | 2.225 | 1.675 | 275 | 3.3 | 2.75 | 2.5 | 1.95 | | |
| 550 | 650 | 18.18 | 1.45 | 0xFF | 0x9F | 26 | 650 | 2.975 | 2.325 | 2.175 | 1.525 | 325 | 3.3 | 2.65 | 2.5 | 1.85 | | |
| 600 | 600 | 0.00 | 0.00 | 0xFF | 0x0F | 24 | 600 | 3 | 2.4 | N/A ² | N/A ² | 300 | 3.3 | 2.7 | 2.5 | 1.9 | | |

¹ Symbol definitions are shown in Table 14.² This setting is not allowed when ac-coupled with $V_{CC} = 2.7\text{ V}$ and $V_{TTON} = 2.5\text{ V}$ or $V_{TTOS} = 2.5\text{ V}$.

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

The high speed differential inputs and outputs should be routed with 100 Ω controlled impedance differential transmission lines. The transmission lines, either microstrip or stripline, should be referenced to a solid low impedance reference plane. An example of a PCB cross-section is shown in Figure 55. The trace width (W), differential spacing (S), height above reference plane (H), and dielectric constant of the PCB material determine the characteristic impedance. Adjacent channels should be kept apart by a distance greater than 3 W to minimize crosstalk.

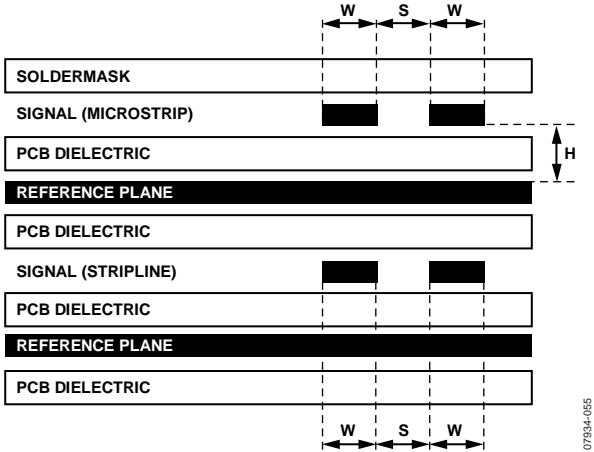


Figure 55. Example of a PCB Cross-Section

Thermal Paddle Design

The TQFP is designed with an exposed thermal paddle to conduct heat away from the package and into the PCB. By incorporating thermal vias into the PCB thermal paddle, heat is dissipated more effectively into the inner metal layers of the PCB. To ensure device performance at elevated temperatures, it is important to have a sufficient number of thermal vias incorporated into the design. An insufficient number of thermal vias results in a θ_{JA} value larger than specified in Table 1.

It is recommended that a via array of 4 × 4 or 5 × 5 with a diameter of 0.3 mm to 0.33 mm be used to set a pitch between 1.0 mm and 1.2 mm. A representative of these arrays is shown in Figure 56.

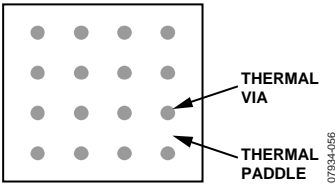


Figure 56. PCB Thermal Paddle and Via

Stencil Design for the Thermal Paddle

To effectively remove heat from the package and to enhance electrical performance, the thermal paddle must be soldered (bonded) to the PCB thermal paddle, preferably with minimum voids. However, eliminating voids may not be possible because of the presence of thermal vias and the large size of the thermal paddle for larger size packages. Also, outgassing during the reflow process may cause defects (splatter, solder balling) if the solder paste coverage is too big.

It is recommended that smaller multiple openings in the stencil be used instead of one big opening for printing solder paste on the thermal paddle region. This typically results in 50% to 80% solder paste coverage. Figure 57 shows how to achieve these levels of coverage.

Voids within solder joints under the exposed paddle can have an adverse affect on high speed and RF applications, as well as on thermal performance. Because the package incorporates a large center paddle, controlling solder voiding within this region can be difficult. Voids within this ground plane can increase the current path of the circuit. The maximum size for a void should be less than via pitch within the plane. This assures that any one via is not rendered ineffectual when any void increases the current path beyond the distance to the next available via.

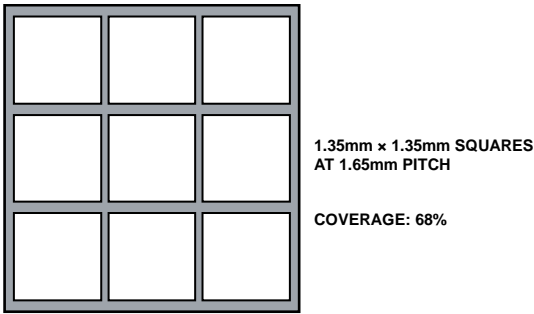


Figure 57. Typical Thermal Paddle Stencil Design

Large voids in the thermal paddle area should be avoided. To control voids in the thermal paddle area, solder masking may be required for thermal vias to prevent solder wicking inside the via during reflow, thus displacing the solder away from the interface between the package thermal paddle and thermal paddle land on the PCB. There are several methods employed for this purpose, such as via tenting (top or bottom side), using dry film solder mask; via plugging with liquid photo-imagible (LPI) solder mask from the bottom side; or via encroaching. These options are depicted in Figure 58. In case of via tenting, the solder mask diameter should be 100 microns larger than the via diameter.

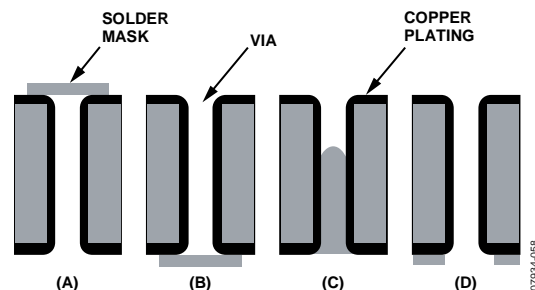
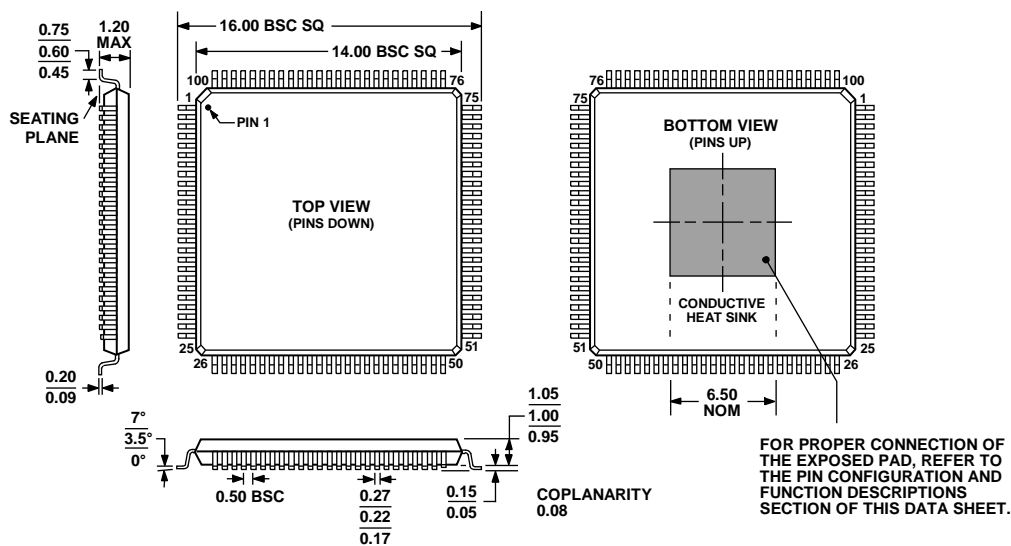


Figure 58. Solder Mask Options for Thermal Vias: (A) Via Tenting from the Top; (B) Via Tenting from the Bottom; (C) Via Plugging, Bottom; and (D) Via Encroaching, Bottom

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

021809-A

Figure 59. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Ordering Quantity |
|-----------------------------|-------------------|---|----------------|-------------------|
| ADN4604ASVZ ¹ | –40°C to +85°C | 100-Lead Thin Quad Flat Package [TQFP_EP] | SV-100-1 | 1000 |
| ADN4604ASVZ-RL ¹ | –40°C to +85°C | 100-Lead Thin Quad Flat Package [TQFP_EP], 13" Tape & Reel | SV-100-1 | |
| ADN4604-EVALZ ¹ | | Evaluation Board | | |

¹ Z = RoHS Compliant Part.

NOTES

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.