Micropower, High Accuracy Voltage References

ADR3425/ADR3450

FEATURES

Initial accuracy: ±0.1% (max)
Maximum temperature coefficient: 8 ppm/°C
Operating temperature range: −40°C to +125°C
Output current: +10 mA source/−3 mA sink
Low quiescent current: 100 µA (max)
Low dropout voltage: 250 mV at 2 mA
Output noise (0.1 Hz to 10 Hz): < 18 µV p-p at 2.5 V typ
6-lead SOT-23 package

APPLICATIONS

Precision data acquisition systems
High resolution data converters
Industrial instrumentation
Medical devices
Automotive controls
Battery-powered devices

GENERAL DESCRIPTION

The ADR3425/ADR3450 are low-cost, low-power, high precision CMOS voltage references, featuring ±0.1% initial accuracy, low operating current, and low output noise in a small SOT-23 package.

For high accuracy, output voltage and temperature coefficient are trimmed digitally during final assembly using Analog Devices, Inc., patented DigiTrim® technology. Stability and system reliability are further improved by the low output voltage hysteresis of the device and low long-term output voltage drift.

Furthermore, the low operating current of the device (100 µA maximum) facilitates usage in low-power devices, while its low output noise helps maintain signal integrity in critical signal processing systems.

The ADR3425/ADR3450 are available in a wide range of output voltages, all of which are specified over the industrial temperature range of −40°C to +125°C.

Table 1. Selection Guide

Model	Output Voltage (V)	Input Voltage Range (V)
ADR3425	2.500	2.7 to 5.5
ADR3450	5.000	5.2 to 5.5

PIN CONFIGURATION

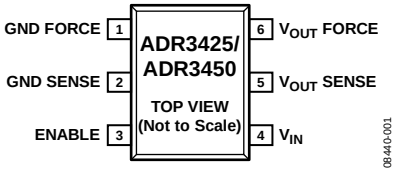

Figure 1. 6-Lead SOT-23

Table 2. Voltage Reference Choices from Analog Devices

V_{OUT} (V)	Low Cost/ Low Power	Ultralow Power	Low Noise	High Voltage, High Performance
0.5/1.0			ADR130	
2.048	ADR360	REF191	ADR430 ADR440	
2.5	ADR3425 AD1582 ADR361	ADR291 REF192	ADR431 ADR441	ADR03 AD780
3.0	AD1583 ADR363	REF193	ADR433 ADR443	ADR06 AD780
3.3	ADR366	REF196		
4.096	AD1584 ADR364	ADR292 REF198	ADR434 ADR444	
5.0	ADR3450 AD1585 ADR365	ADR293 REF195	ADR435 ADR445	ADR02 AD780 AD586
10.0				ADR01 AD587

Rev. 0

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3/10—Revision 0: Initial Version

SPECIFICATIONS

ADR3425 ELECTRICAL CHARACTERISTICS

V_{IN} = 2.7 V to 5.5 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}		2.4975	2.500	2.5025	V
INITIAL ACCURACY	V_{OERR}				±0.1	%
					±2.5	mV
TEMPERATURE COEFFICIENT	TCV_{OUT}	−40°C ≤ T_A ≤ +125°C		2.5	8	ppm/°C
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 2.7 V to 5.5 V			50	ppm/V
		V_{IN} = 2.7 V to 5.5 V, −40°C ≤ T_A ≤ +125°C			120	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$					
Sourcing		I_L = 0 mA to +10 mA, −40°C ≤ T_A ≤ +125°C, V_{IN} = 3.0 V to 5.0 V			30	ppm/mA
Sinking		I_L = 0 mA to −3 mA, −40°C ≤ T_A ≤ +125°C, V_{IN} = 3.0 V to 5.0 V			50	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing		V_{IN} = 3.0 V to 5.5 V	10			mA
Sinking		V_{IN} = 3.0 V to 5.5 V	−3			mA
QUIESCENT CURRENT	I_Q					
Normal Operation		ENABLE ≥ V_{IN} × 0.85			85	µA
		ENABLE = V_{IN}, −40°C ≤ T_A ≤ +125°C			100	µA
Shutdown		ENABLE ≤ 0.7 V			5	µA
DROPOUT VOLTAGE[1]	V_{DO}	I_L = 0 mA, T_A = −40°C ≤ T_A ≤ +125°C			200	mV
		I_L = 2 mA, T_A = −40°C ≤ T_A ≤ +125°C			250	mV
ENABLE PIN						
Shutdown Voltage	V_L		0		0.7	V
Enable Voltage	V_H		V_{IN} × 0.85		V_{IN}	V
ENABLE Pin Leakage Current	I_{EN}	ENABLE = V_{IN}, T_A = −40°C ≤ T_A ≤ +125°C		1	3	µA
OUTPUT VOLTAGE NOISE	en p-p	f = 0.1 Hz to 10 Hz		18		µV p-p
		f = 10 Hz to 10 kHz		42		µV rms
OUTPUT VOLTAGE NOISE DENSITY	en	f = 1 kHz		1.2		µV/√Hz
OUTPUT VOLTAGE HYSTERESIS[2]	ΔV_{OUT_HYS}	T_A = +25°C to −40°C to +125°C to +25°C		70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 60 Hz		−60		dB
LONG-TERM STABILITY	ΔV_{OUT_LTD}	1000 hours at 50°C		30		ppm
TURN-ON SETTLING TIME	t_R			800		µs

[1] Refer to the minimum difference between V_{IN} and V_{OUT} such that V_{OUT} maintains a minimum accuracy of 0.1%. See the Terminology section.
[2] See the Terminology section. The part is placed through the temperature cycle in the order of temperatures shown.

ADR3450 ELECTRICAL CHARACTERISTICS

V_{IN} = 5.2 V to 5.5 V, I_L = 0 mA, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE	V_{OUT}		4.995	5.000	5.005	V
INITIAL ACCURACY	V_{OERR}				±0.1	%
					±5.0	mV
TEMPERATURE COEFFICIENT	TCV_{OUT}	−40°C ≤ T_A ≤ +125°C		2.5	8	ppm/°C
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 5.2 V to 5.5 V			50	ppm/V
		V_{IN} = 5.2 V to 5.5 V, −40°C ≤ T_A ≤ +125°C			120	ppm/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$					
Sourcing		I_L = 0 mA to +10 mA, −40°C ≤ T_A ≤ +125°C, V_{IN} = 5.5 V			30	ppm/mA
Sinking		I_L = 0 mA to −3 mA, −40°C ≤ T_A ≤ +125°C, V_{IN} = 5.5 V			50	ppm/mA
OUTPUT CURRENT CAPACITY	I_L					
Sourcing		V_{IN} = 5.5 V	10			mA
Sinking		V_{IN} = 5.5 V	−3			mA
QUIESCENT CURRENT	I_Q					
Normal Operation		ENABLE ≥ V_{IN} × 0.85			85	µA
		ENABLE = V_{IN}, −40°C ≤ T_A ≤ +125°C			100	µA
Shutdown		ENABLE ≤ 0.7 V			5	µA
DROPOUT VOLTAGE[1]	V_{DO}	I_L = 0 mA, T_A = −40°C ≤ T_A ≤ +125°C			200	mV
		I_L = 2 mA, T_A = −40°C ≤ T_A ≤ +125°C			250	mV
ENABLE PIN						
Shutdown Voltage	V_L		0		0.7	V
Enable Voltage	V_H		V_{IN} × 0.85		V_{IN}	V
ENABLE Pin Leakage Current	I_{EN}	ENABLE = V_{IN}, T_A = −40°C ≤ T_A ≤ +125°C		1	3	µA
OUTPUT VOLTAGE NOISE	en p-p	f = 0.1 Hz to 10 Hz		35		µV p-p
		f = 10 Hz to 10 kHz		60		µV rms
OUTPUT VOLTAGE NOISE DENSITY	en	f = 1 kHz		1.9		µV/√Hz
OUTPUT VOLTAGE HYSTERESIS[2]	ΔV_{OUT_HYS}	T_A = +25°C to −40°C to +125°C to +25°C		70		ppm
RIPPLE REJECTION RATIO	RRR	f_{IN} = 60 Hz		−58		dB
LONG-TERM STABILITY	ΔV_{OUT_LTD}	1000 hours at 50°C		30		ppm
TURN-ON SETTLING TIME	t_R			1.2		ms

[1] Refer to the minimum difference between V_{IN} and V_{OUT} such that V_{OUT} maintains a minimum accuracy of 0.1%. See the Terminology section.
[2] See the Terminology section. The part is placed through the temperature cycle in the order of temperatures shown.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
Supply Voltage	6 V
ENABLE to GND SENSE Voltage	V_{IN}
V_{IN} Minimum Slew Rate	0.1 V/ms
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +125°C
Junction Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions; that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
6-Lead SOT-23 (RJ-6)	230	92	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

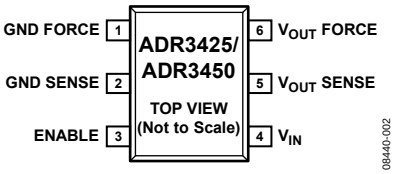

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND FORCE	Ground Force Connection[1].
2	GND SENSE	Ground Voltage Sense Connection. Connect directly to point of lowest potential in application[1].
3	ENABLE	Enable Connection. Enables or disables the device.
4	V_{IN}	Input Voltage Connection.
5	V_{OUT} SENSE	Reference Voltage Output Sensing Connection. Connect directly to the voltage input of load devices[1].
6	V_{OUT} FORCE	Reference Voltage Output[1].

[1] See the Applications section for more information on force/sense connections.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

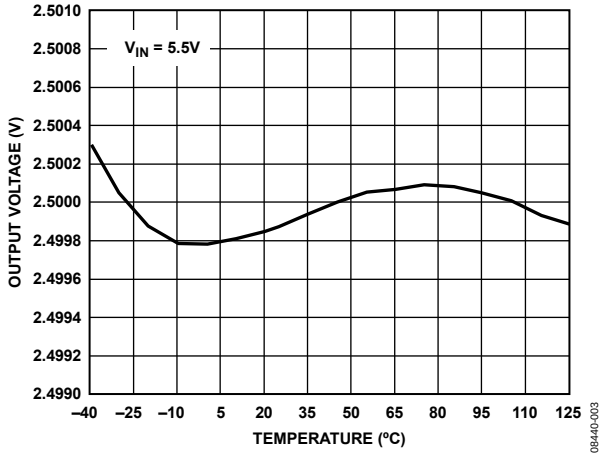

Figure 3. ADR3425 Output Voltage vs. Temperature

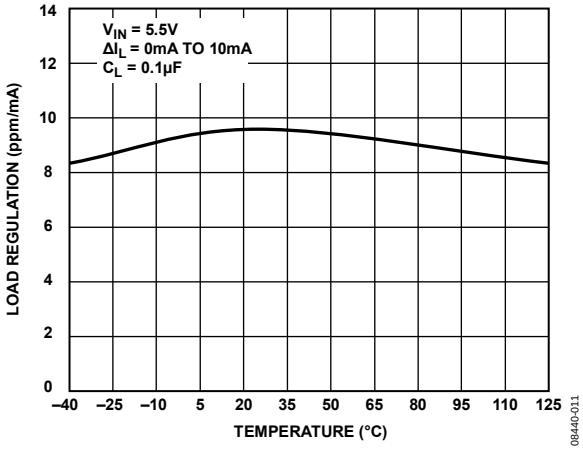

Figure 6. ADR3425 Load Regulation vs. Temperature (Sourcing)

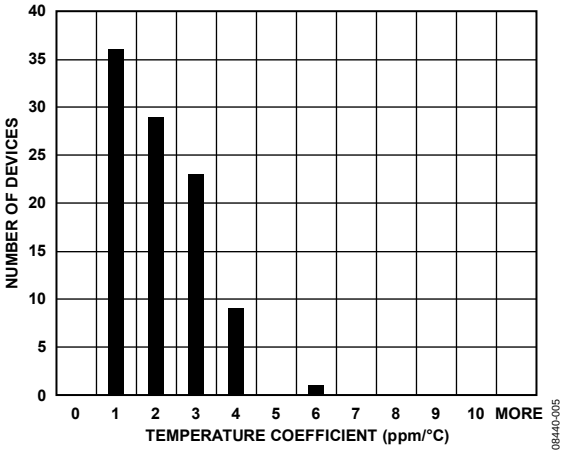

Figure 4. ADR3425 Temperature Coefficient Distribution

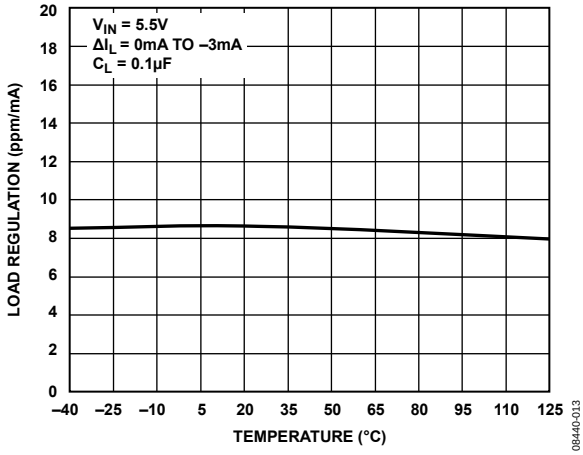

Figure 7. ADR3425 Load Regulation vs. Temperature (Sinking)

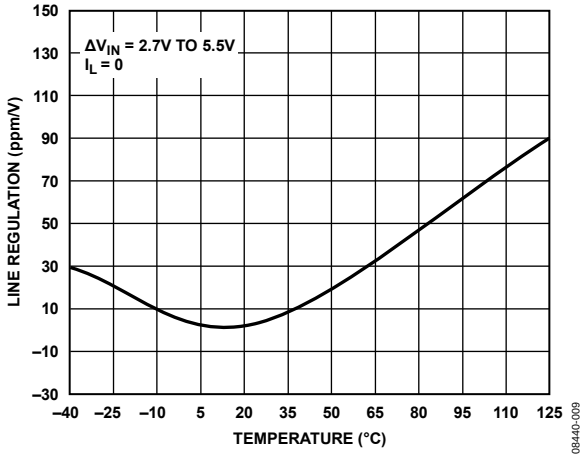

Figure 5. ADR3425 Line Regulation vs. Temperature

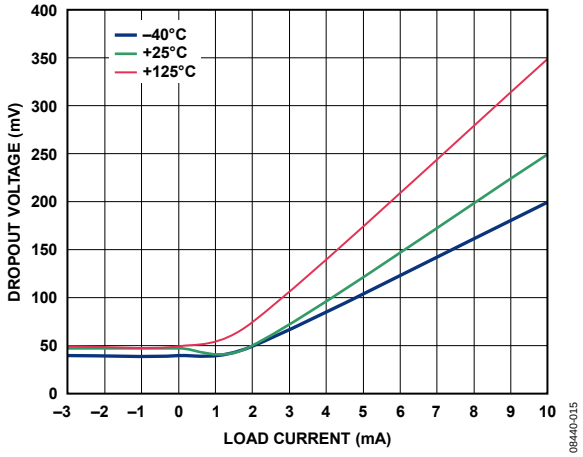

Figure 8. ADR3425 Dropout Voltage vs. Load Current

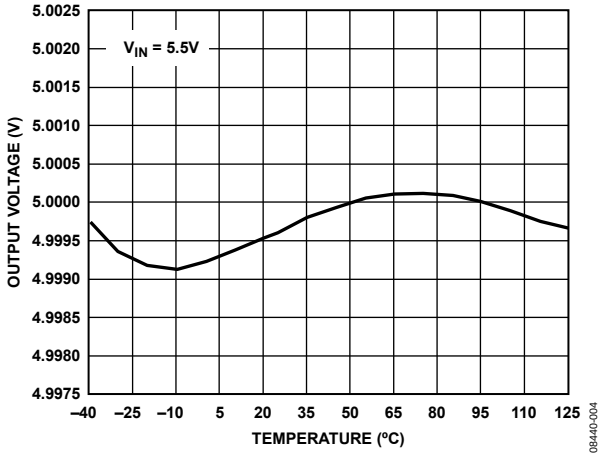

Figure 9. ADR3450 Output Voltage vs. Temperature

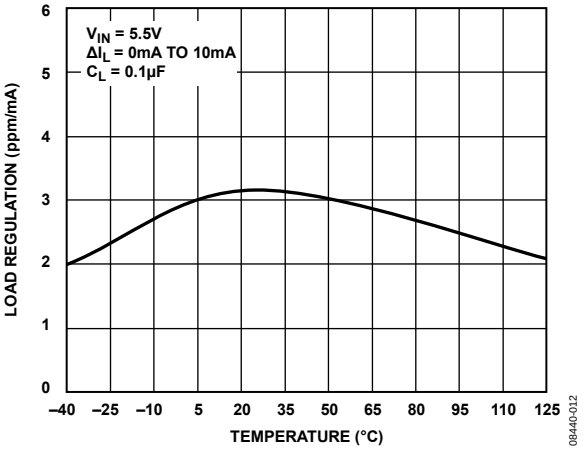

Figure 12. ADR3450 Load Regulation vs. Temperature (Sourcing)

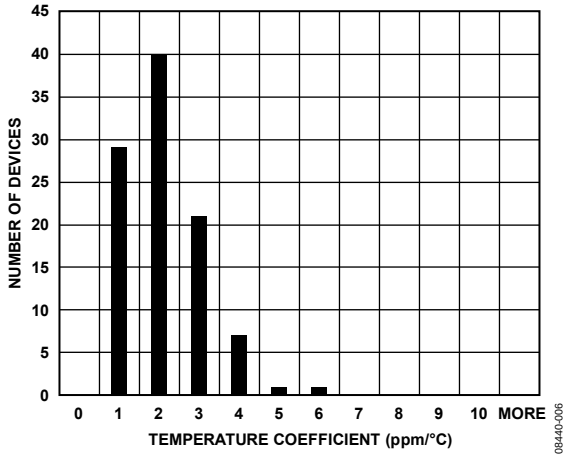

Figure 10. ADR3450 Temperature Coefficient Distribution

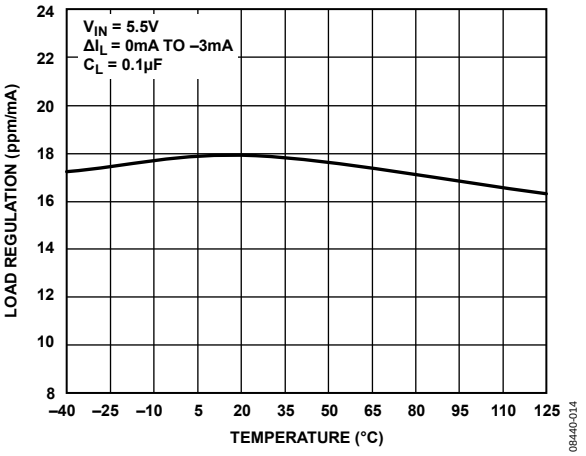

Figure 13. ADR3450 Load Regulation vs. Temperature (Sinking)

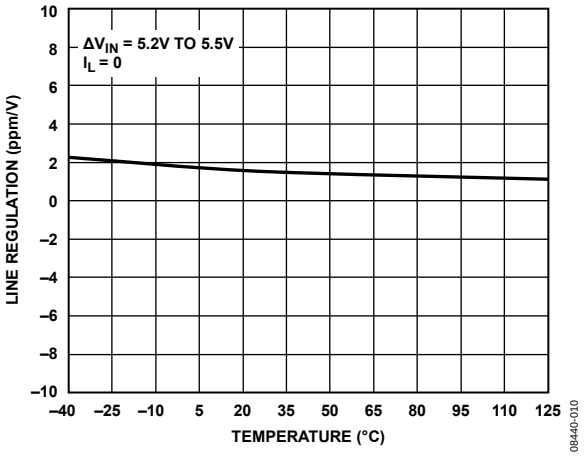

Figure 11. ADR3450 Line Regulation vs. Temperature

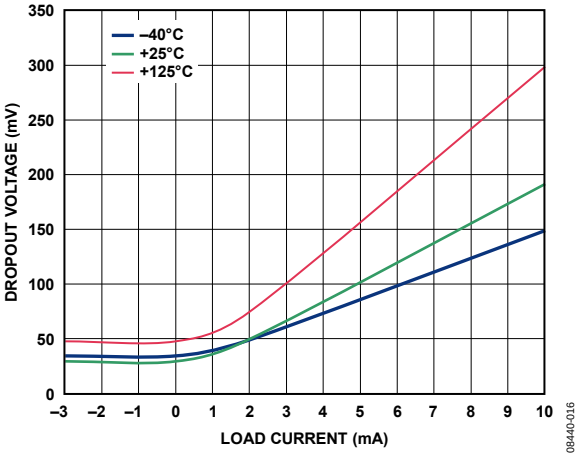

Figure 14. ADR3450 Dropout Voltage vs. Load Current

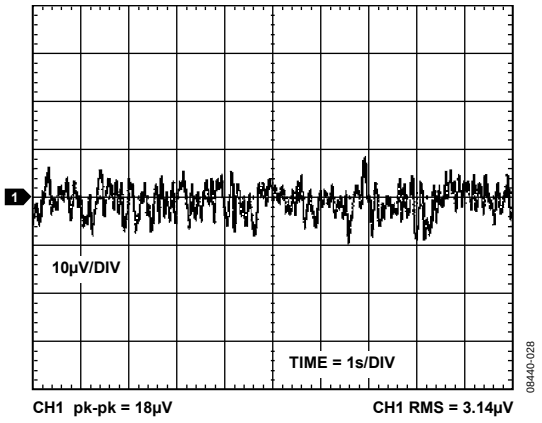

Figure 15. ADR3425 Output Voltage Noise (0.1 Hz to 10 Hz)

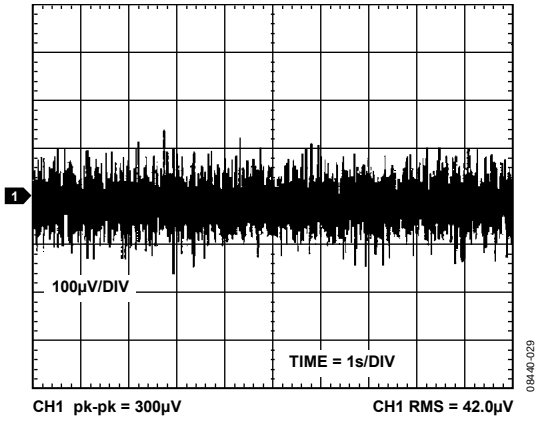

Figure 16. ADR3425 Output Voltage Noise (10 Hz to 10 kHz)

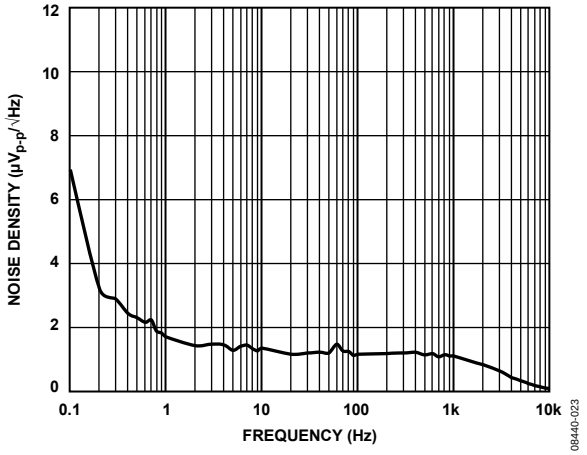

Figure 17. ADR3425 Output Noise Spectral Density

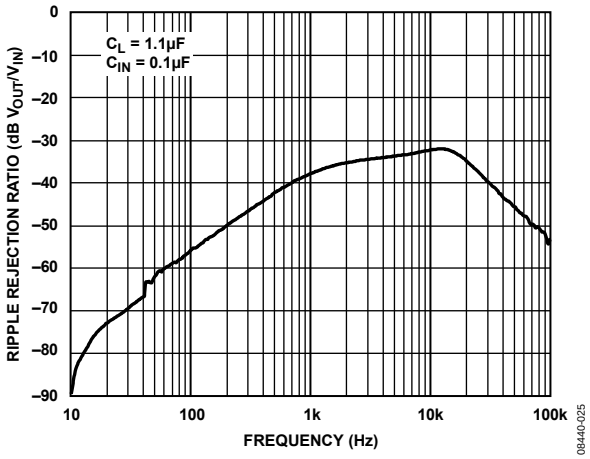

Figure 18. ADR3425 Ripple Rejection Ratio vs. Frequency

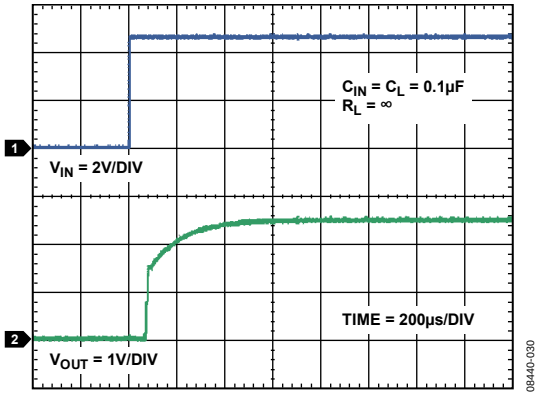

Figure 19. ADR3425 Start-Up Response

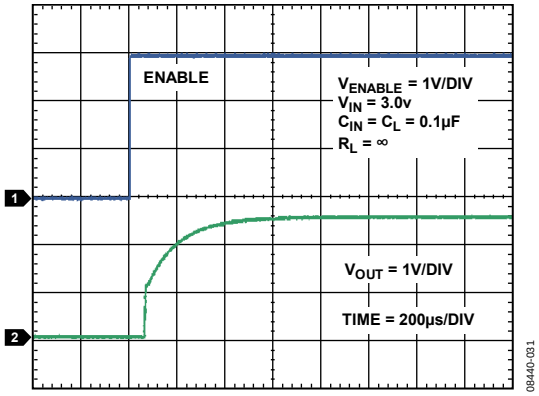

Figure 20. ADR3425 Restart Response from Shutdown

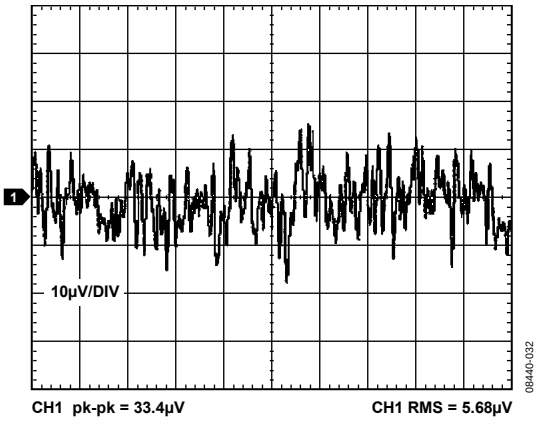

Figure 21. ADR3450 Output Voltage Noise (0.1 Hz to 10 Hz)

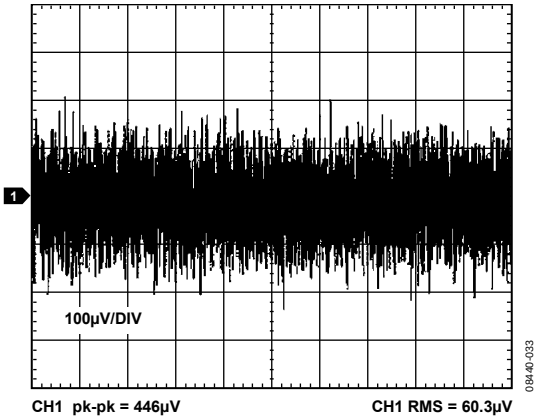

Figure 22. ADR3450 Output Voltage Noise (10 Hz to 10 kHz)

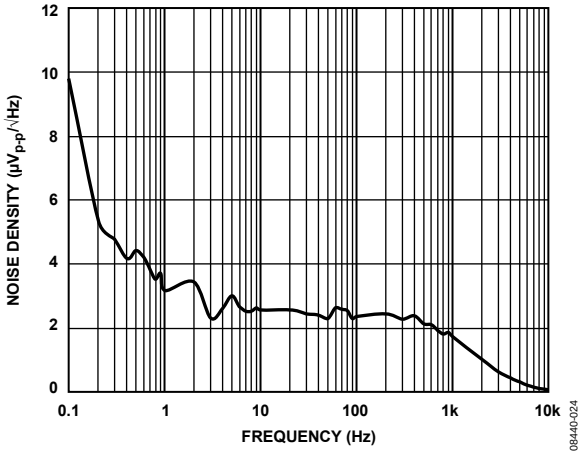

Figure 23. ADR3450 Output Noise Spectral Density

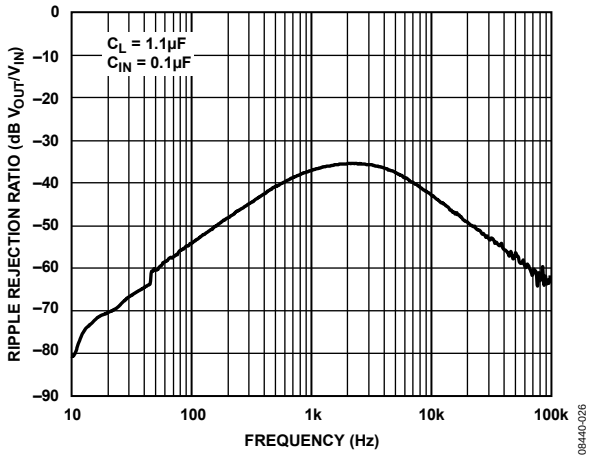

Figure 24. ADR3450 Ripple Rejection Ratio vs. Frequency

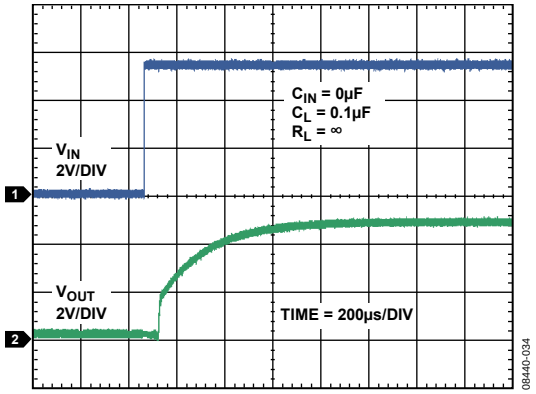

Figure 25. ADR3450 Start-Up Response

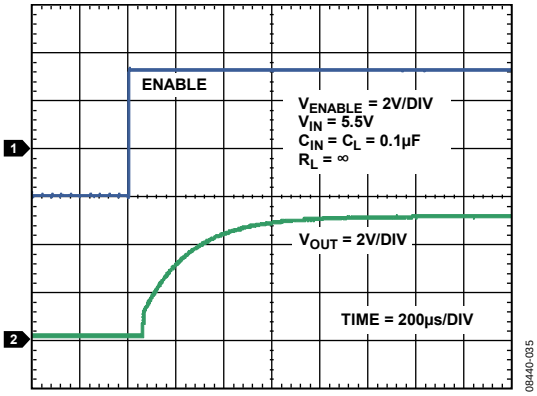

Figure 26. ADR3450 Restart Response from Shutdown

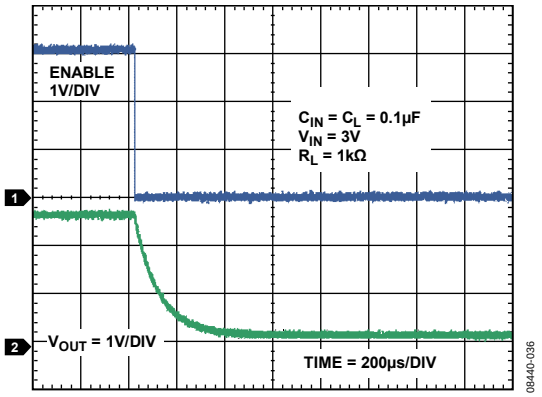

Figure 27. ADR3425 Shutdown Response

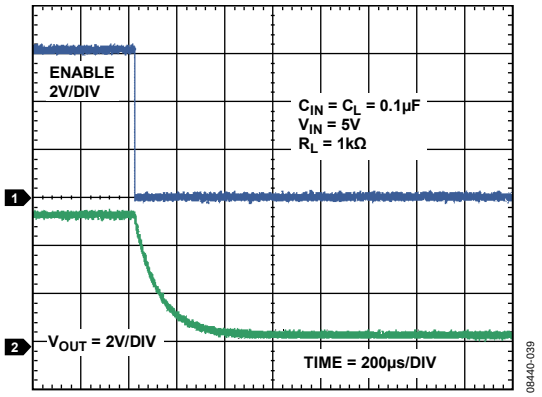

Figure 30. ADR3450 Shutdown Response

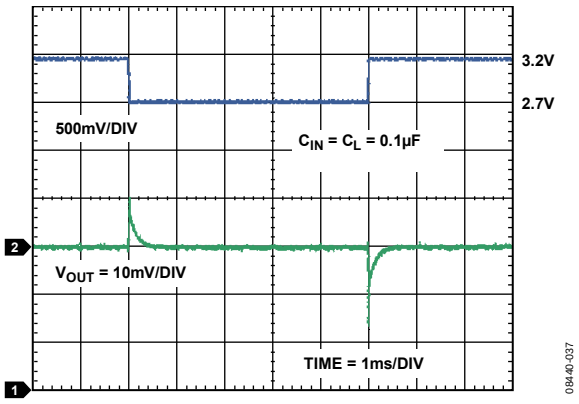

Figure 28. ADR3425 Line Transient Response

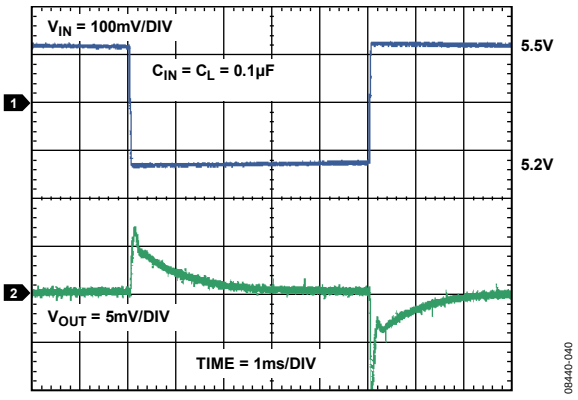

Figure 31. ADR3450 Line Transient Response

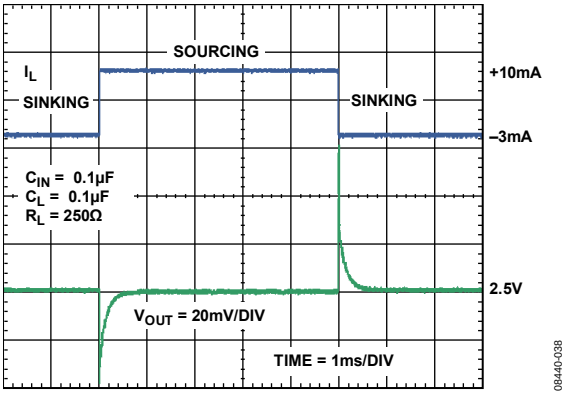

Figure 29. ADR3425 Load Transient Response

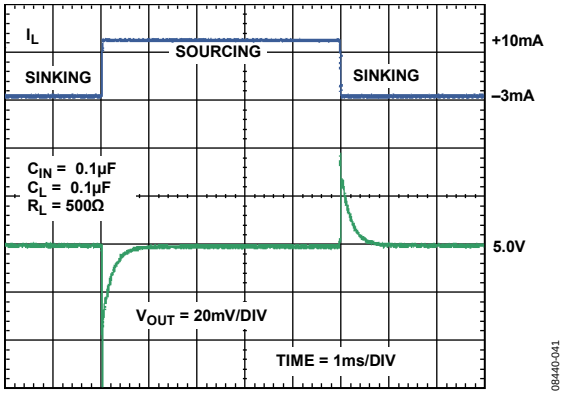

Figure 32. ADR3450 Load Transient Response

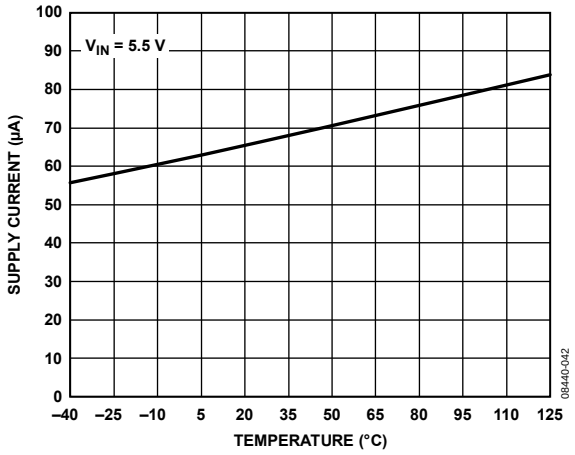

Figure 33. Supply Current vs. Temperature

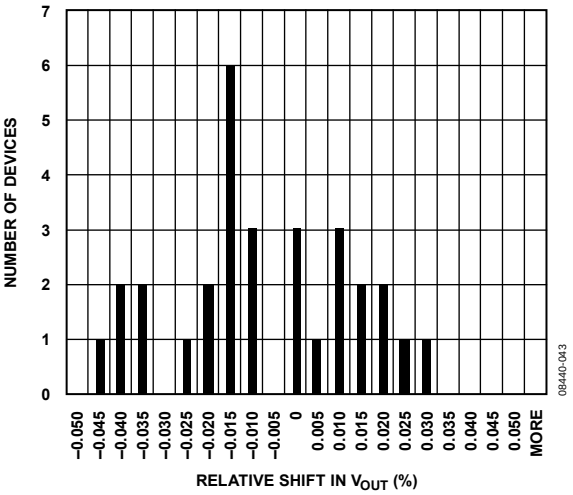

Figure 36. Output Voltage Drift Distribution After Reflow (SHR Drift)

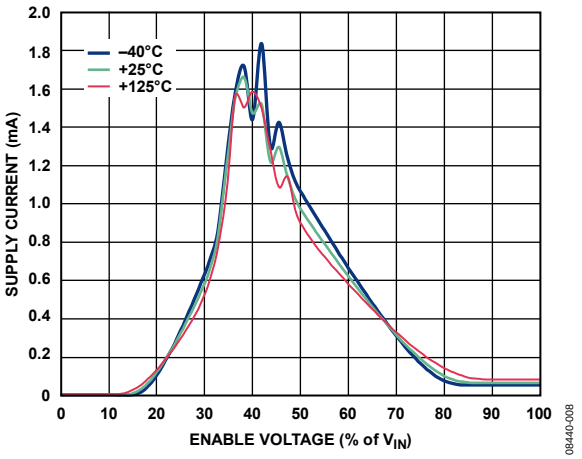

Figure 34. Supply Current vs. Enable Pin Voltage

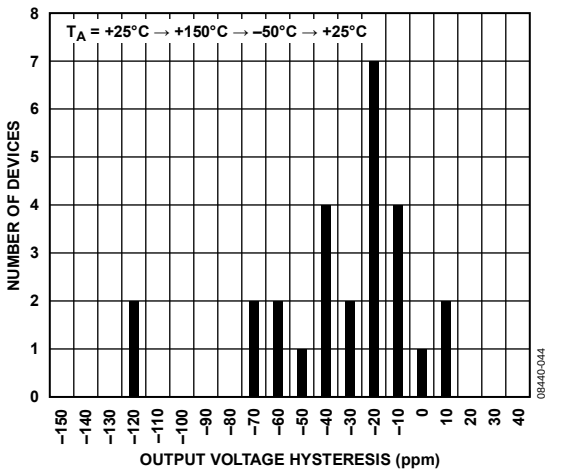

Figure 37. Thermally Induced Output Voltage Hysteresis Distribution

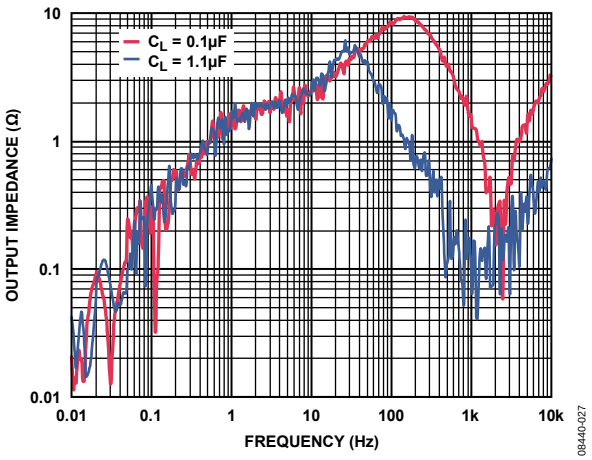

Figure 35. ADR3450 Output Impedance vs. Frequency

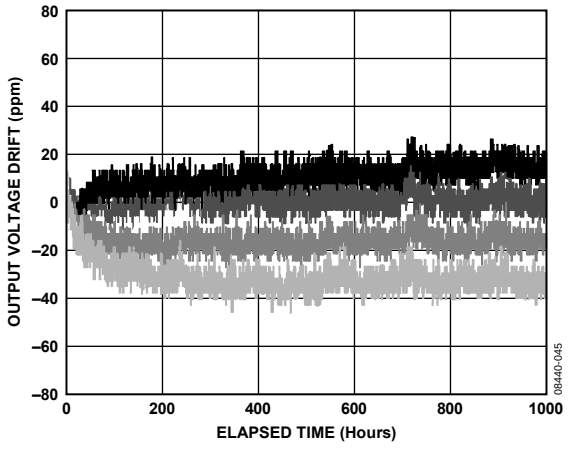

Figure 38. ADR3450 Typical Long-Term Drift (Four Devices, 1000 Hours)

TERMINOLOGY

Dropout Voltage (V_{DO})
Dropout voltage, sometimes referred to as supply voltage headroom or supply-output voltage differential, is defined as the minimum voltage differential between the input and output such that the output voltage is maintained to within 0.1% accuracy.

$$V_{DO} = (V_{IN} - V_{OUT})_{min} \mid I_L = constant$$

Because the dropout voltage depends upon the current passing through the device, it is always specified for a given load current. In series-mode devices, dropout voltage typically increases proportionally to load current; see Figure 8 and Figure 14.

Temperature Coefficient (TCV_{OUT})
The temperature coefficient relates the change in output voltage to the change in ambient temperature of the device, as normalized by the output voltage at 25°C. This parameter is expressed in ppm/°C and can be determined by the following equation:

$$TCV_{OUT} = \left| \frac{\max\{V_{OUT}(T_1, T_2, T_3)\} - \min\{V_{OUT}(T_1, T_2, T_3)\}}{V_{OUT}(T_2) \times (T_3 - T_1)} \right| \times 10^6 \, [ppm/°C]$$

where:
$V_{OUT}(T)$ is the output voltage at temperature T and
T_1 = −40°C.
T_2 = +25°C.
T_3 = +125°C.

This three-point method ensures that TCV_{OUT} accurately portrays the maximum difference between any of the three temperatures at which the output voltage of the part is measured.

The TCV_{OUT} for the ADR3425/ADR3450 is guaranteed via statistical means. This is accomplished by recording output voltage data for a large number of units over temperature, computing TCV_{OUT} for each individual device via the above equation, then defining the maximum TCV_{OUT} limits as the mean TCV_{OUT} for all devices extended by 6 standard deviations (6σ).

Thermally Induced Output Voltage Hysteresis (ΔV_{OUT_HYS})
Thermally induced output voltage hysteresis represents the change in output voltage after the device is exposed to a specified temperature cycle. This is expressed as either a shift in voltage or a difference in ppm from the nominal output:

$$\Delta V_{OUT\_HYS} = V_{OUT}(25°C) - V_{OUT\_TC} \quad [V]$$

$$\Delta V_{OUT\_HYS} = \frac{V_{OUT}(25°C) - V_{OUT\_TC}}{V_{OUT}(25°C)} \times 10^6 \quad [ppm]$$

where:
V_{OUT}(25°C) is the output voltage at 25°C.
V_{OUT_TC} is the output voltage after temperature cycling.

Long-Term Stability (ΔV_{OUT_LTD})
Long-term stability refers to the shift in output voltage at 50°C after 1000 hours of operation in a 50°C environment. Ambient temperature is kept at 50°C to ensure that the temperature chamber does not switch randomly between heating and cooling, which can cause instability over the 1000 hour measurement. This is also expressed as either a shift in voltage or a difference in ppm from the nominal output.

$$\Delta V_{OUT\_LTD} = \left| V_{OUT}(t_1) - V_{OUT}(t_0) \right| \quad [V]$$

$$\Delta V_{OUT\_LTD} = \left| \frac{V_{OUT}(t_1) - V_{OUT}(t_0)}{V_{OUT}(t_0)} \right| \times 10^6 \quad [ppm]$$

where:
$V_{OUT}(t_0)$ is the V_{OUT} at 50°C at time 0.
$V_{OUT}(t_1)$ is the V_{OUT} at 50°C after 1000 hours of operation at 50°C.

Line Regulation
Line regulation refers to the change in output voltage in response to a given change in input voltage and is expressed in either percent per volt, ppm per volt, or µV per volt change in input voltage. This parameter accounts for the effects of self-heating.

Load Regulation
Load regulation refers to the change in output voltage in response to a given change in load current and is expressed in µV per mA, ppm per mA, or ohms of dc output resistance. This parameter accounts for the effects of self-heating.

Solder Heat Resistance (SHR) Drift
SHR drift refers to the permanent shift in output voltage induced by exposure to reflow soldering, expressed in units of ppm. This is caused by changes in the stress exhibited upon the die by the package materials when exposed to high temperatures. This effect is more pronounced in lead-free soldering processes due to higher reflow temperatures.

THEORY OF OPERATION

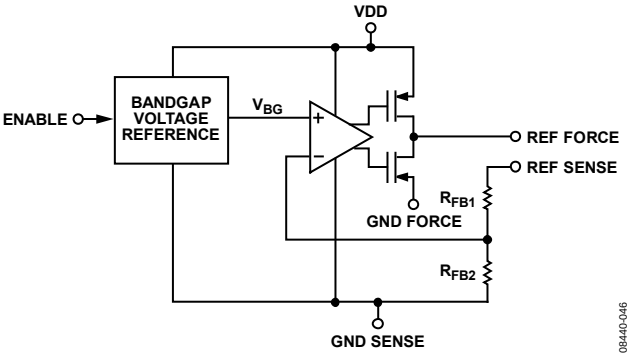

Figure 39. Block Diagram

The ADR3425/ADR3450 use a patented voltage reference architecture to achieve high accuracy, low temperature coefficient (TC), and low noise in a CMOS process. Like all bandgap references, the ADR3425/ADR3450 combine two voltages of opposite TCs to create an output voltage that is nearly independent of ambient temperature. However, unlike traditional bandgap voltage references, the temperature-independent voltage of the ADR3425/ADR3450 are arranged to be the base-emitter voltage, V_{BE}, of a bipolar transistor at room temperature rather than the V_{BE} extrapolated to 0 K (the V_{BE} of bipolar transistor at 0 K is approximately V_{G0}, the band gap voltage of silicon). A corresponding positive-TC voltage is then added to the V_{BE} voltage to compensate for its negative TC.

The key benefit of this technique is that the trimming of the initial accuracy and TC can be performed without interfering with one another, thereby increasing overall accuracy across temperature. Curvature correction techniques further reduce the temperature variation.

The bandgap voltage is then buffered and amplified to produce stable output voltages of 2.5 V and 5.0 V. The output buffer can source up to 10 mA and sink up to 3 mA of load current.

The ADR3425/ADR3450 leverage Analog Devices patented DigiTrim technology to achieve high initial accuracy and low TC, while precision layout techniques lead to very low long-term drift and thermal hysteresis.

LONG-TERM STABILITY

One of the key parameters of the ADR3425/ADR3450 references is long-term stability. Regardless of output voltage, internal testing during development showed a typical drift of approximately 30 ppm after 1,000 hours of continuous, non loaded operation in a +50°C environment.

It is important to understand that long-term stability is not guaranteed by design and that the output from the device may shift beyond the typical 30 ppm specification at any time, especially during the first 200 hours of operation. For systems that require highly stable output voltages over long periods of time, the designer should consider burning-in the devices prior to use to minimize the amount of output drift exhibited by the reference over time. See the AN-713 Application Note for more information regarding the effects of long-term drift and how it can be minimized.

POWER DISSIPATION

The ADR3425/ADR3450 voltage references are capable of sourcing up to 10 mA of load current at room temperature across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current should be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated via the following equation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}} [W]$$

where:
P_D is the device power dissipation.
T_J is the device junction temperature.
T_A is the ambient temperature.
θ_{JA} is the package (junction-to-air) thermal resistance.

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the part be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

APPLICATIONS

BASIC VOLTAGE REFERENCE CONNECTION

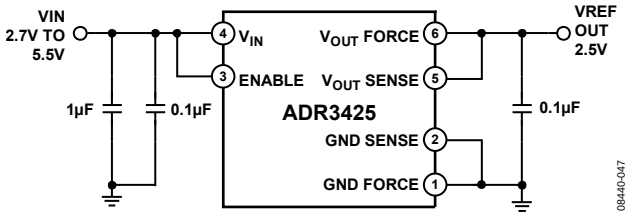

Figure 40. Basic Reference Connection

The circuit shown in Figure 40 illustrates the basic configuration for the ADR3425/ADR3450. Bypass capacitors should be connected according to the guidelines below.

INPUT AND OUTPUT CAPACITORS

A 1 µF to 10 µF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. An additional 0.1 µF ceramic capacitor should be connected in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least a 0.1 µF must be connected to the output to improve stability and help filter out high frequency noise. An additional 1 µF to 10 µF electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, the designer should keep in mind that doing so increases the turn-on time of the device.

Best performance and stability is attained with low-ESR (for example, less than 1 Ω), low-inductance ceramic chip-type output capacitors (X5R, X7R or similar). If using an electrolytic capacitor on the output, a 0.1 µF ceramic capacitor should be placed in parallel to reduce overall ESR on the output.

4-WIRE KELVIN CONNECTIONS

Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this drop can reach several millivolts or more, introducing a considerable error into the output voltage of the reference. A 1 inch long, 5 millimeter wide trace of 1 ounce copper has a resistance of approximately 100 mΩ at room temperature; at a load current of 10 mA, this can introduce a full millivolt of error. In an ideal board layout, the reference should be mounted as close to the load as possible to minimize the length of the output traces, and, therefore, the error introduced by voltage drop. However, in applications where this is not possible or convenient, force and sense connections (sometimes referred to as Kelvin sensing connections) are provided as a means of minimizing the IR drop and improving accuracy.

Kelvin connections work by providing a set of high impedance voltage-sensing lines to the output and ground nodes. Because very little current flows through these connections, the IR drop across their traces is negligible, and the output and ground voltages can be sensed very accurately. These voltages are fed back into the internal amplifier and used to automatically correct for the voltage drop across the current-carrying output and ground lines, resulting in a highly accurate output voltage across the load. To achieve the best performance, the sense connections should be connected directly to the point in the load where the output voltage should be the most accurate. See Figure 41 for an example application.

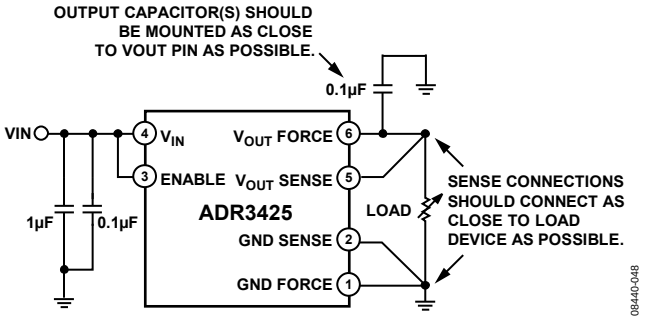

Figure 41. Application Showing Kelvin Connection

It is always advantageous to use Kelvin connections whenever possible. However, in applications where the IR drop is negligible or an extra set of traces cannot be routed to the load, the force and sense pins for both V_{OUT} and GND can simply be tied together and the device can be used in the same fashion as a normal 3-terminal reference (as shown in Figure 40).

V_{IN} SLEW RATE CONSIDERATIONS

In applications with slow-rising input voltage signals, the reference exhibits overshoot or other transient anomalies that appear on the output. These phenomena also appear during shutdown as the internal circuitry loses power.

To avoid such conditions, ensure that the input voltage waveform has both a rising and falling slew rate of at least 0.1 V/ms.

SHUTDOWN/ENABLE FEATURE

The ADR3425/ADR3450 references can be switched to a low-power shutdown mode when a voltage of 0.7 V or lower is input to the ENABLE pin. Likewise, the reference becomes operational for ENABLE voltages of 0.85 × V_{IN} or higher. During shutdown, the supply current drops to less than 5 µA, useful in applications that are sensitive to power consumption.

If using the shutdown feature, ensure that the ENABLE pin voltage does not fall between 0.7 V and 0.85 × V_{IN} because this causes a large increase in the supply current of the device and may keep the reference from starting up correctly (see Figure 34). If not using the shutdown feature, however, the ENABLE pin can simply be tied to the V_{IN} pin, and the reference remains operational continuously.

SAMPLE APPLICATIONS

Negative Reference

Figure 42 shows how to connect the ADR3425/ADR3450 and a standard CMOS op amp, such as the AD8663, to provide a negative reference voltage. This configuration provides two main advantages: first, it only requires two devices and, therefore, does not require excessive board space; second, and more importantly, it does not require any external resistors, meaning the performance of this circuit does not rely on choosing expensive parts with low temperature coefficients to ensure accuracy.

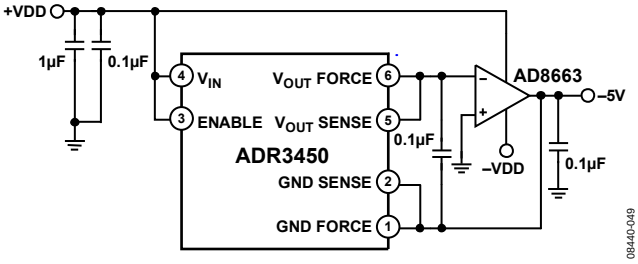

Figure 42. ADR3450 Negative Reference

In this configuration, the V_{OUT} pins of the reference sit at virtual ground, and the negative reference voltage and load current are taken directly from the output of the operational amplifier. Note that in applications where the negative supply voltage is close to the reference output voltage, a dual-supply, low offset, rail-to-rail output amplifier must be used to ensure an accurate output voltage. The operational amplifier must also be able to source or sink an appropriate amount of current for the application.

Bipolar Output Reference

Figure 43 shows a bipolar reference configuration. By connecting the output of the ADR3425/ADR3450 to the inverting terminal of an operational amplifier, it is possible to obtain both positive and negative reference voltages. R1 and R2 must be matched as closely as possible to ensure minimal difference between the negative and positive outputs. Resistors with low temperature coefficients must also be used if the circuit is used in environments with large temperature swings; otherwise, a voltage difference develops between the two outputs as the ambient temperature changes.

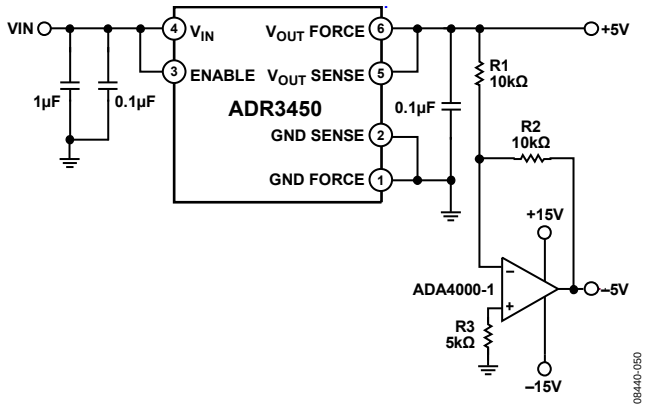

Figure 43. Bipolar Output Reference

Boosted Output Current Reference

Figure 44 shows a configuration for obtaining higher current drive capability from the ADR3425/ADR3450 references without sacrificing accuracy. The op amp regulates the current flow through the MOSFET until V_{OUT} equals the output voltage of the reference; current is then drawn directly from V_{IN} instead of from the reference itself, allowing increased current drive capability.

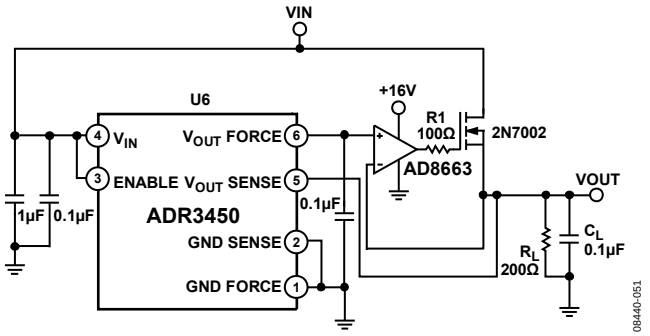

Figure 44. Boosted Output Current Reference

Because the current-sourcing capability of this circuit depends only on the I_D rating of MOSFET, the output drive capability can be adjusted to the application simply by choosing an appropriate MOSFET. In all cases, the V_{OUT} SENSE pin should be tied directly to the load device to maintain maximum output voltage accuracy.

OUTLINE DIMENSIONS

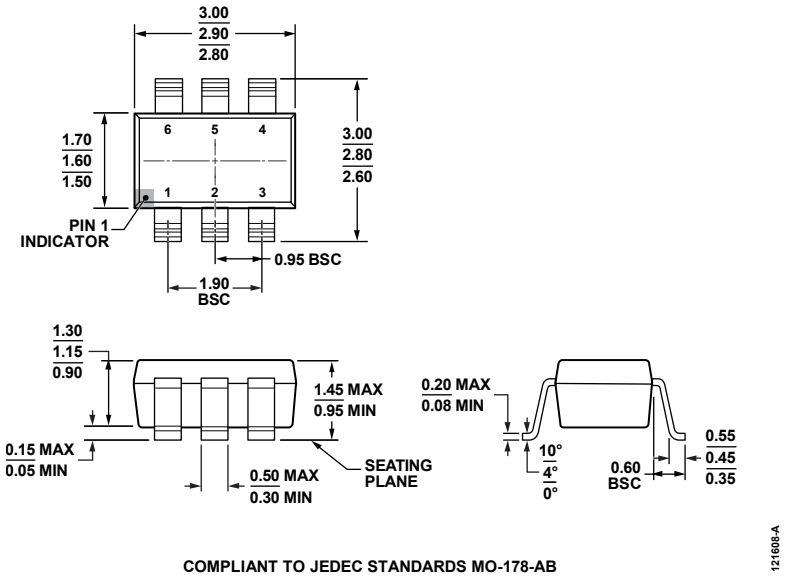

Figure 45. 6-Lead Small Outline Transistor Package (SOT-23)
(RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Output Voltage (V)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADR3425ARJZ-R2	2.500	−40°C to +125°C	6-Lead SOT-23	RJ-6	250	R2X
ADR3425ARJZ-R7	2.500	−40°C to +125°C	6-Lead SOT-23	RJ-6	3,000	R2X
ADR3450ARJZ-R2	5.000	−40°C to +125°C	6-Lead SOT-23	RJ-6	250	R34
ADR3450ARJZ-R7	5.000	−40°C to +125°C	6-Lead SOT-23	RJ-6	3,000	R34

[1] Z = RoHS Compliant Part.

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