

MCR12D, MCR12M, MCR12N

Preferred Device

Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls, and power supplies; or wherever half-wave silicon gate-controlled devices are needed.

Features

- Blocking Voltage to 800 Volts
- On-State Current Rating of 12 Amperes RMS at 80°C
- High Surge Current Capability – 100 Amperes
- Rugged, Economical TO-220AB Package
- Glass Passivated Junctions for Reliability and Uniformity
- Minimum and Maximum Values of IGT, VGT and IH Specified for Ease of Design
- High Immunity to dv/dt – 100 V/μsec Minimum at 125°C
- Pb-Free Packages are Available*

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ($T_J = -40$ to 125°C , Sine Wave, 50 to 60 Hz, Gate Open)	V_{DRM} , V_{RRM}	400 600 800	V
On-State RMS Current (180° Conduction Angles; $T_C = 80^\circ\text{C}$)	$I_{T(RMS)}$	12	A
Peak Non-repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, $T_J = 125^\circ\text{C}$)	I_{TSM}	100	A
Circuit Fusing Consideration ($t = 8.33$ ms)	I^2t	41	A ² sec
Forward Peak Gate Power (Pulse Width ≤ 1.0 μs, $T_C = 80^\circ\text{C}$)	P_{GM}	5.0	W
Forward Average Gate Power ($t = 8.3$ ms, $T_C = 80^\circ\text{C}$)	$P_{G(AV)}$	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μs, $T_C = 80^\circ\text{C}$)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



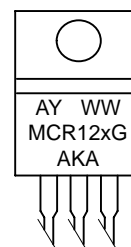
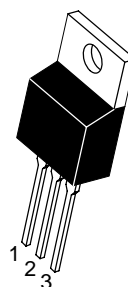
ON Semiconductor®

<http://onsemi.com>

SCRs
12 AMPERES RMS
400 thru 800 VOLTS



MARKING DIAGRAM



TO-220AB
CASE 221A-09
STYLE 3

A = Assembly Location
Y = Year
WW = Work Week
x = D, M, or N
G = Pb-Free Package
AKA = Diode Polarity

PIN ASSIGNMENT

1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

Device	Package	Shipping
MCR12D	TO-220AB	50 Units / Rail
MCR12DG	TO-220AB (Pb-Free)	50 Units / Rail
MCR12M	TO-220AB	50 Units / Rail
MCR12MG	TO-220AB (Pb-Free)	50 Units / Rail
MCR12N	TO-220AB	50 Units / Rail
MCR12NG	TO-220AB (Pb-Free)	50 Units / Rail

Preferred devices are recommended choices for future use and best overall value.

MCR12D, MCR12M, MCR12N

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.2	$^{\circ}\text{C/W}$
Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	T_L	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current ($V_D = \text{Rated } V_{DRM} \text{ and } V_{RRM}$; Gate Open)	I_{DRM} , I_{RRM}	–	–	0.01 2.0	mA
$T_J = 25^{\circ}\text{C}$					
$T_J = 125^{\circ}\text{C}$					

ON CHARACTERISTICS

Peak Forward On-State Voltage (Note 2) ($I_{TM} = 24 \text{ A}$)	V_{TM}	–	–	2.2	V
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ V}$; $R_L = 100 \Omega$)	I_{GT}	2.0	8.0	20	mA
Holding Current ($V_D = 12 \text{ V}$, Gate Open, Initiating Current = 200 mA)	I_H	4.0	20	40	mA
Latch Current ($V_D = 12 \text{ V}$, $I_G = 20 \text{ mA}$)	I_L	6.0	25	60	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12 \text{ V}$; $R_L = 100 \Omega$)	V_{GT}	0.5	0.65	1.0	V

DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}$, Exponential Waveform, Gate Open, $T_J = 125^{\circ}\text{C}$)	dv/dt	100	250	–	$\text{V}/\mu\text{s}$
Repetitive Critical Rate of Rise of On-State Current IPK = 50 A, Pw = 40 μsec , $di_G/dt = 1 \text{ A}/\mu\text{sec}$, $I_{gt} = 50 \text{ mA}$	di/dt	–	–	50	$\text{A}/\mu\text{s}$

2. Indicates Pulse Test: Pulse Width $\leq 2.0 \text{ ms}$, Duty Cycle $\leq 2\%$.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current

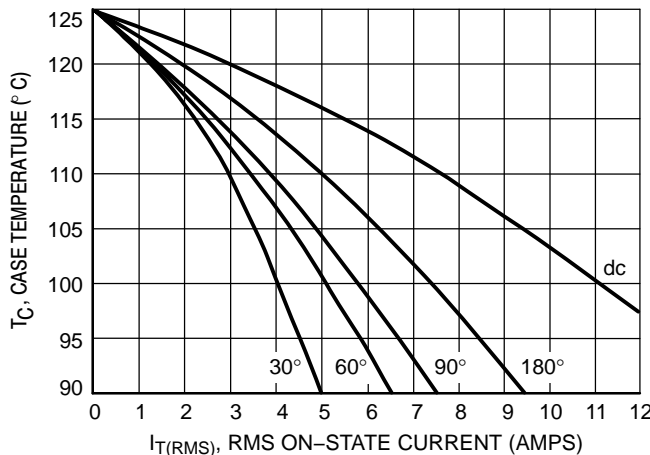
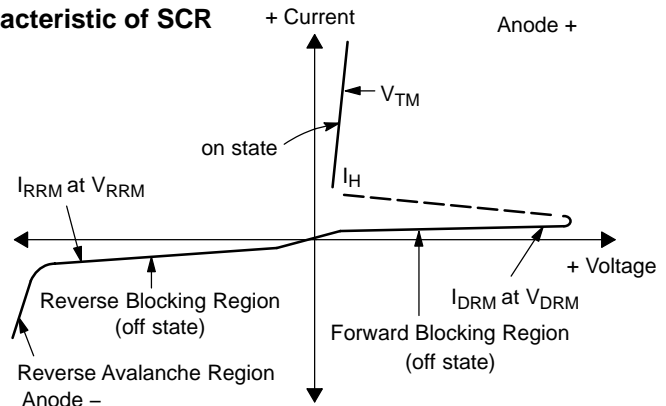


Figure 1. Typical RMS Current Derating

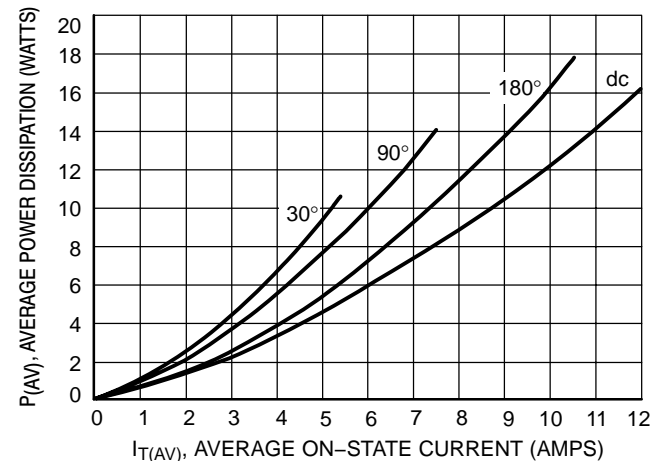


Figure 2. On-State Power Dissipation

MCR12D, MCR12M, MCR12N

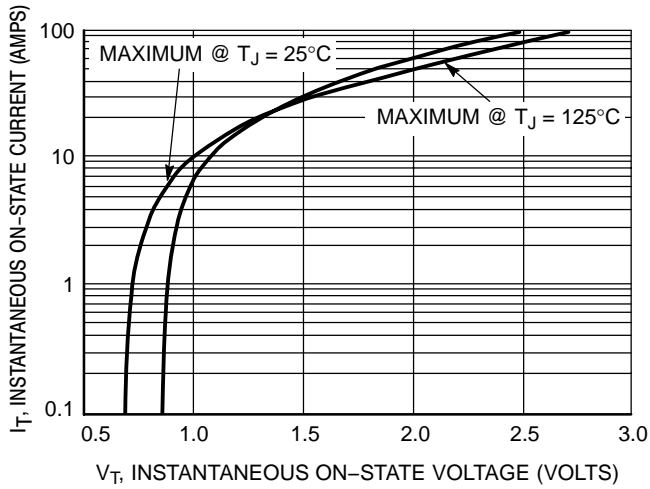


Figure 3. Typical On-State Characteristics

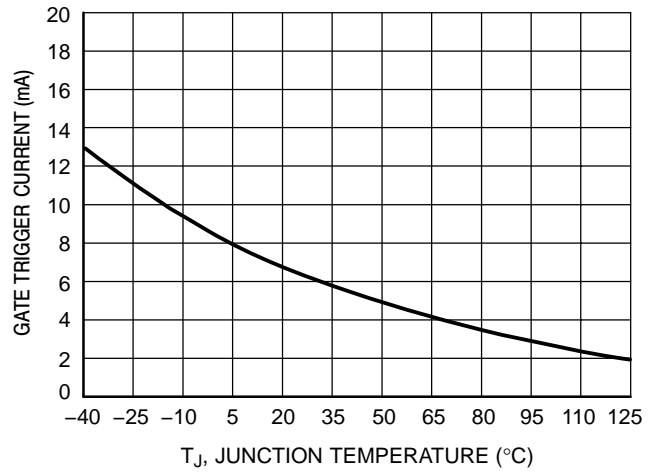


Figure 4. Typical Gate Trigger Current versus Junction Temperature

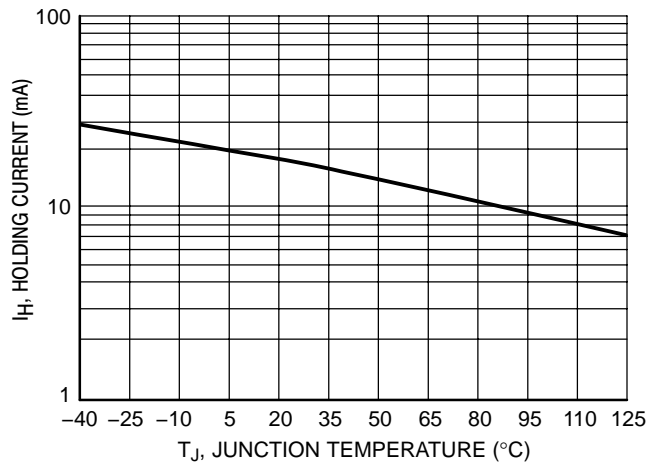


Figure 5. Typical Holding Current versus Junction Temperature

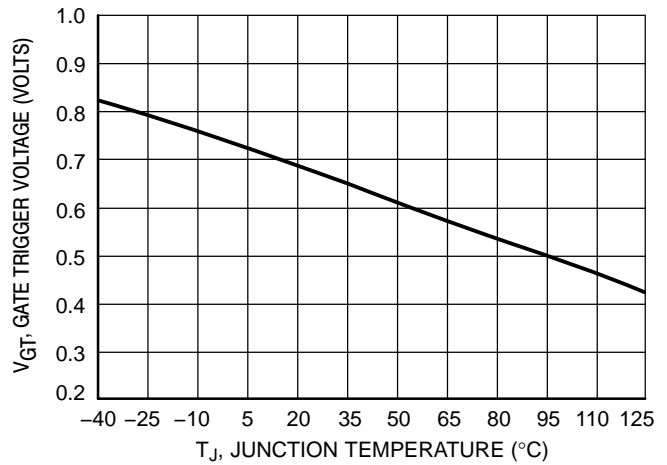


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

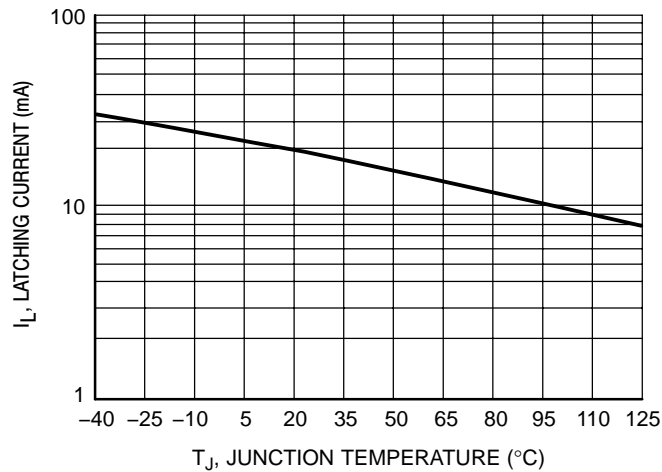
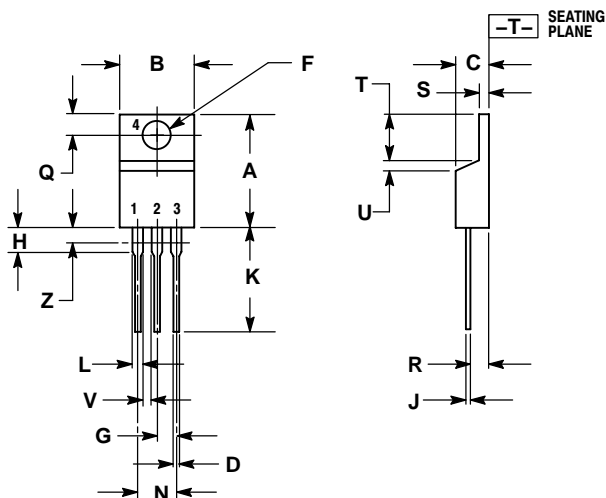


Figure 7. Typical Latching Current versus Junction Temperature

MCR12D, MCR12M, MCR12N

PACKAGE DIMENSIONS

TO-220AB
CASE 221A-09
ISSUE AA




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 3:

- PIN 1. CATHODE
- ANODE
- GATE
- ANODE

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.