

# NTF2955, NTF2955P

## Power MOSFET

–60 V, –2.6 A, Single P–Channel SOT–223

### Features

- TMOS7 Design for low  $R_{DS(on)}$
- Withstands High Energy in Avalanche and Commutation Modes
- Pb–Free Packages are Available

### Applications

- Power Supplies
- PWM Motor Control
- Converters
- Power Management

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			$V_{DSS}$	–60	V
Gate–to–Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	–2.6	A
		$T_A = 85^{\circ}\text{C}$		–2.0	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	$P_D$	2.3	W
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	–1.7	A
		$T_A = 85^{\circ}\text{C}$		–1.3	
Power Dissipation (Note 2)		$T_A = 25^{\circ}\text{C}$	$P_D$	1.0	W
Pulsed Drain Current	tp = 10 $\mu\text{s}$		$I_{DM}$	–17	A
Operating Junction and Storage Temperature			$T_J$ , $T_{STG}$	–55 to 175	$^{\circ}\text{C}$
Single Pulse Drain–to–Source Avalanche Energy ( $V_{DD} = 25\text{ V}$ , $V_G = 10\text{ V}$ , $I_{PK} = 6.7\text{ A}$ , $L = 10\text{ mH}$ , $R_G = 25\text{ }\Omega$ )			EAS	225	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			$T_L$	260	$^{\circ}\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction–to–Tab (Drain) – Steady State (Note 2)	$R_{\theta JC}$	14	$^\circ\text{C/W}$
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	65	
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	150	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1 in. pad size (Cu. area = 1.127 in<sup>2</sup> [1 oz] including traces)
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu. area = 0.341 in<sup>2</sup>)

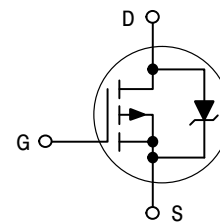


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$V_{(BR)DS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
–60 V	145 m $\Omega$ @ –10 V	–2.6 A

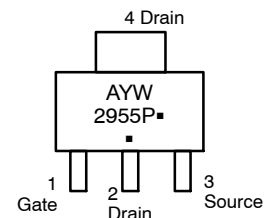
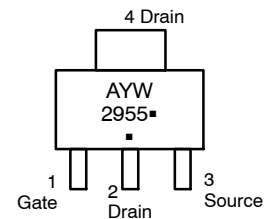
### P–Channel



### MARKING DIAGRAMS AND PIN ASSIGNMENT



SOT–223  
CASE 318E  
STYLE 3



A = Assembly Location  
Y = Year  
W = Work Week  
■ = Pb–Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTF2955T1	SOT–223	1000/Tape & Reel
NTF2955T1G	SOT–223 (Pb–Free)	1000/Tape & Reel
NTF2955PT1G	SOT–223 (Pb–Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTF2955, NTF2955P

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			66.4		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -60 V	T <sub>J</sub> = 25°C		-1.0	μA
			T <sub>J</sub> = 125°C		-50	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1.0 mA	-2.0		-4.0	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -0.75 A		145	170	mΩ
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.5 A		150	180	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.4 A		154	185	
Forward Transconductance	g <sub>FS</sub>	V <sub>GS</sub> = -15 V, I <sub>D</sub> = -0.75 A		1.77		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V		492		pF
Output Capacitance	C <sub>OSS</sub>			165		
Reverse Transfer Capacitance	C <sub>RSS</sub>			50		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 30 V, I <sub>D</sub> = 1.5 A		14.3		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.2		
Gate-to-Source Charge	Q <sub>GS</sub>			2.3		
Gate-to-Drain Charge	Q <sub>GD</sub>			5.2		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 25 V, I <sub>D</sub> = 1.5 A, R <sub>G</sub> = 9.1 Ω, R <sub>L</sub> = 25 Ω		11		ns
Rise Time	t <sub>r</sub>			7.6		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			65		
Fall Time	t <sub>f</sub>			38		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.5 A	T <sub>J</sub> = 25°C		-1.10	-1.30	V
			T <sub>J</sub> = 125°C		-0.9		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 1.5 A		36			ns
Charge Time	t <sub>a</sub>			20			
Discharge Time	t <sub>b</sub>			16			
Reverse Recovery Charge	Q <sub>RR</sub>			0.139			nC

3. Pulse Test: pulse width ≤ 300μs, duty cycle ≤ 2%.  
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

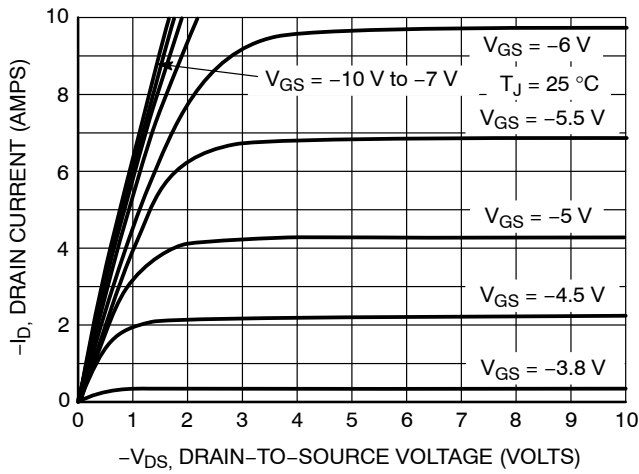


Figure 1. On-Region Characteristics

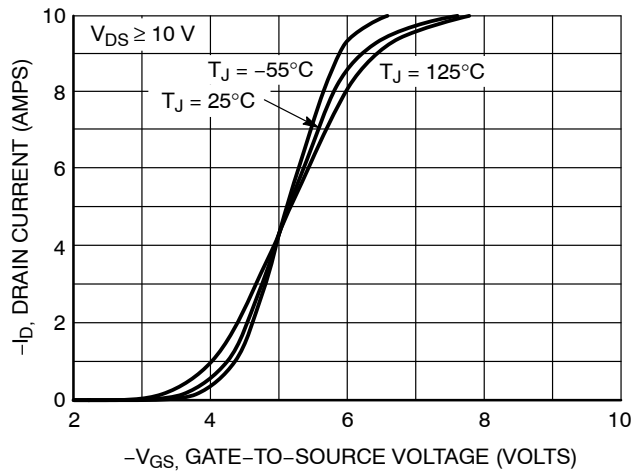


Figure 2. Transfer Characteristics

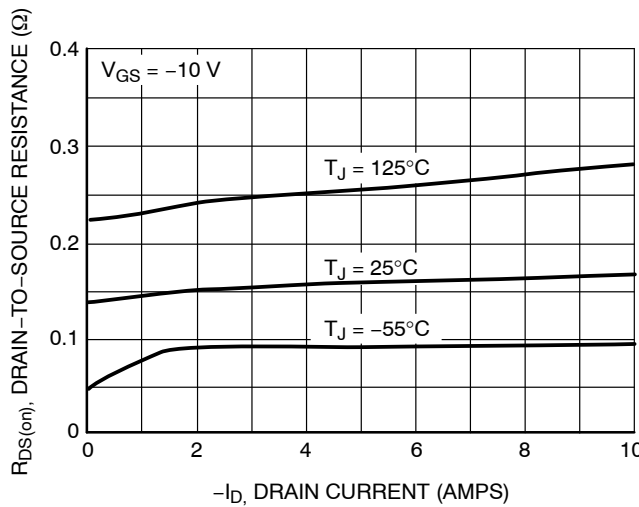


Figure 3. On-Resistance versus Drain Current and Temperature

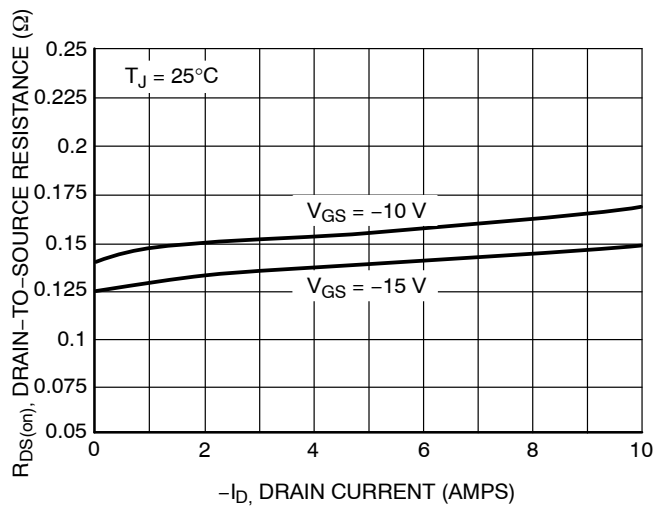


Figure 4. On-Resistance versus Drain Current and Gate Voltage

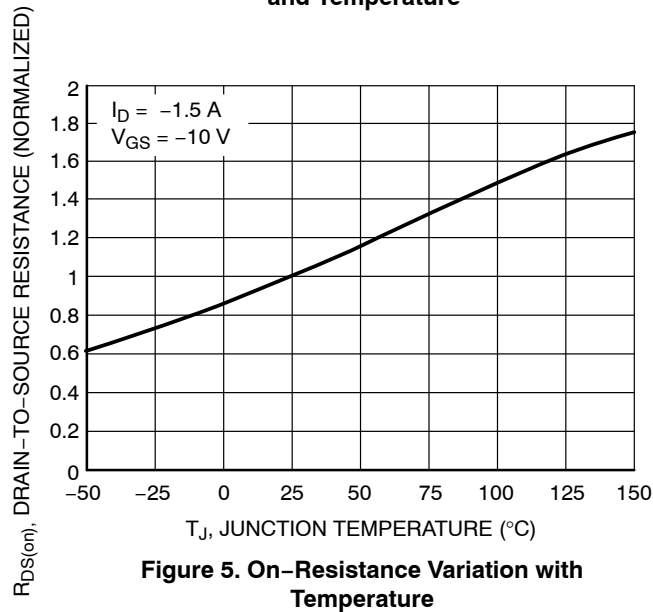


Figure 5. On-Resistance Variation with Temperature

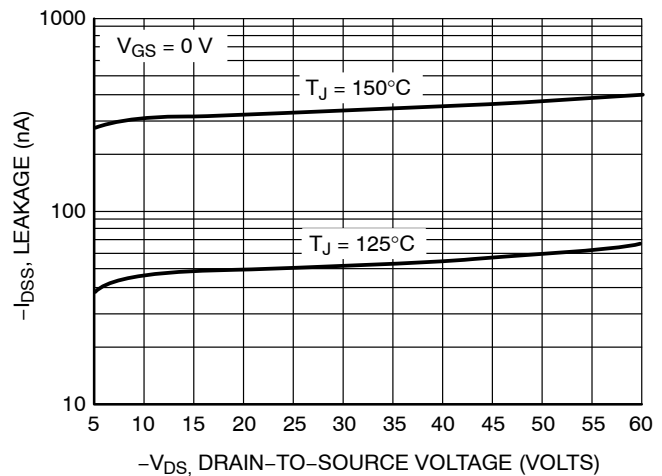


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

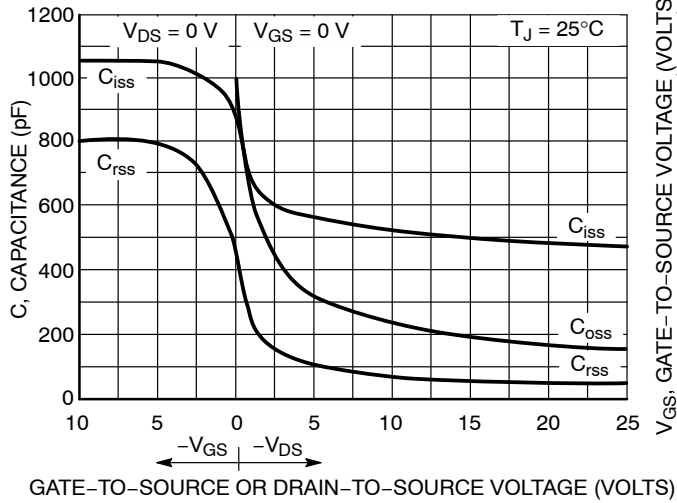


Figure 7. Capacitance Variation

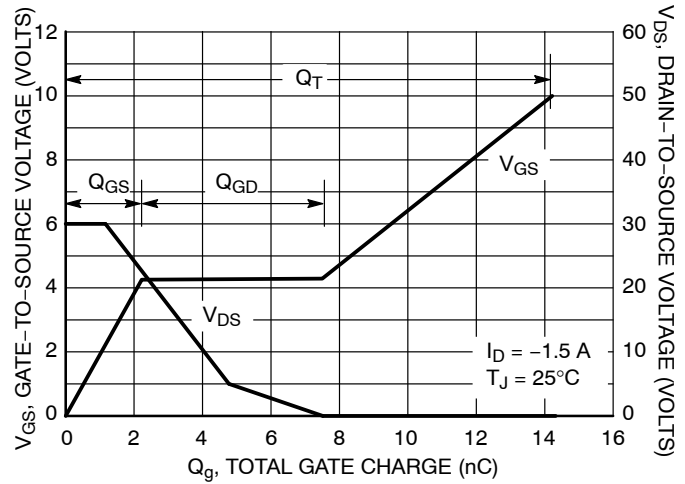


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

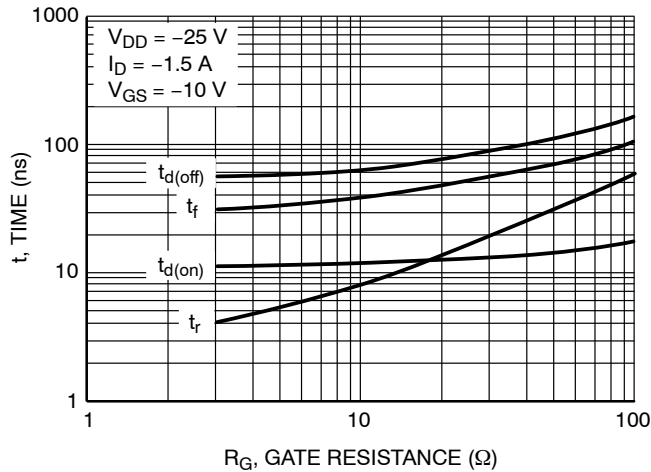


Figure 9. Resistive Switching Time Variation versus Gate Resistance

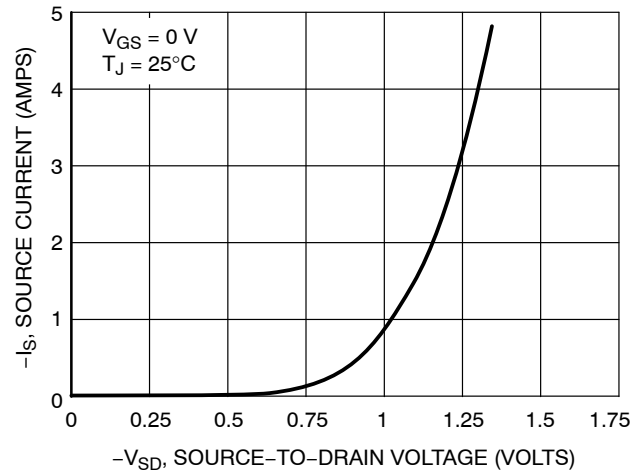


Figure 10. Diode Forward Voltage versus Current

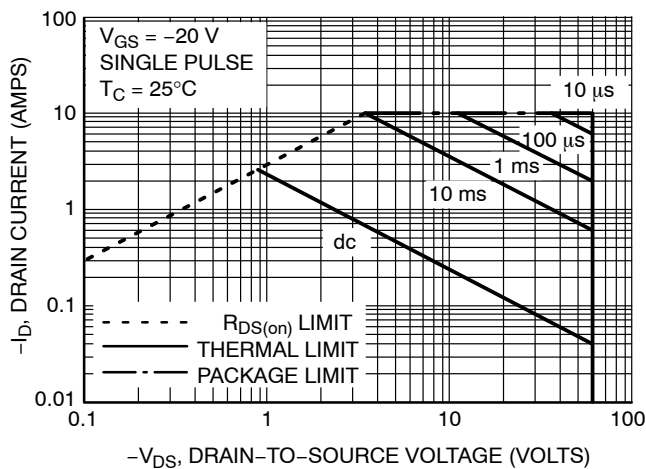


Figure 11. Maximum Rated Forward Biased Safe Operating Area

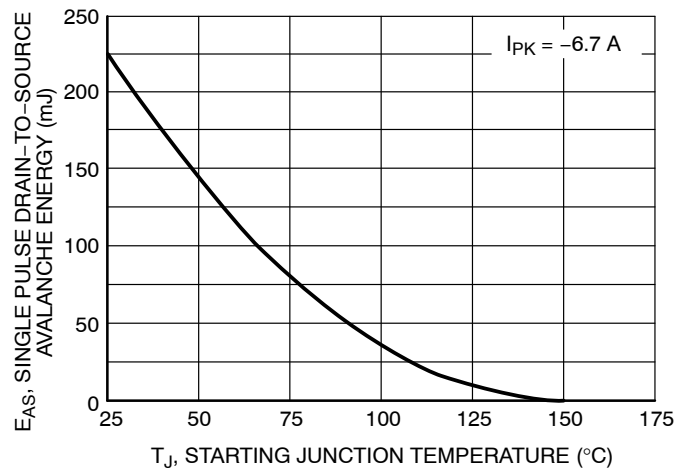
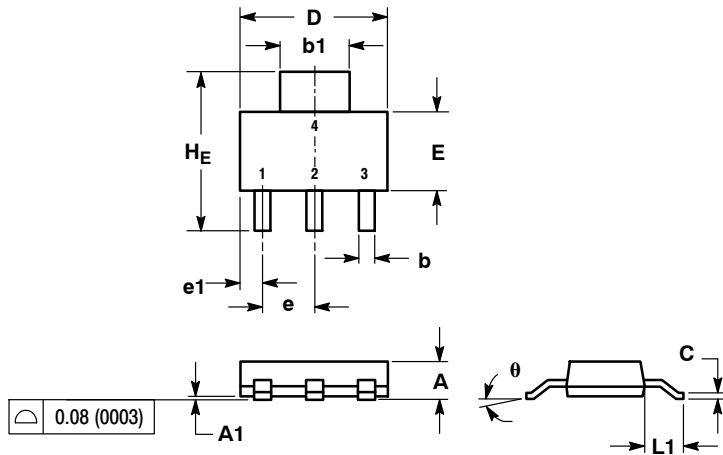


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

# NTF2955, NTF2955P

## PACKAGE DIMENSIONS

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE M



### NOTES:

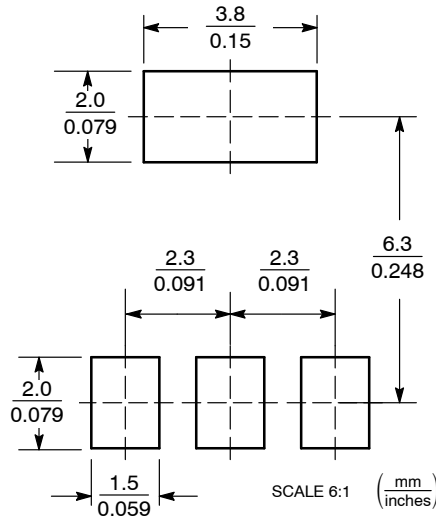
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H <sub>E</sub>	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	—	10°	0°	—	10°


### STYLE 3:

- PIN 1: GATE  
PIN 2: DRAIN  
PIN 3: SOURCE  
PIN 4: DRAIN

## SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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