

74AHC1G125; 74AHCT1G125

Bus buffer/line driver; 3-state

Rev. 07 — 5 July 2007

Product data sheet

1. General description

74AHC1G125 and 74AHCT1G125 are high-speed Si-gate CMOS devices. They provide one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (\overline{OE}). A HIGH at \overline{OE} causes the output to assume a high-impedance OFF-state.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. Features

- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- SOT353-1 and SOT753 package options
- ESD protection:
 - ◆ HBM JESD22-A114E: exceeds 2000 V
 - ◆ MM JESD22-A115-A: exceeds 200 V
 - ◆ CDM JESD22-C101C: exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G125GW 74AHCT1G125GW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHC1G125GV 74AHCT1G125GV	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SC-74A	plastic surface-mounted package; 5 leads	SOT753

4. Marking

Table 2. Marking codes

Type number	Marking
74AHC1G125GW	AM
74AHC1G125GV	A25
74AHCT1G125GW	CM
74AHCT1G125GV	C25

5. Functional diagram

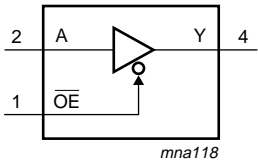


Fig 1. Logic symbol

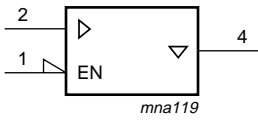


Fig 2. IEC logic symbol

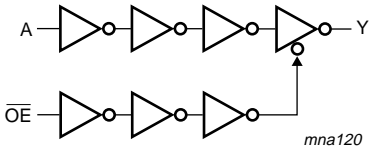


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

74AHC1G125
74AHCT1G125

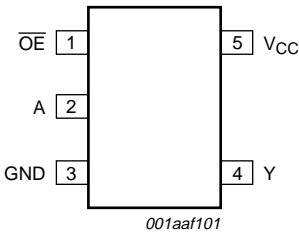


Fig 4. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
OE	1	data input
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Inputs		Output
OE	A	Y
L	L	L
L	H	H
H	X	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -	±20	mA
I_O	output current	-0.5 V < V_O < $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For both TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC1G125			74AHCT1G125			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHC1G125										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = –50 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = –50 µA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = –50 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = –8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF
For type 74AHCT1G125										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = –50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V

Table 7. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	0.25	-	2.5	-	10	μ A
I_I	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μ A
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.0	-	10	-	40	μ A
ΔI_{CC}	additional supply current	per input pin; $V_I = 3.4$ V; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics
 $GND = 0$ V; $t_r = t_f = \leq 3.0$ ns. For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	

For type 74AHC1G125

t_{pd}	propagation delay	A to Y; see Figure 5 [1]								
		$V_{CC} = 3.0$ V to 3.6 V [2]								
		$C_L = 15$ pF	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50$ pF	-	6.6	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5$ V to 5.5 V [3]								
		$C_L = 15$ pF	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
t_{en}	enable time	\overline{OE} to Y; see Figure 6 [1]								
		$V_{CC} = 3.0$ V to 3.6 V [2]								
		$C_L = 15$ pF	-	5.0	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50$ pF	-	6.9	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5$ V to 5.5 V [3]								
		$C_L = 15$ pF	-	3.6	5.1	1.0	6.0	1.0	6.5	ns
t_{dis}	disable time	\overline{OE} to Y; see Figure 6 [1]								
		$V_{CC} = 3.0$ V to 3.6 V [2]								
		$C_L = 15$ pF	-	6.0	9.7	1.0	11.5	1.0	12.5	ns
		$C_L = 50$ pF	-	8.3	13.2	1.0	15.0	1.0	16.5	ns
		$V_{CC} = 4.5$ V to 5.5 V [3]								
		$C_L = 15$ pF	-	4.1	6.8	1.0	8.0	1.0	8.5	ns
		$C_L = 50$ pF	-	5.7	8.8	1.0	10.0	1.0	11.0	ns

Table 8. Dynamic characteristics ...continuedGND = 0 V; $t_r = t_f \leq 3.0$ ns. For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$	[4]	-	9	-	-	-	-	pF
For type 74AHCT1G125										
t_{pd}	propagation delay	A to Y; see Figure 5	[1]							
		$V_{CC} = 4.5$ V to 5.5 V	[3]							
		$C_L = 15$ pF	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50$ pF	-	4.8	7.5	1.0	8.5	1.0	9.5	ns
t_{en}	enable time	\overline{OE} to Y; see Figure 6	[1]							
		$V_{CC} = 4.5$ V to 5.5 V	[3]							
		$C_L = 15$ pF	-	3.9	5.1	1.0	6.0	1.0	6.5	ns
		$C_L = 50$ pF	-	5.1	7.5	1.0	8.5	1.0	9.5	ns
t_{dis}	disable time	\overline{OE} to Y; see Figure 6	[1]							
		$V_{CC} = 4.5$ V to 5.5 V	[3]							
		$C_L = 15$ pF	-	4.5	6.8	1.0	8.0	1.0	8.5	ns
		$C_L = 50$ pF	-	6.1	8.8	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$	[4]	-	11	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} . t_{en} is the same as t_{PZL} and t_{PZH} . t_{dis} is the same as t_{PLZ} and t_{PHZ} .[2] Typical values are measured at $V_{CC} = 3.3$ V.[3] Typical values are measured at $V_{CC} = 5.0$ V.[4] C_{PD} is used to determine the dynamic power dissipation P_D (μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{CC} = supply voltage in Volts.

12. Waveforms

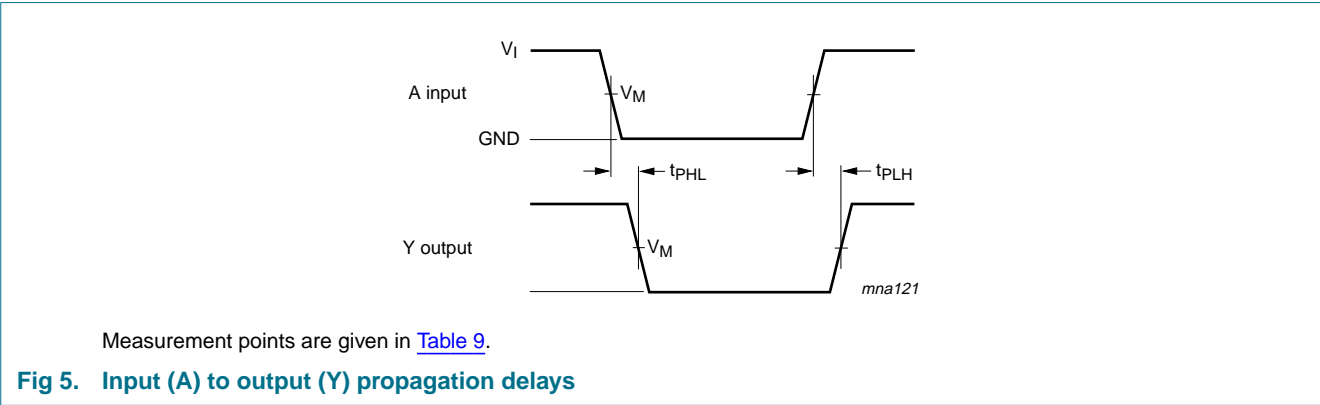
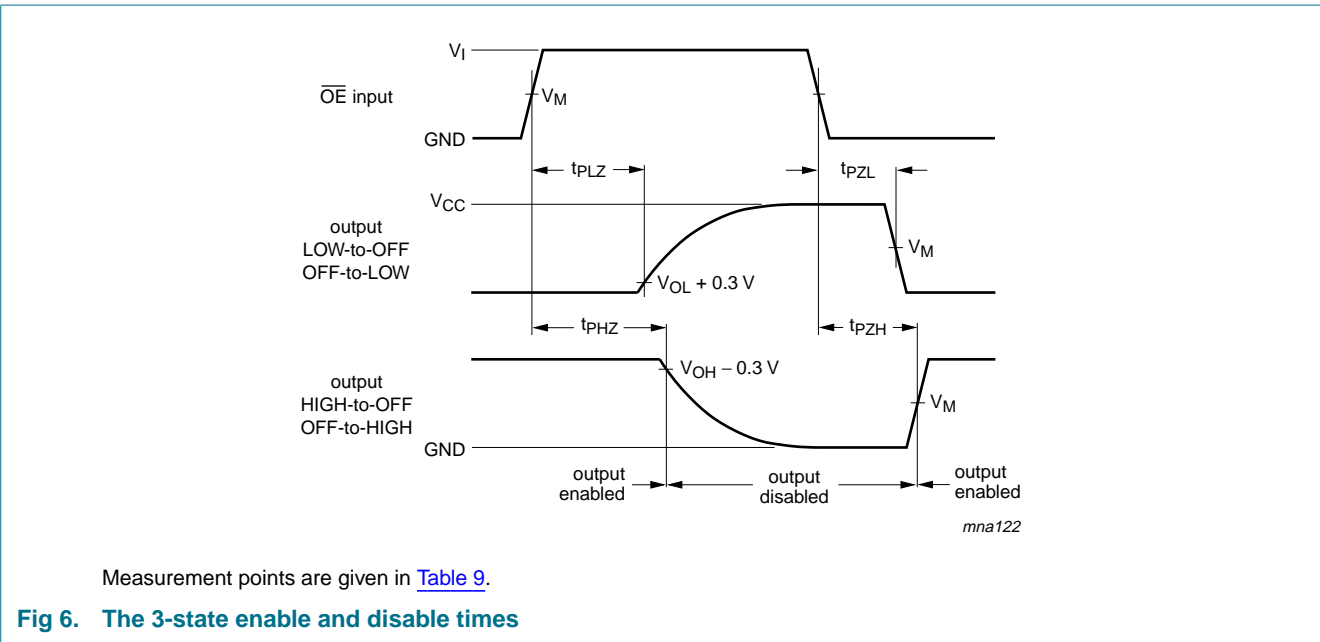
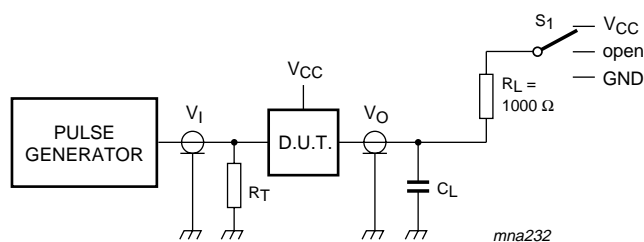


Table 9. Measurement point

Type	Inputs		Output
	V _I	V _M	V _M
74AHC1G125	GND to V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}
74AHCT1G125	GND to 3.0 V	1.5 V	0.5 × V _{CC}





Test data is given in [Table 8](#). Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

For t_{PLH} , t_{PHL} , S_1 = open

For t_{PLZ} , t_{PZL} , S_1 = V_{CC}

For t_{PHZ} , t_{PZH} , S_1 = GND

Fig 7. Load circuitry for switching times

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mmSOT353-1

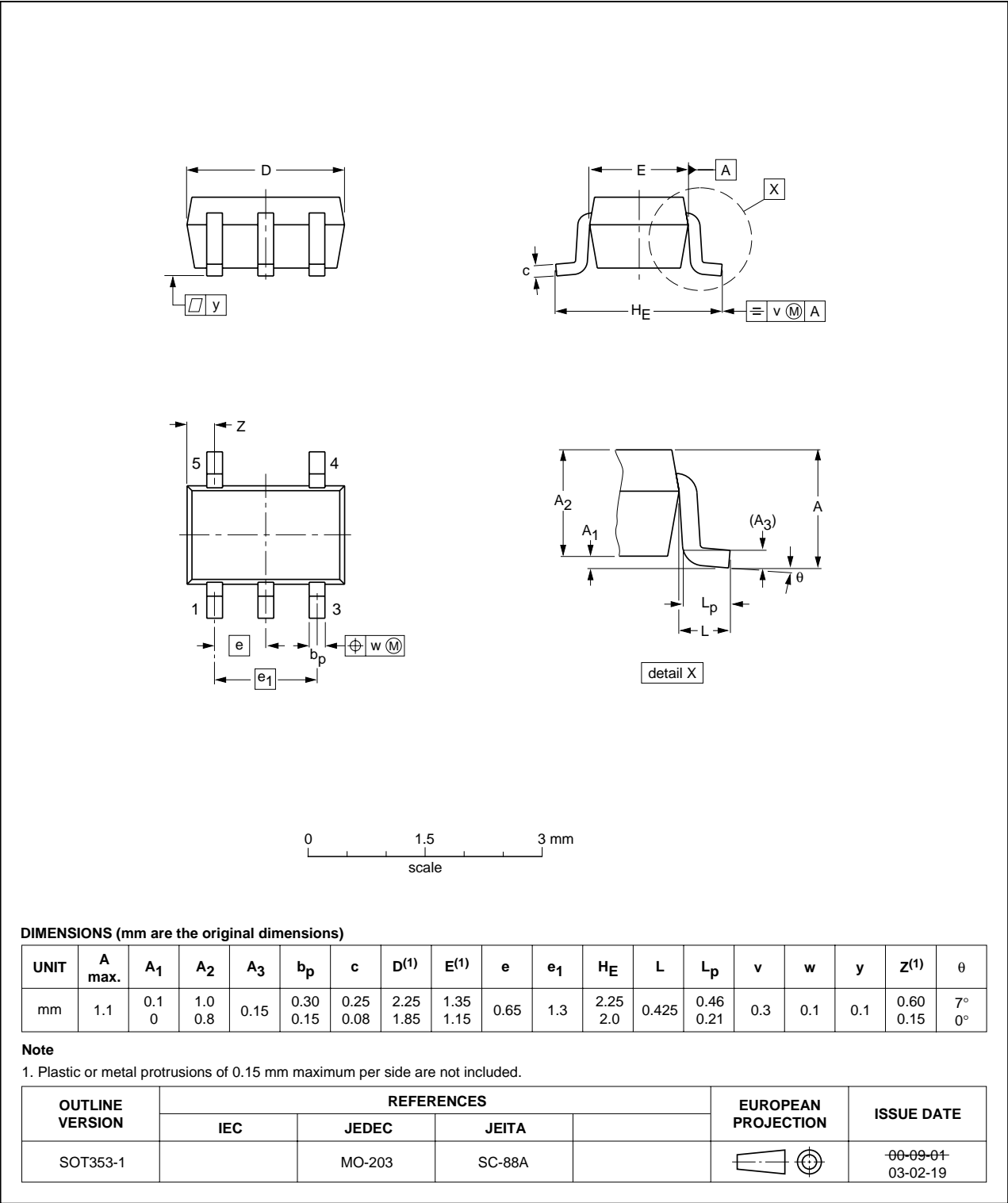


Fig 8. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

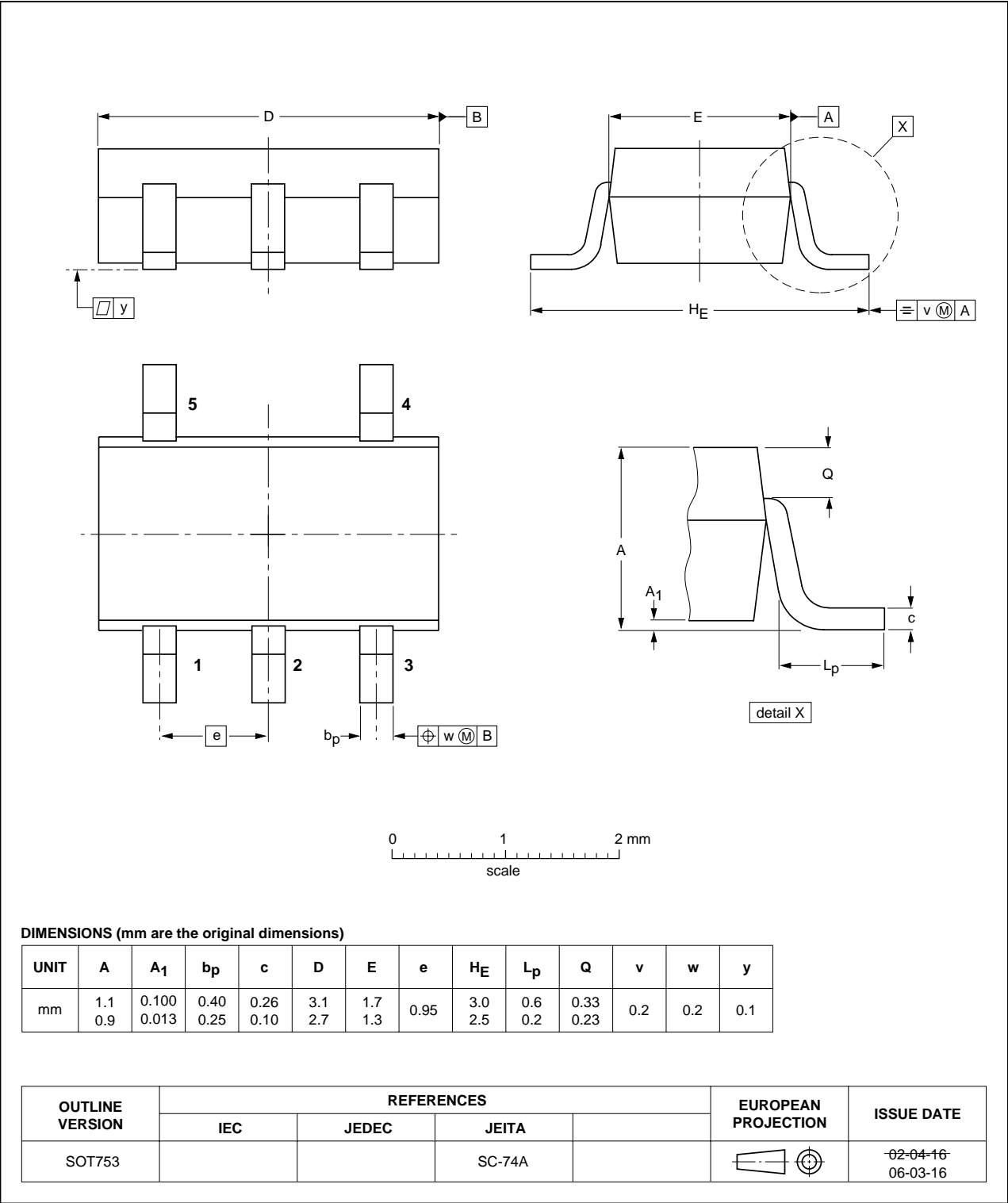


Fig 9. Package outline SOT753 (SC-74A)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G125_7	20070705	Product data sheet	-	74AHC_AHCT1G125_6
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Package SOT353 changed to SOT353-1 in Section 3 and Section 13.• Quick reference data and Soldering sections removed.			
74AHC_AHCT1G125_6	20020606	Product specification	-	74AHC_AHCT1G125_5
74AHC_AHCT1G125_5	20020322	Product specification	-	74AHC_AHCT1G125_4
74AHC_AHCT1G125_4	20010222	Product specification	-	74AHC_AHCT1G125_3
74AHC_AHCT1G125_3	19990615	Product specification	-	74AHC_AHCT1G125_N_2
74AHC_AHCT1G125_N_2	19981207	Preliminary specification	-	74AHC_AHCT1G125_N_1
74AHC_AHCT1G125_N_1	19981125	Preliminary specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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