

74LV08

Quad 2-input AND gate

Rev. 03 — 6 April 2009

Product data sheet

1. General description

The 74LV08 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC08 and 74HCT08.

The 74LV08 provides a quad 2-input AND function.

2. Features

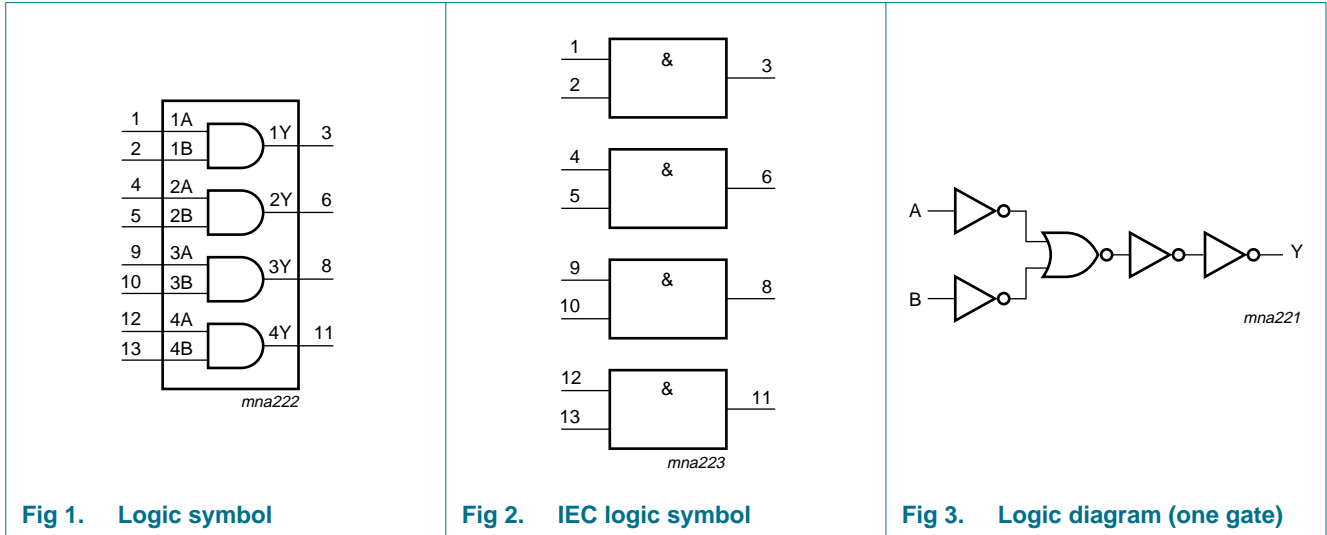
- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical output ground bounce < 0.8 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

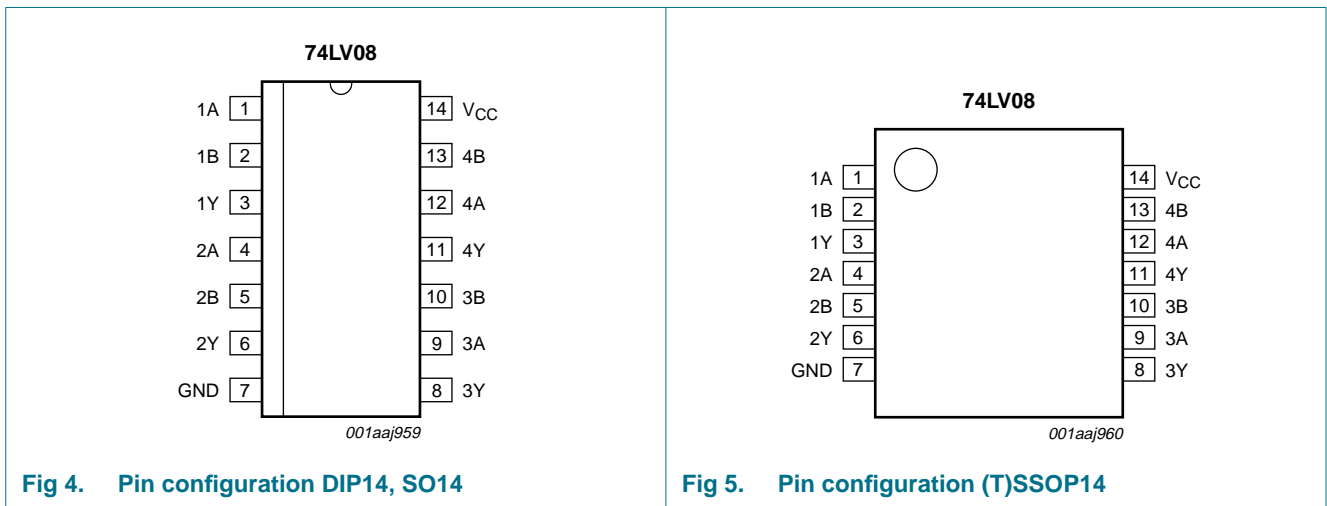
| Type number | Package | | | |
|-------------|-------------------|---------|---|----------|
| | Temperature range | Name | Description | Version |
| 74LV08N | -40 °C to +125 °C | DIP14 | plastic dual in-line package; 14 leads (300 mil) | SOT27-1 |
| 74LV08D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LV08DB | -40 °C to +125 °C | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74LV08PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------|----------------|
| 1A, 2A, 3A, 4A | 1, 4, 9, 12 | data input |
| 1B, 2B, 3B, 4B | 2, 5, 10, 13 | data input |
| 1Y, 2Y, 3Y, 4Y | 3, 6, 8, 11 | data output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function selection^[1]

| Input | | Output |
|-------|----|--------|
| nA | nB | nY |
| L | X | L |
| X | L | L |
| H | H | H |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|-------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7.0 | V |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V | [1] - | ±20 | mA |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{CC} + 0.5 V | [1] - | ±50 | mA |
| I _O | output current | V _O = -0.5 V to (V _{CC} + 0.5 V) | - | ±25 | mA |
| I _{CC} | supply current | | - | 50 | mA |
| I _{GND} | ground current | | -50 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C | [2] | | |
| | | DIP14 package | - | 750 | mW |
| | | SO14, SSOP14, TSSOP14 | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP14 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
 For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---|-----|-----|----------|------|
| V_{CC} | supply voltage ^[1] | | 1.0 | 3.3 | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.0\text{ V to }2.0\text{ V}$ | - | - | 500 | ns/V |
| | | $V_{CC} = 2.0\text{ V to }2.7\text{ V}$ | - | - | 200 | ns/V |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | - | - | 100 | ns/V |
| | | $V_{CC} = 3.6\text{ V to }5.5\text{ V}$ | - | - | 50 | ns/V |

[1] The static characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$, but LV devices are guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|----------|---------------------------|--|------------------|--------------------|-------------|-------------------|-------------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.2\text{ V}$ | 0.9 | - | - | 0.9 | - | V |
| | | $V_{CC} = 2.0\text{ V}$ | 1.4 | - | - | 1.4 | - | V |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $0.7V_{CC}$ | - | - | $0.7V_{CC}$ | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.2\text{ V}$ | - | - | 0.3 | - | 0.3 | V |
| | | $V_{CC} = 2.0\text{ V}$ | - | - | 0.6 | - | 0.6 | V |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | |
| | | $I_O = -100\ \mu\text{A}; V_{CC} = 1.2\text{ V}$ | - | 1.2 | - | - | - | V |
| | | $I_O = -100\ \mu\text{A}; V_{CC} = 2.0\text{ V}$ | 1.8 | 2.0 | - | 1.8 | - | V |
| | | $I_O = -100\ \mu\text{A}; V_{CC} = 2.7\text{ V}$ | 2.5 | 2.7 | - | 2.5 | - | V |
| | | $I_O = -100\ \mu\text{A}; V_{CC} = 3.0\text{ V}$ | 2.8 | 3.0 | - | 2.8 | - | V |
| | | $I_O = -100\ \mu\text{A}; V_{CC} = 4.5\text{ V}$ | 4.3 | 4.5 | - | 4.3 | - | V |
| | | $I_O = -6\text{ mA}; V_{CC} = 3.0\text{ V}$ | 2.4 | 2.82 | - | 2.2 | - | V |
| | | $I_O = -12\text{ mA}; V_{CC} = 4.5\text{ V}$ | 3.6 | 4.2 | - | 3.5 | - | V |

Table 6. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|------------------|--------------------|------|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 100 μA; V _{CC} = 1.2 V | - | 0 | - | - | - | V |
| | | I _O = 100 μA; V _{CC} = 2.0 V | - | 0 | 0.2 | - | 0.2 | V |
| | | I _O = 100 μA; V _{CC} = 2.7 V | - | 0 | 0.2 | - | 0.2 | V |
| | | I _O = 100 μA; V _{CC} = 3.0 V | - | 0 | 0.2 | - | 0.2 | V |
| | | I _O = 100 μA; V _{CC} = 4.5 V | - | 0 | 0.2 | - | 0.2 | V |
| | | I _O = 6 mA; V _{CC} = 3.0 V | - | 0.25 | 0.40 | - | 0.50 | V |
| | | I _O = 12 mA; V _{CC} = 4.5 V | - | 0.35 | 0.55 | - | 0.65 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | 1.0 | - | 1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 20.0 | - | 40 | μA |
| ΔI _{CC} | additional supply current | per input; V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V | - | - | 500 | - | 850 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics
 GND = 0 V; For test circuit see [Figure 7](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|--|------------------|--------------------|-----|-------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| t _{pd} | propagation delay | nA, nB to nY; see Figure 6 ^[2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 45 | - | - | - | ns |
| | | V _{CC} = 2.0 V | - | 15 | 26 | - | 33 | ns |
| | | V _{CC} = 2.7 V | - | 11 | 17 | - | 21 | ns |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF ^[3] | - | 7 | - | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V ^[3] | - | 9.0 | 15 | - | 19 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 11 | - | 14 | ns |
| C _{PD} | power dissipation capacitance | C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} ^[4] | - | 10 | - | - | - | pF |

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz, f_o = output frequency in MHz

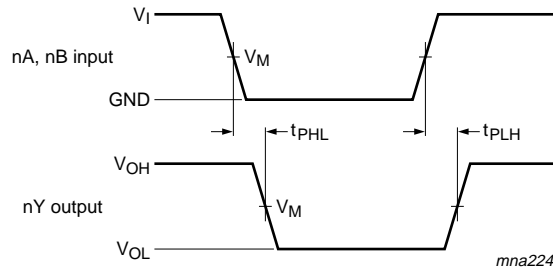
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11. Waveforms

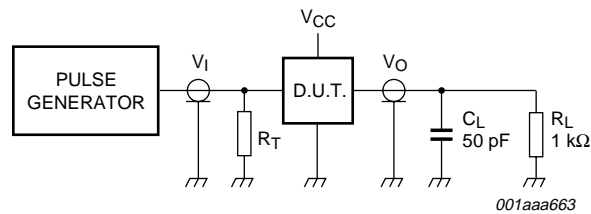


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. The input (nA, nB) to output (nY) propagation delays

Table 8. Measurement points

| Supply voltage | Input | Output |
|----------------|-------------|-------------|
| V_{CC} | V_M | V_M |
| < 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 2.7 V to 3.6 V | 1.5 V | 1.5 V |
| ≥ 4.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ |



Test data is given in [Table 9](#).
 Definitions test circuit:
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.

Fig 7. Load circuit for switching times

Table 9. Test data

| Supply voltage | Input | t_r, t_f |
|----------------|----------|---------------|
| V_{CC} | V_I | t_r, t_f |
| < 2.7 V | V_{CC} | ≤ 2.5 ns |
| 2.7 V to 3.6 V | 2.7 V | ≤ 2.5 ns |
| ≥ 4.5 V | V_{CC} | ≤ 2.5 ns |

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

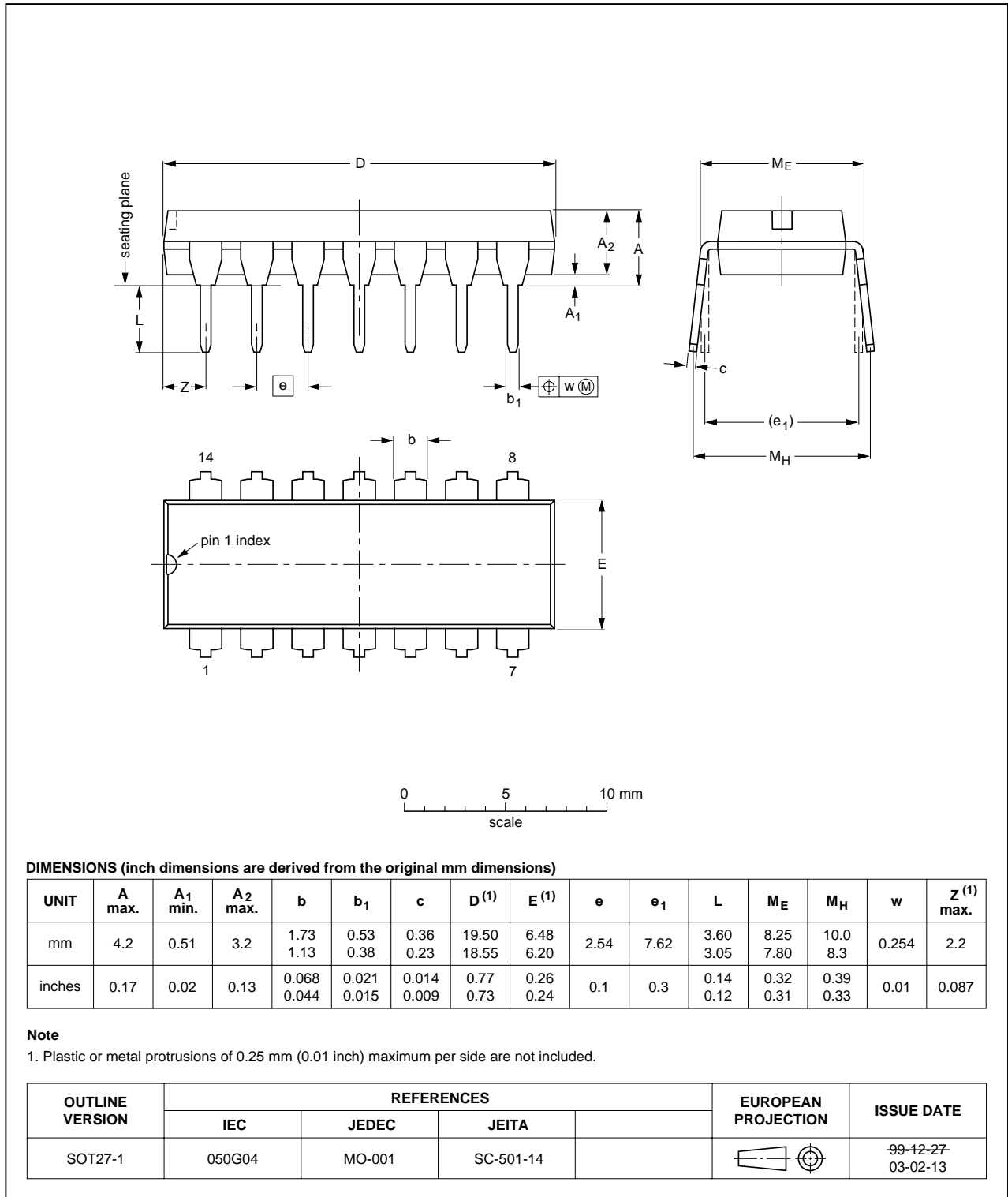


Fig 8. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

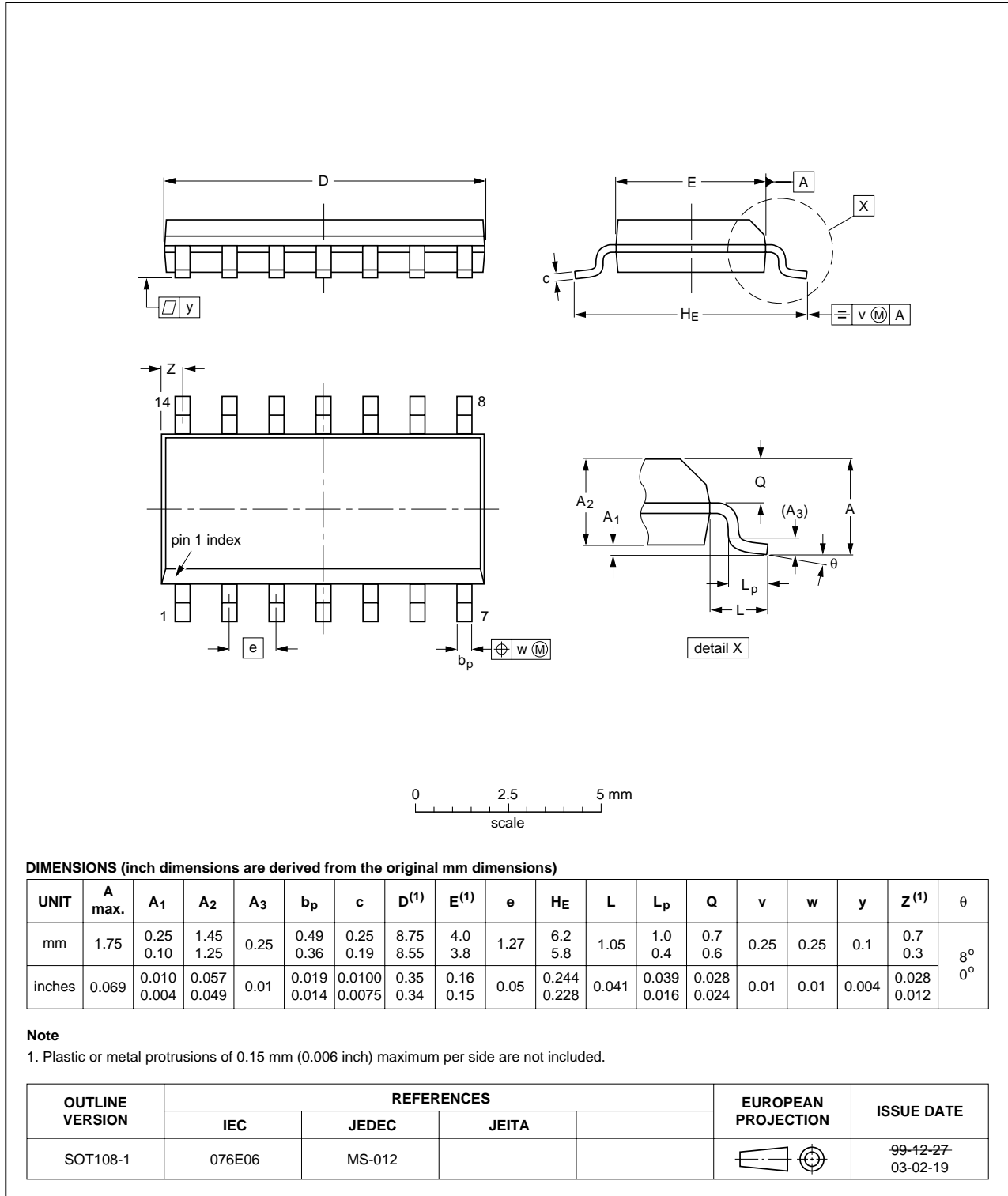


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

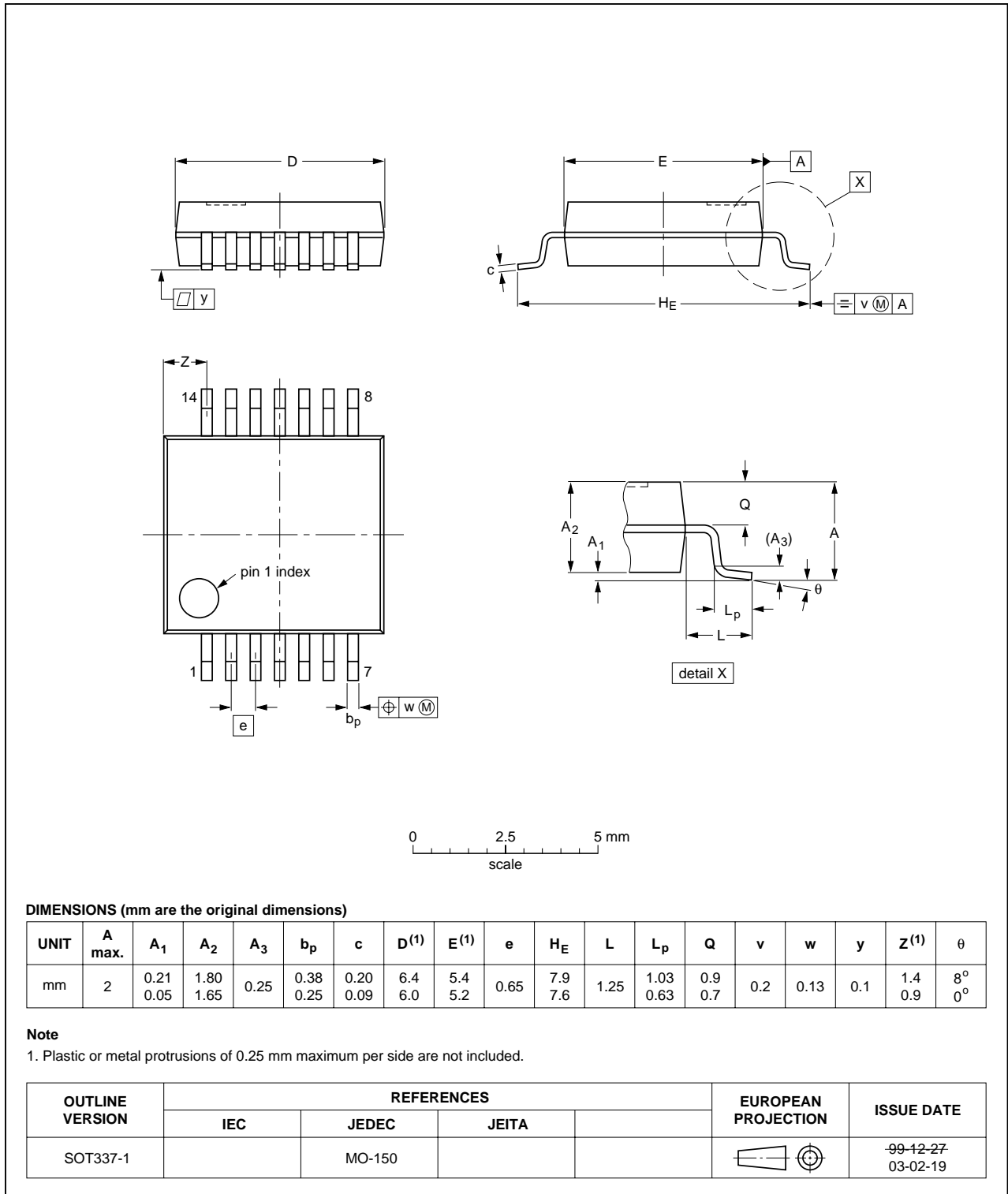


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

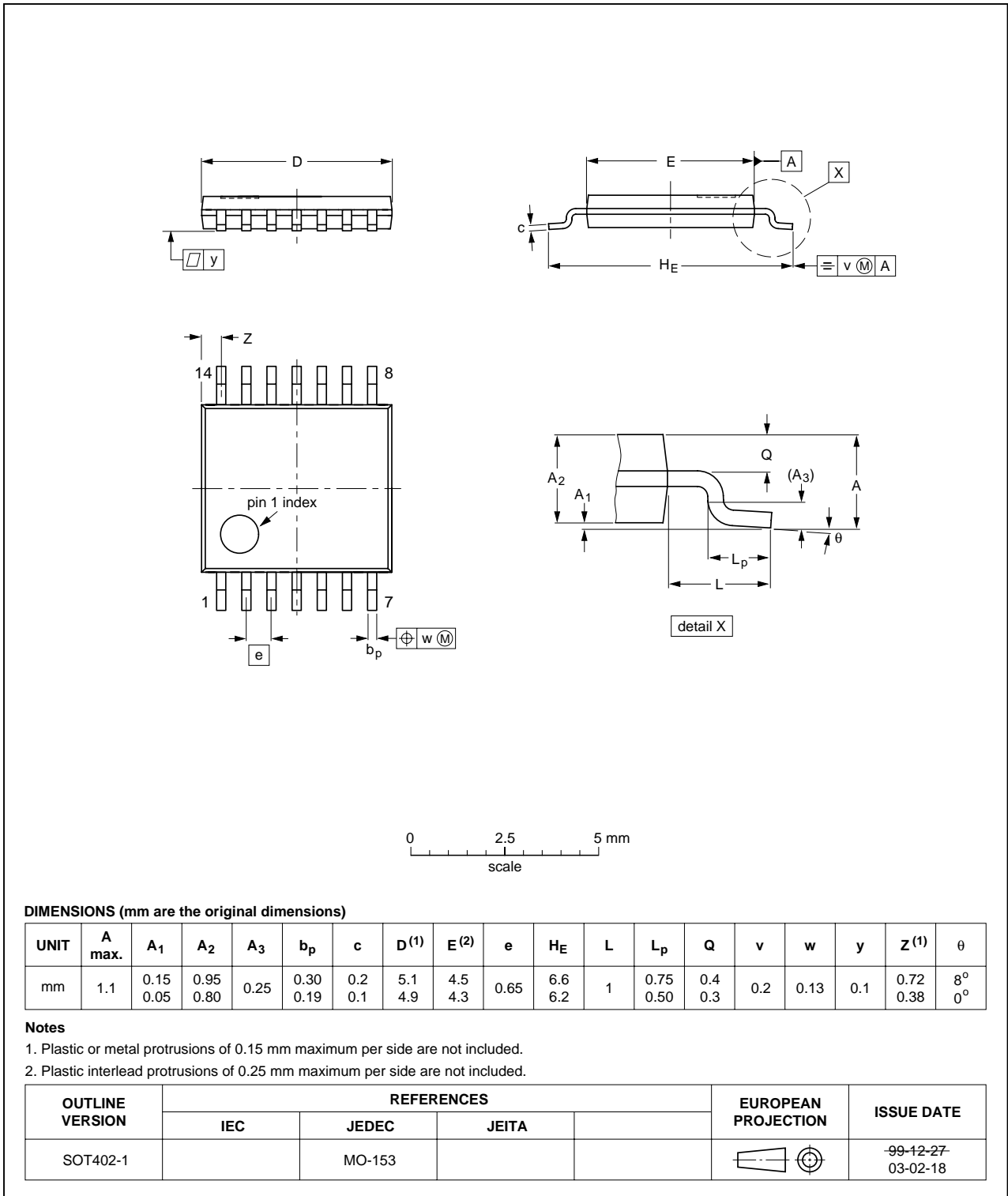


Fig 11. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|-----------------------|---------------|------------|
| 74LV08_3 | 20090406 | Product data sheet | - | 74LV08_2 |
| Modifications: | <ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name when appropriate. | | | |
| 74LV08_2 | 19980420 | Product specification | - | 74LV08_1 |
| 74LV08_1 | 19970203 | Product specification | - | - |

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15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 6 April 2009

Document identifier: 74LV08_3