DATA SHEET

74LVT2952

3.3 V LVT octal registered transceiver (3-State)

Product data sheet
Supersedes data of 1998 Feb 19
IC23 Data Handbook

2004 Sep 07

Philips
Semiconductors

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3.3 V Octal registered transceiver (3-State) 74LVT2952

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64 mA/–32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The LVT2952 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses.

Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

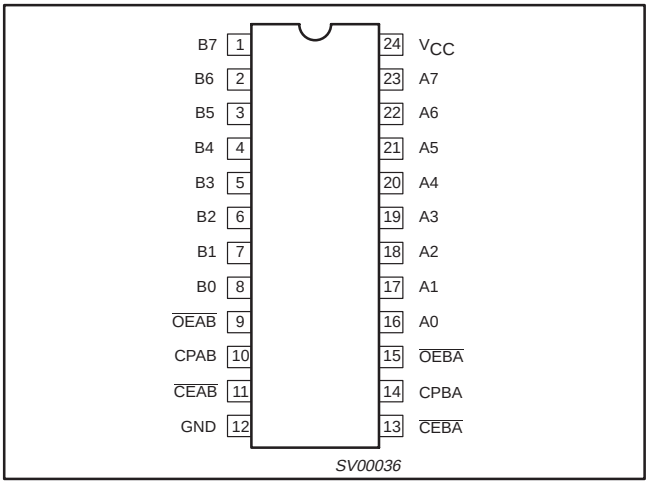
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50 pF; V_{CC} = 3.3 V	3.1 3.8	ns
C_{IN}	Input capacitance	V_I = 0 V or 3.0 V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0 V or 3.0 V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6 V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	TYPE NUMBER	DWG NUMBER
24-Pin Plastic SOL	–40 °C to +85 °C	74LVT2952D	SOT137-1
24-Pin Plastic SSOP Type II	–40 °C to +85 °C	74LVT2952DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40 °C to +85 °C	74LVT2952PW	SOT355-1

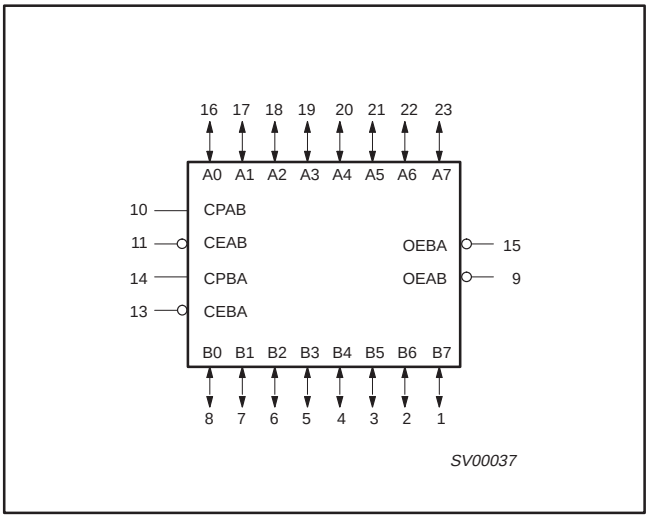
PIN CONFIGURATION



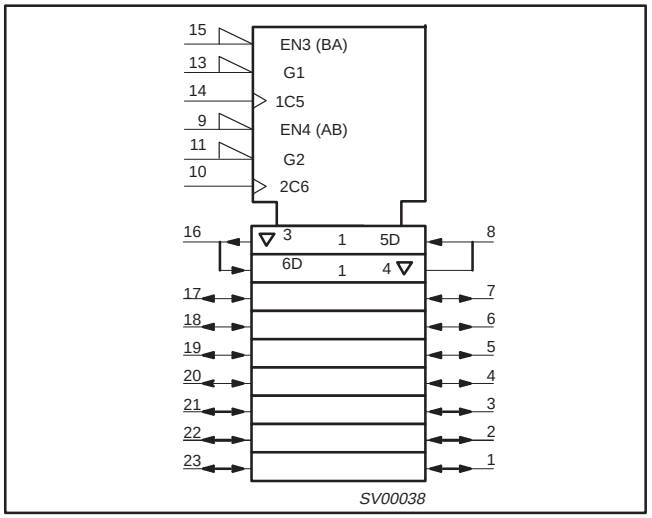
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
8, 7, 6, 5, 4, 3, 2, 1	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Output enable inputs
12	GND	Ground (0 V)
24	V_{CC}	Positive supply voltage

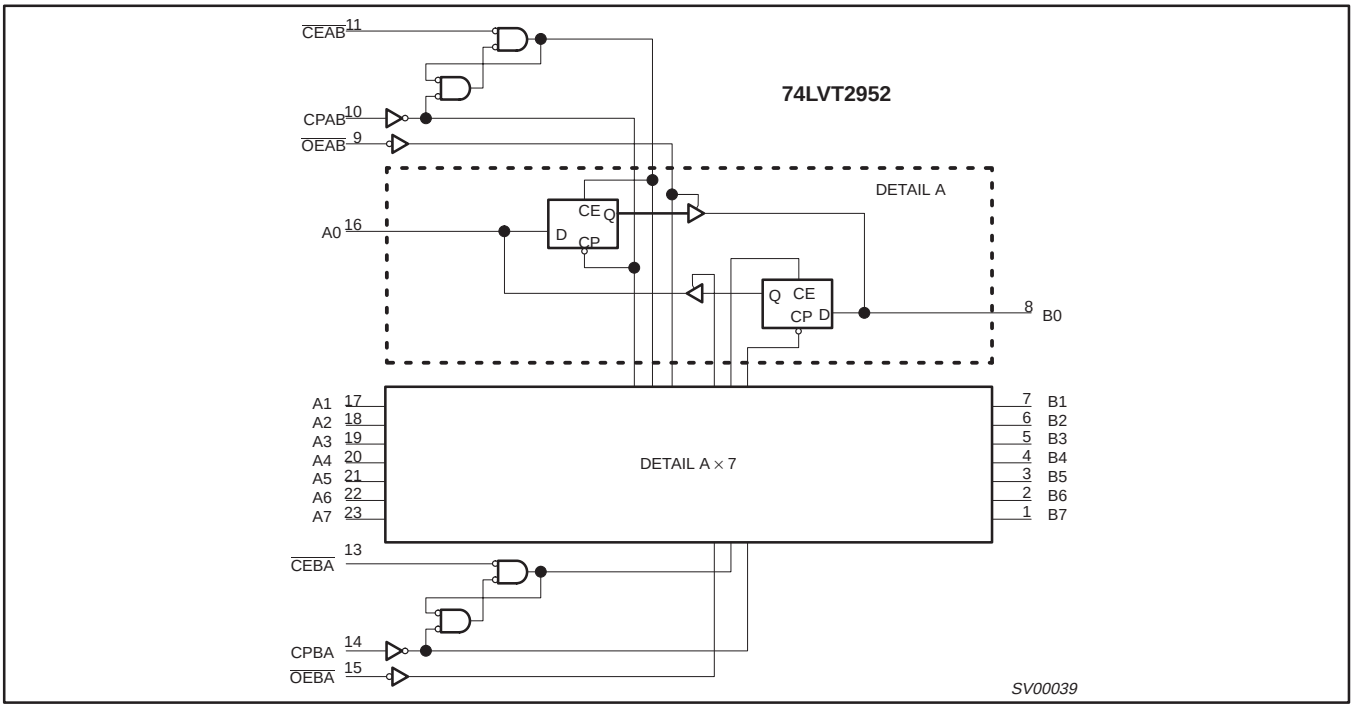
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OEXX}$			
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = HIGH voltage level
L = LOW voltage level
X = Don't care
XX = AB or BA
Z = High-impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$ V	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or HIGH state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in HIGH state	–64	mA
		Output in LOW state	128	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	LOW-level Input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	–32	mA
I_{OL}	LOW-level output current	–	32	mA
	LOW-level output current; current duty cycle ≤ 50 %, f ≥ 1 kHz	–	64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	–	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = –40 °C to +85 °C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA		–	–0.9	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = –100 µA		V_{CC} – 0.2	V_{CC} – 0.1	–	V
		V_{CC} = 2.7 V; I_{OH} = –8 mA		2.4	2.5	–	
		V_{CC} = 3.0 V; I_{OH} = –32 mA		2.0	2.2	–	
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 µA		–	0.1	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA		–	0.3	0.5	
		V_{CC} = 3.0 V; I_{OL} = 16 mA		–	0.25	0.4	
		V_{CC} = 3.0 V; I_{OL} = 32 mA		–	0.3	0.5	
		V_{CC} = 3.0 V; I_{OL} = 64 mA		–	0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6 V; I_O = 1 mA; V_I = GND or V_{CC}		–	0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND	Control pins	–	± 0.1	± 1.0	µA
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		–	1	10	
		V_{CC} = 3.6 V; V_I = 5.5 V	I/O Data pins[4]	–	1	20	
		V_{CC} = 3.6 V; V_I = V_{CC}		–	0.1	1.0	
		V_{CC} = 3.6 V; V_I = 0 V		–	–1	–5.0	
I_{OFF}	Output off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		–	1	± 100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3 V; V_I = 0.8 V		75	150	–	µA
		V_{CC} = 3 V; V_I = 2.0 V		–75	–150	–	
		V_{CC} = 0 V to 3.6 V; V_{CC} = 3.6 V		± 500	–	–	
I_{EX}	Current into an output in the HIGH state when $V_O > V_{CC}$	V_O = 5.5 V; V_{CC} = 3.0 V		–	60	125	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]	$V_{CC0} \leq$ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care		–	± 1	± 100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6 V; Outputs HIGH, V_I = GND or V_{CC}; I_O = 0 mA		–	0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6 V; Outputs LOW, V_I = GND or V_{CC}; I_O = 0 mA		–	3	12	
I_{CCZ}		V_{CC} = 3.6 V; Outputs Disabled; V_I = GND or V_{CC}; I_O = 0 mA		–	0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3 V to 3.6 V; One input at V_{CC} – 0.6 V; Other inputs at V_{CC} or GND		–	0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. This is the increase in supply current for each input at V_{CC} = 0.6 V.
3. This parameter is valid for any V_{CC} between 0 V and 1.3 V with a transition time of up to 10 msec. From V_{CC} = 1.3 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µsec is permitted. This parameter is valid for T_{amb} = 25 °C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF, R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	200			MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	1	1.3 1.8	3.1 3.8	6.1 6.0	7.1 6.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	3 4	1.0 1.2	3.4 3.6	5.6 6.5	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	3 4	1.0 1.6	3.7 3.4	6.3 5.1	6.9 5.3	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

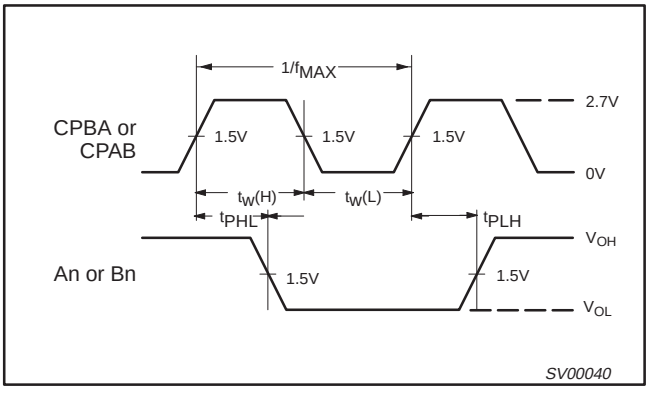
AC SETUP REQUIREMENTS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF, R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

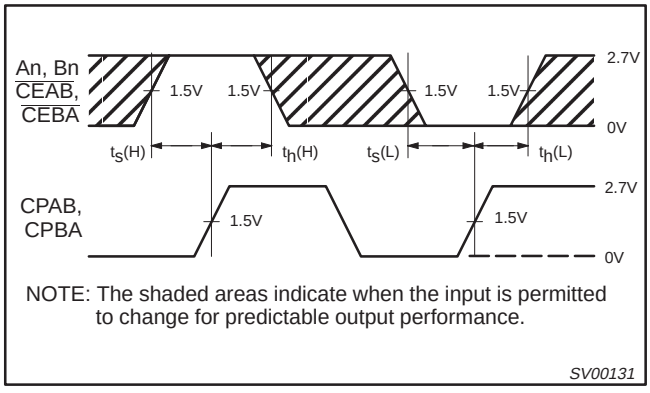
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	
			MIN	TYP[1]	MIN	
$t_s(H)$ $t_s(L)$	Setup time An to CPAB or Bn to CPBA	2	2.5 2.5	1 1	2.8 3.0	ns
$t_n(H)$ $t_n(L)$	Hold time An to CPAB ro Bn to CPBA	2	1.5 1.5	–0.5 –0.5	0.7 2.6	ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA	2	0.9 2.4	0.3 –0.3	0.8 2.7	ns
$t_n(H)$ $t_n(L)$	Hold time $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA	2	2.5 2.5	0.3 0	0.7 2.6	ns
$t_W(H)$ $t_W(L)$	CPAB or CPBA pulse width High or Low	1	3.3 3.3	1 1	3.3 3.3	ns

AC WAVEFORMS

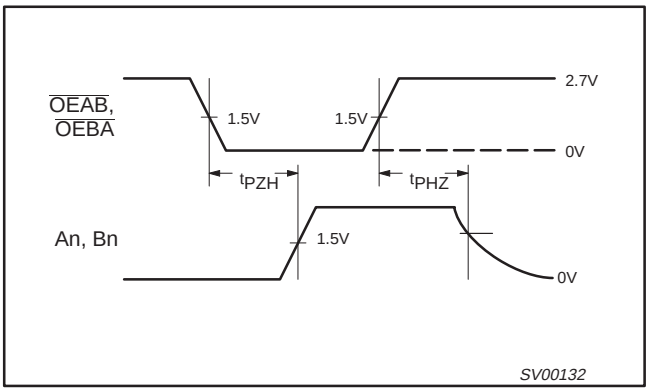
V_M = 1.5 V, V_{IN} = GND to 2.7 V



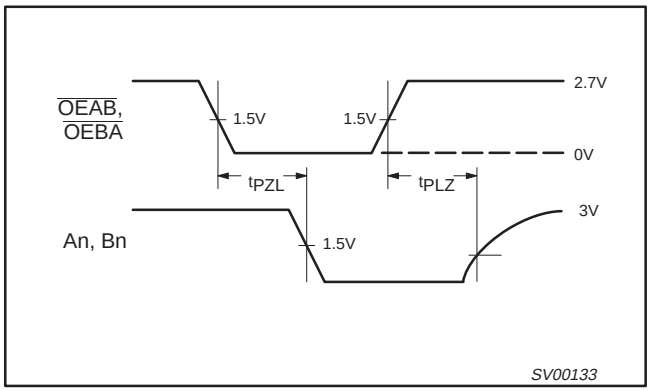
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

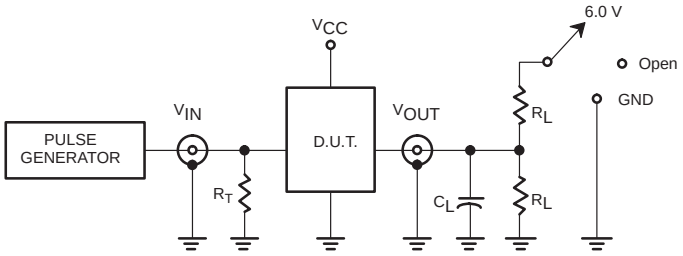


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

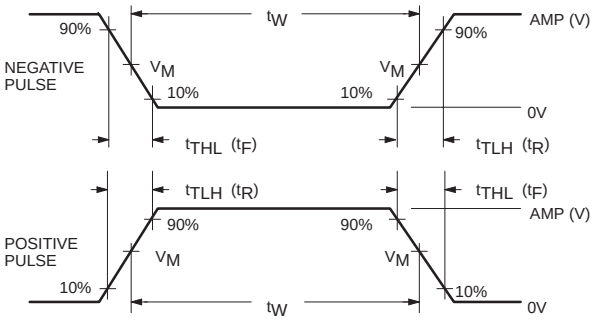


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5 V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

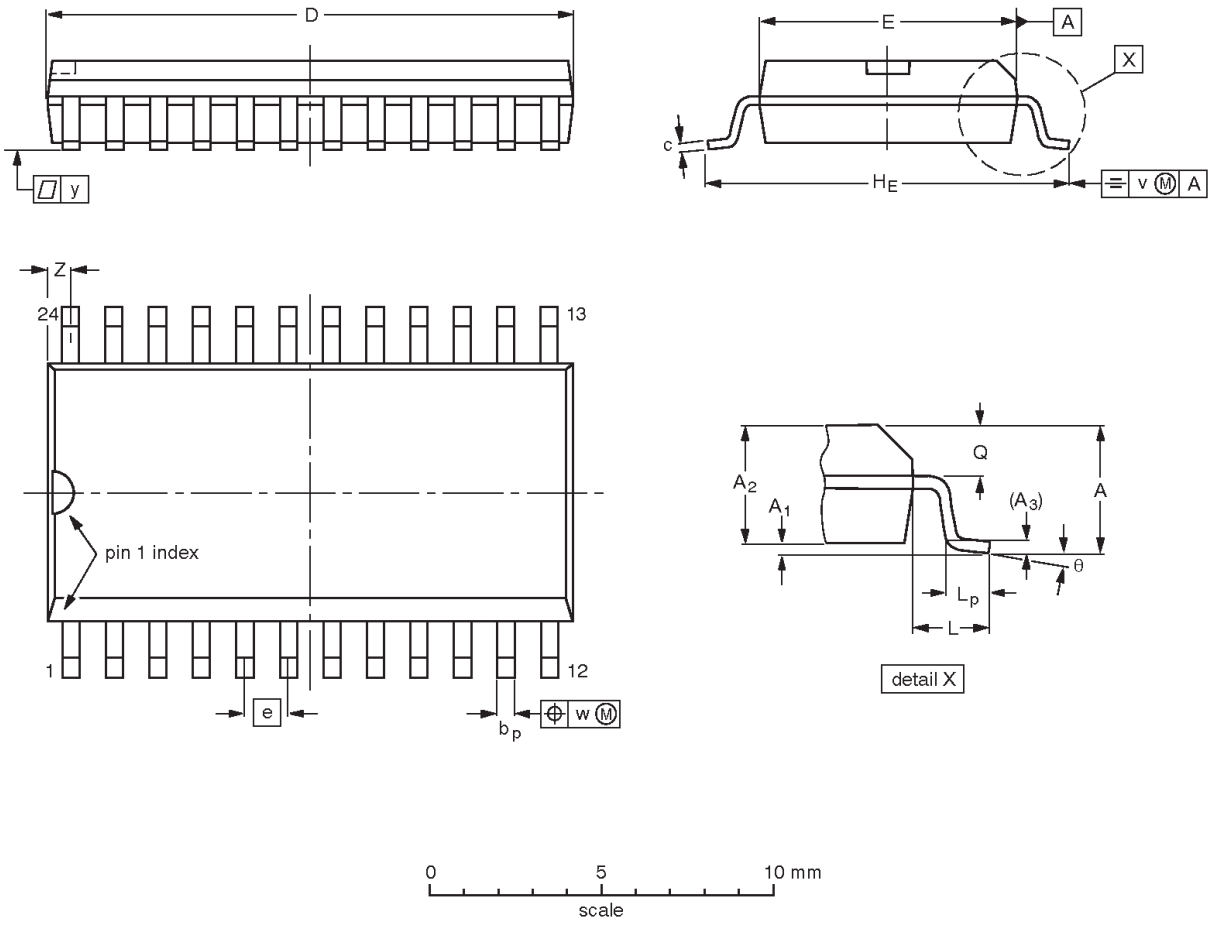
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	≤ 2.5 ns

SV00092

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

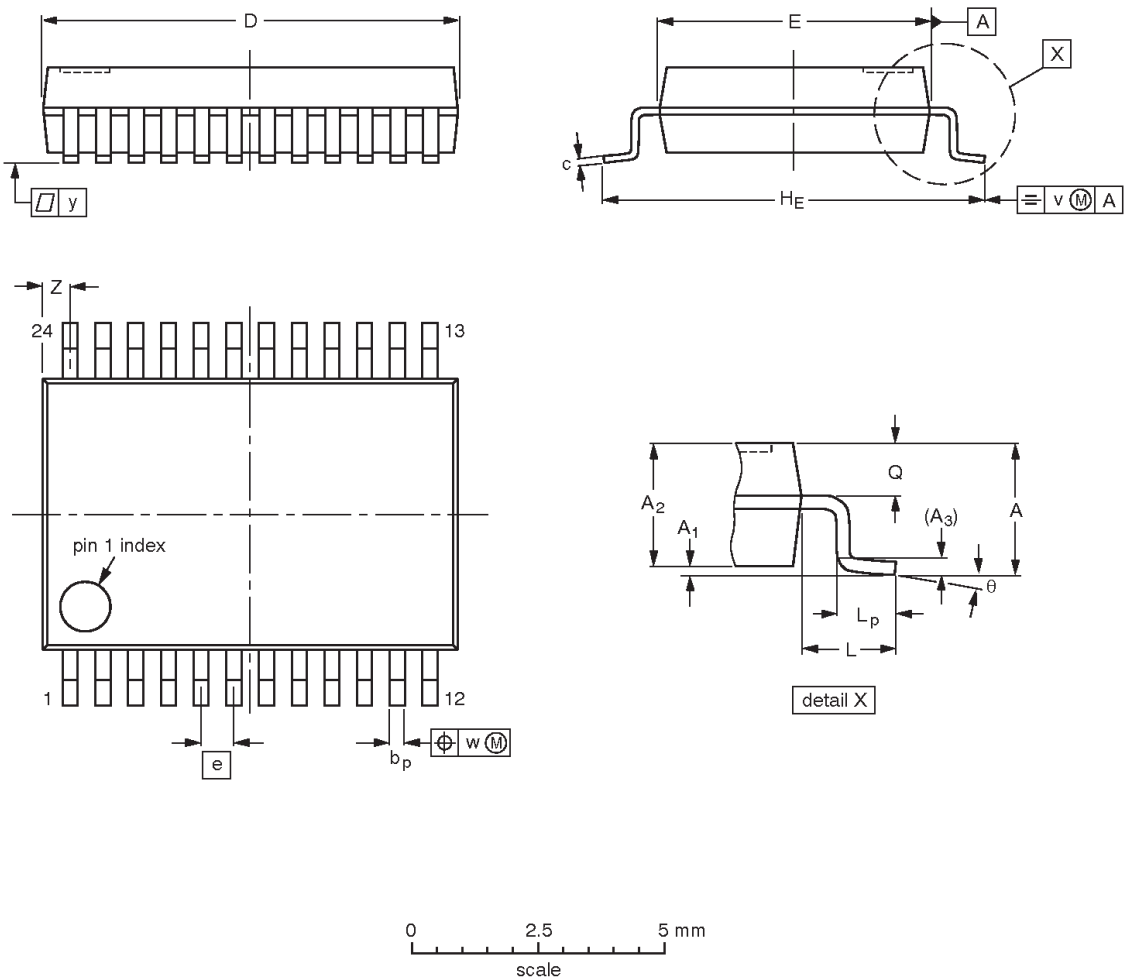
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

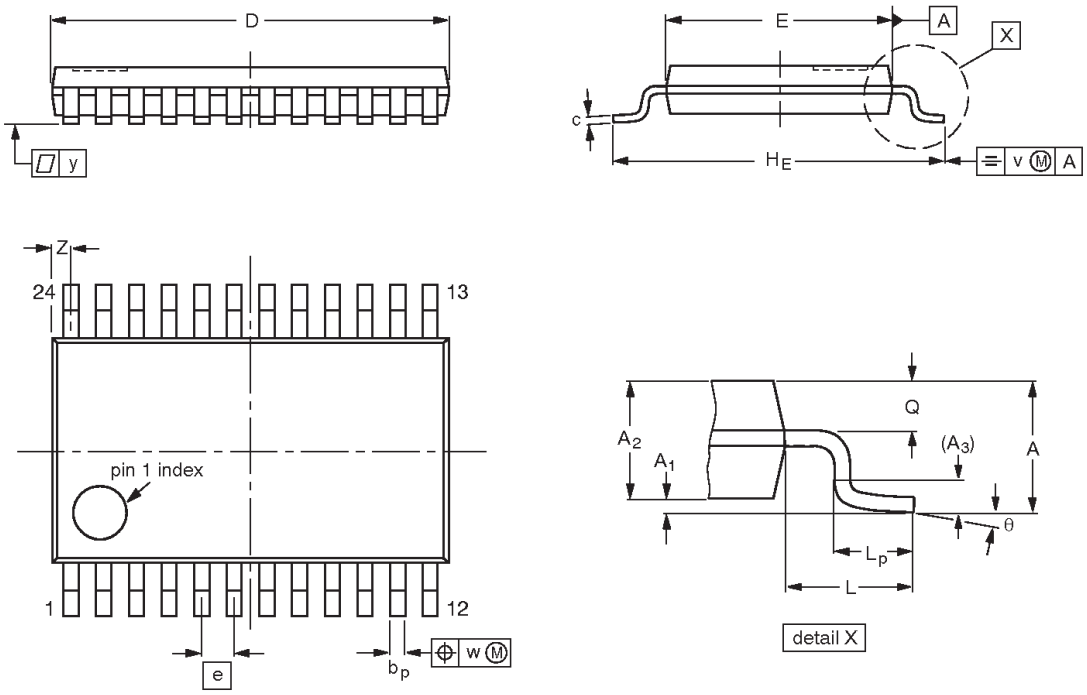
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

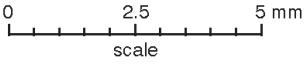
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_3	20040907	**Product data sheet (9397 750 04331). ECN 853-1765 18987 of 19 February 1998. Supersedes data of 1994 September 27.** Modifications: ● Ordering information table on page 2: remove ‘North America’ column; rename ‘Outside North America’ column to ‘Type number’. ● Logic diagram on page 3: add inversion symbols on clock signals before CP inputs.
_2	19980219	**Product specification (9397 750 03546). ECN 853-1765 18987 of 19 February 1998. Supersedes data of 1994 September 27.**
_1	19940927	

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data sheet	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data sheet	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 09-04

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