



# BUK9Y53-100B

N-channel TrenchMOS logic level FET

Rev. 01 — 30 August 2007

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology.

### 1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Logic level compatible

### 1.3 Applications

- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V, 24 V and 42 V loads

### 1.4 Quick reference data

- $E_{DS(AL)S} \leq 85$  mJ
- $I_D \leq 23$  A
- $R_{DSon} = 45$  m $\Omega$  (typ)
- $P_{tot} \leq 75$  W

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)	<p>SOT669 (LFPAK)</p>	<p>mb1798</p>
4	gate (G)		
mb	mounting base; connected to drain (D)		

### 3. Ordering information

**Table 2. Ordering information**

Type number	Package		Version
	Name	Description	
BUK9Y53-100B	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

### 4. Limiting values

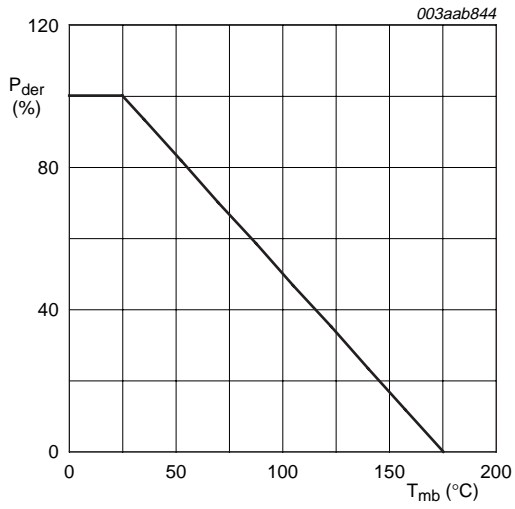
**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	100	V
$V_{DGR}$	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-	$\pm 15$	V
$I_D$	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	23	A
		$T_{mb} = 100\text{ }^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 2</a>	-	16	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	94	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 1</a>	-	75	W
$T_{stg}$	storage temperature		-55	+175	$^\circ\text{C}$
$T_j$	junction temperature		-55	+175	$^\circ\text{C}$
<b>Source-drain diode</b>					
$I_{DR}$	reverse drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	23	A
$I_{DRM}$	peak reverse drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	94	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 23\text{ A}$ ; $V_{DS} \leq 100\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; starting at $T_j = 25\text{ }^\circ\text{C}$	-	85	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		-	[1]	-

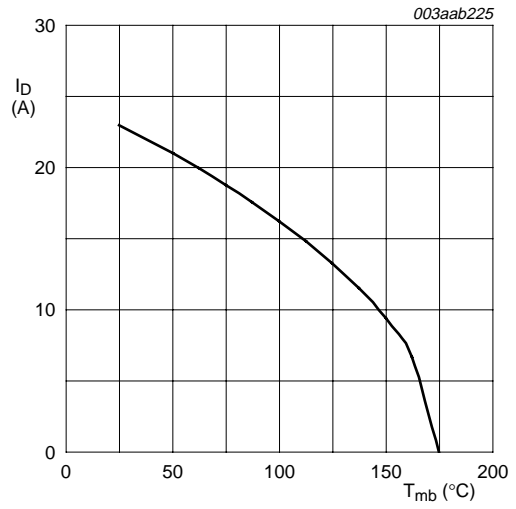
[1] Conditions:

- a) Maximum value not quoted. Repetitive rating defined in [Figure 16](#).
- b) Single-pulse avalanche rating limited by  $T_{j(max)}$  of 175  $^\circ\text{C}$ .
- c) Repetitive avalanche rating limited by  $T_{j(avg)}$  of 170  $^\circ\text{C}$ .
- d) Refer to application note *AN10273* for further information.



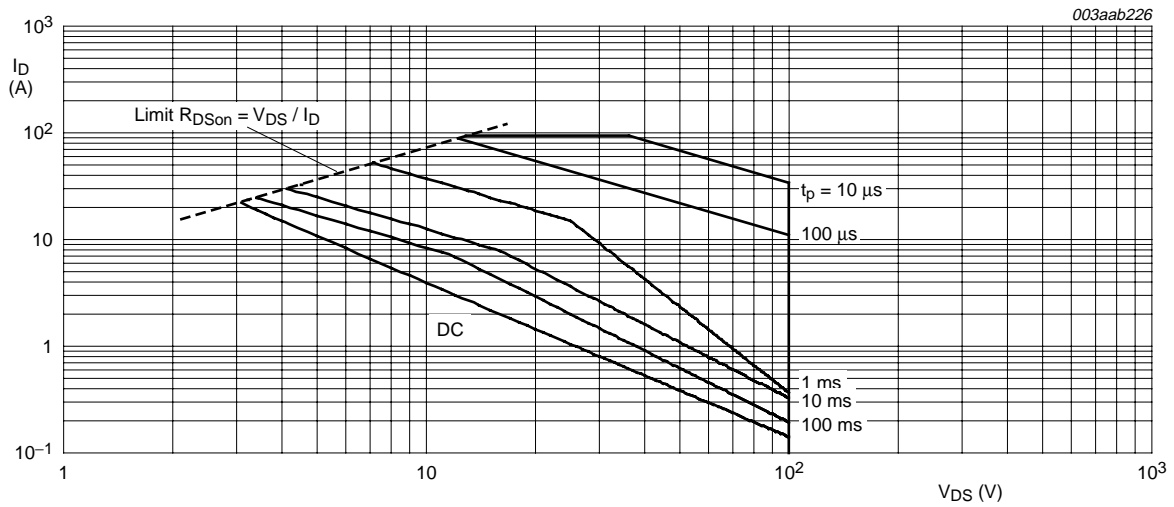
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature**



V<sub>GS</sub> ≥ 5 V

**Fig 2. Continuous drain current as a function of mounting base temperature**



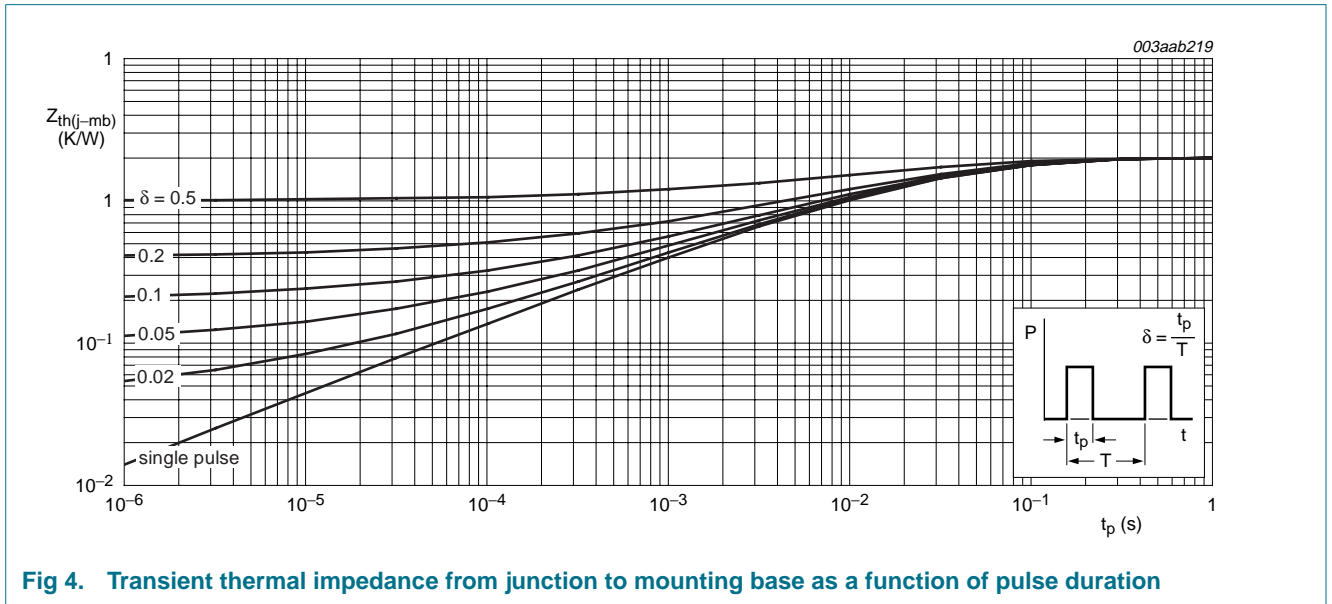
T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

**5. Thermal characteristics**

**Table 4: Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W



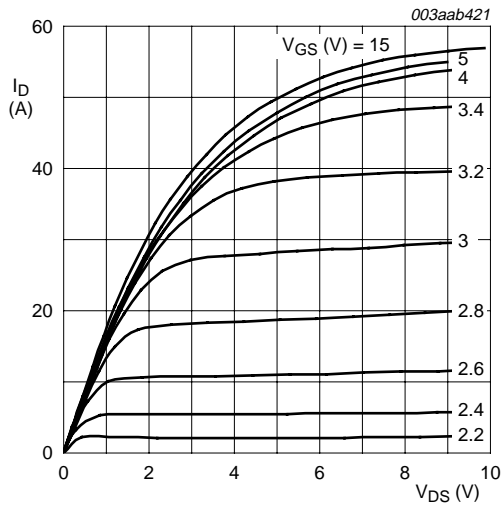
**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

**Table 5: Characteristics**

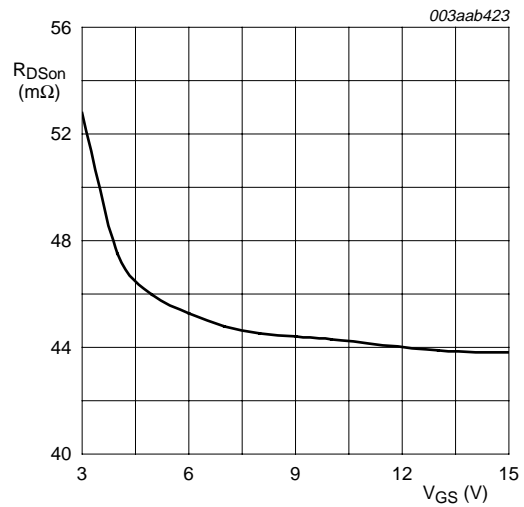
$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	100	-	-	V
		$T_j = -55\text{ °C}$	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>				
		$T_j = 25\text{ °C}$	1.1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.02	1	$\mu\text{A}$
		$T_j = 175\text{ °C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 15\text{ V}; V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 10\text{ A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>				
		$T_j = 25\text{ °C}$	-	45	53	m $\Omega$
		$T_j = 175\text{ °C}$	-	-	132	m $\Omega$
		$V_{GS} = 4.5\text{ V}; I_D = 10\text{ A}$	-	-	59	m $\Omega$
		$V_{GS} = 10\text{ V}; I_D = 10\text{ A}$	-	41	49	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 15\text{ A}; V_{DS} = 80\text{ V}; V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 14</a>	-	18	-	nC
$Q_{GS}$	gate-source charge		-	4.1	-	nC
$Q_{GD}$	gate-drain charge		-	8	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$ ; see <a href="#">Figure 12</a>	-	1600	2130	pF
$C_{oss}$	output capacitance		-	141	170	pF
$C_{riss}$	reverse transfer capacitance		-	60	82	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 2.5\text{ }\Omega$ ; $V_{GS} = 5\text{ V}; R_G = 10\text{ }\Omega$	-	18	-	ns
$t_r$	rise time		-	26	-	ns
$t_{d(off)}$	turn-off delay time		-	52	-	ns
$t_f$	fall time		-	16	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}$ ; see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	71	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	83	-	nC



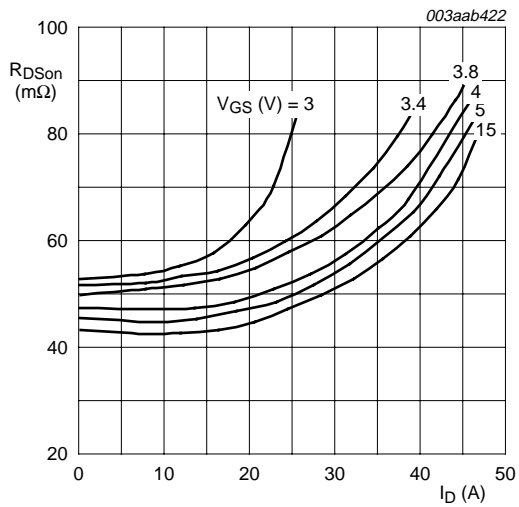
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



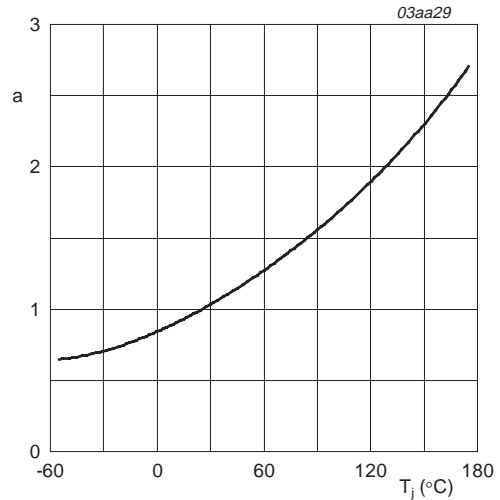
$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**



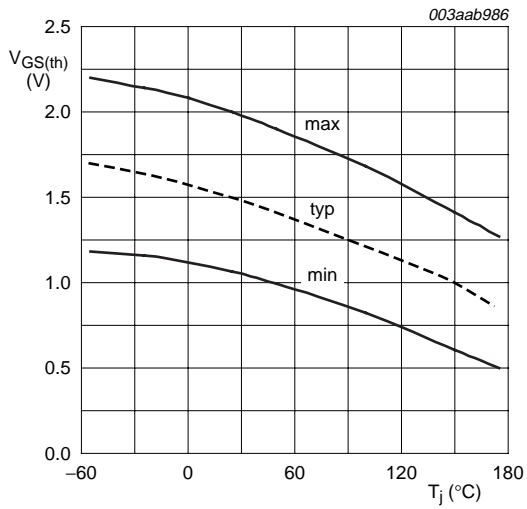
$T_j = 25\text{ }^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**



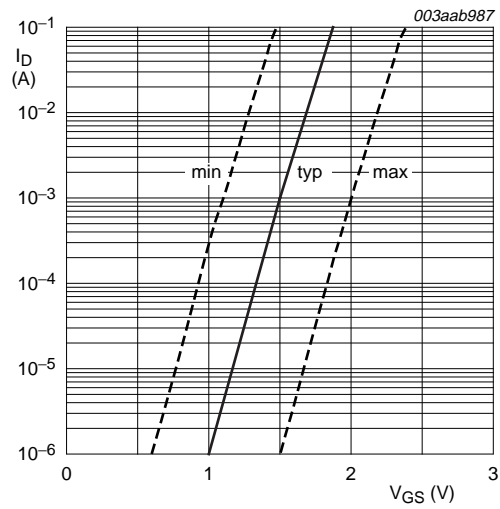
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**



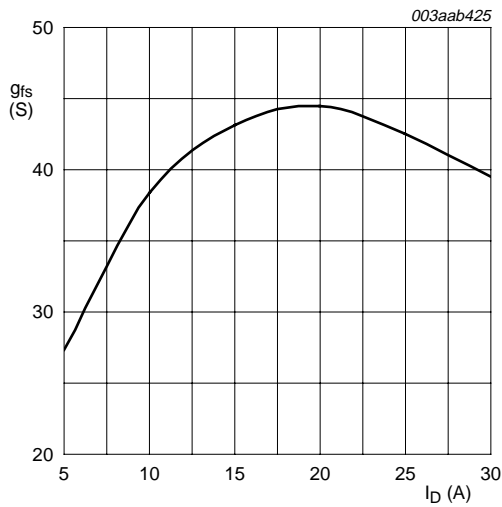
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



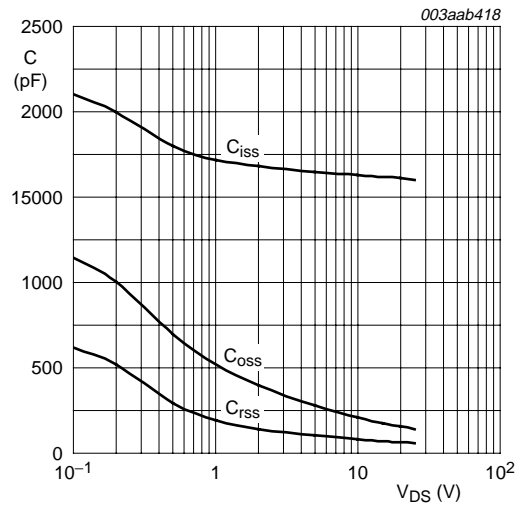
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



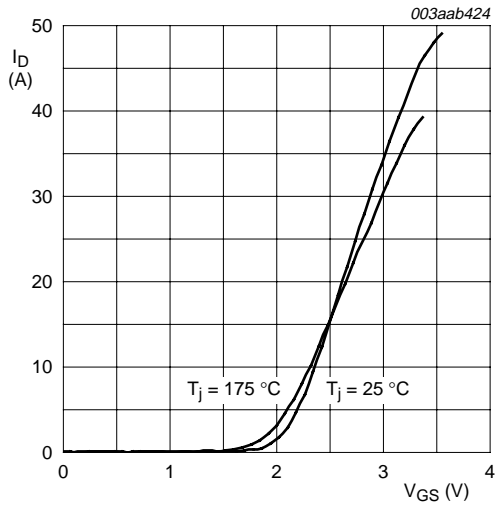
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

**Fig 11. Forward transconductance as a function of drain current; typical values**



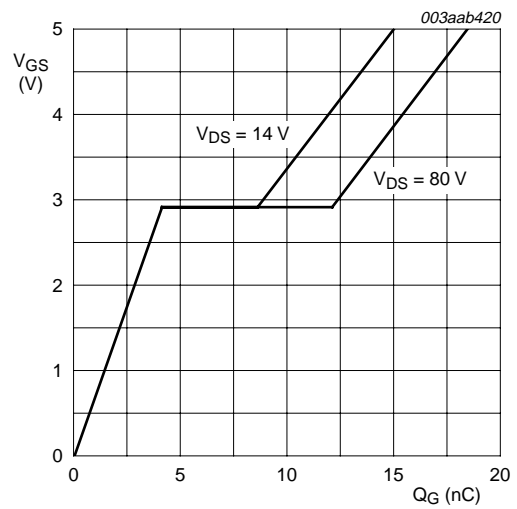
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



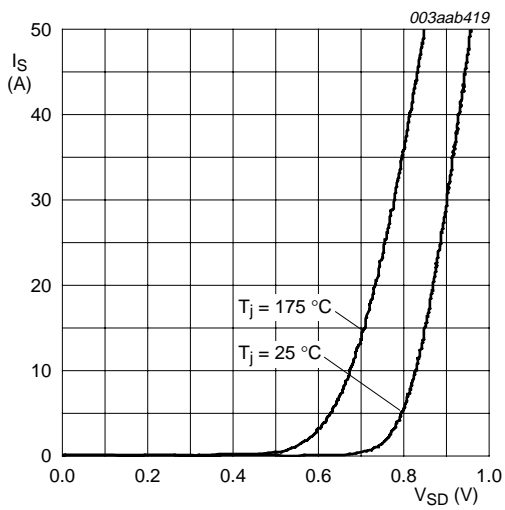
$V_{DS} = 25\text{ V}$

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



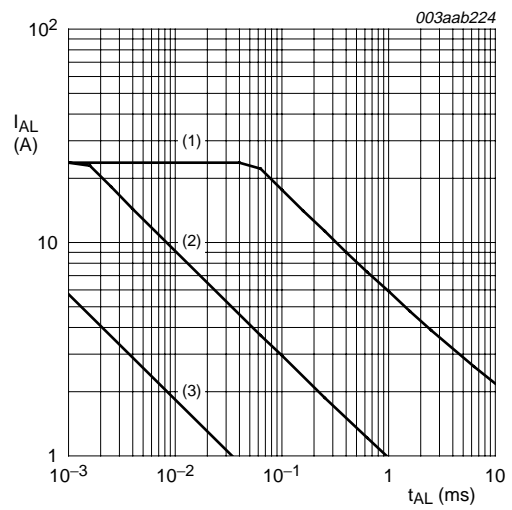
$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{ V}$

**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



See [Table note 1](#) of [Table 3](#) Limiting values.

- (1) Single-pulse;  $T_j = 25^\circ\text{C}$ .
- (2) Single-pulse;  $T_j = 150^\circ\text{C}$ .
- (3) Repetitive.

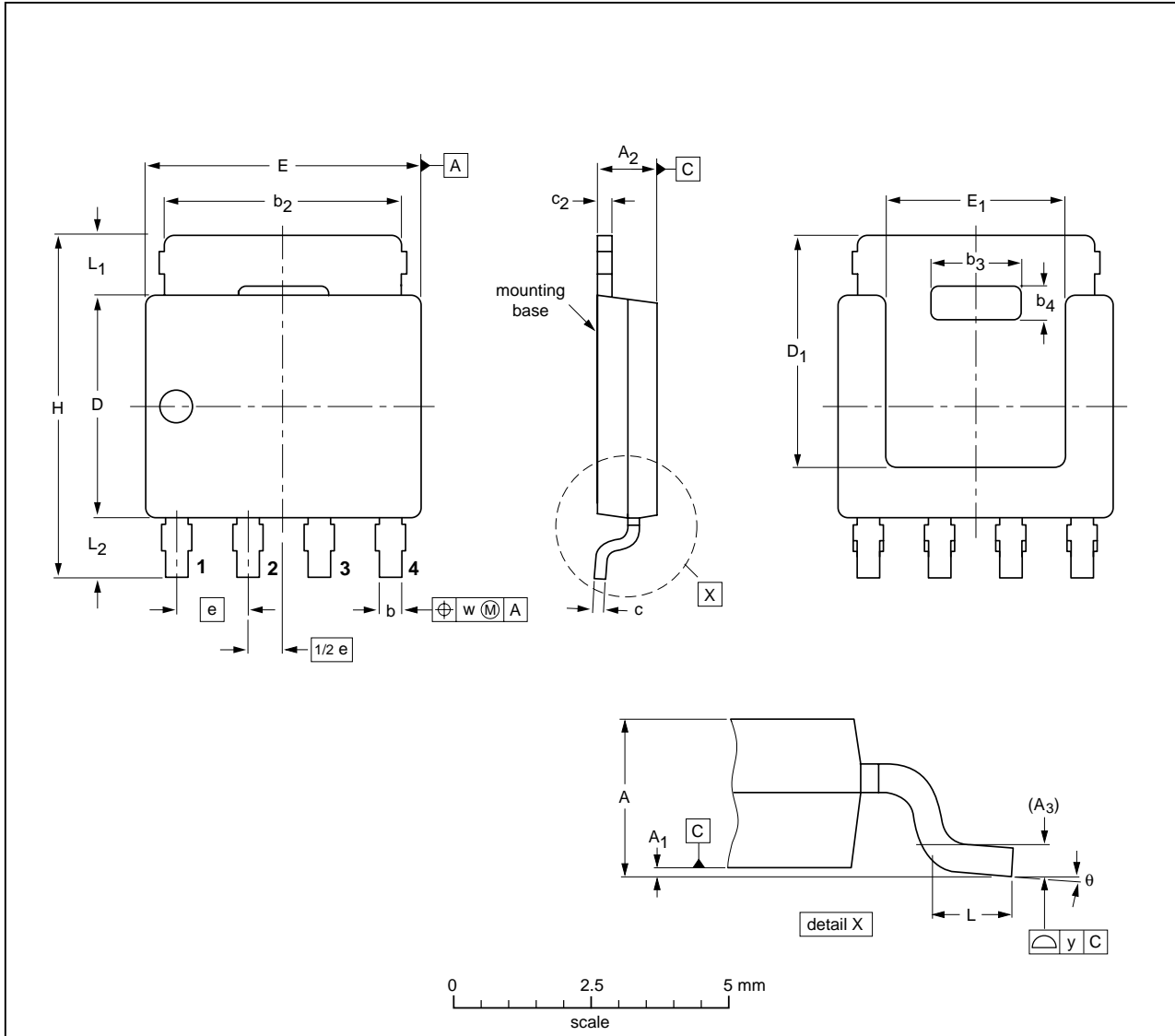
**Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time**



**7. Package outline**

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup> max	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT669		MO-235			04-10-13 06-03-16

**Fig 17. Package outline SOT669 (LPAK)**

## 8. Revision history

**Table 6.** Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9Y53-100B_01	20070830	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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