

# HEF4040B

## 12-stage binary ripple counter

Rev. 06 — 25 November 2009

Product data sheet

### 1. General description

The HEF4040B is a 12-stage binary ripple counter with a clock input ( $\overline{CP}$ ), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (Q0 to Q11). The counter advances on the HIGH-to-LOW transition of  $\overline{CP}$ . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of  $\overline{CP}$ . Each counter stage is a static toggle flip-flop. The clock input is highly tolerant of slow rise and fall times due to its Schmitt trigger action.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input. It is also suitable for use over the full industrial ( $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ) temperature range.

### 2. Features

- Tolerant of slow clock rise and fall time
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

### 4. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Package		Version
	Name	Description	
HEF4040BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4040BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

### 5. Functional diagram

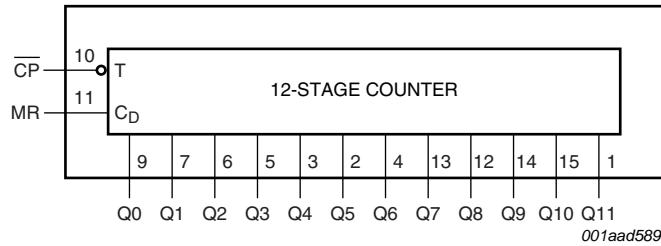


Fig 1. Functional diagram

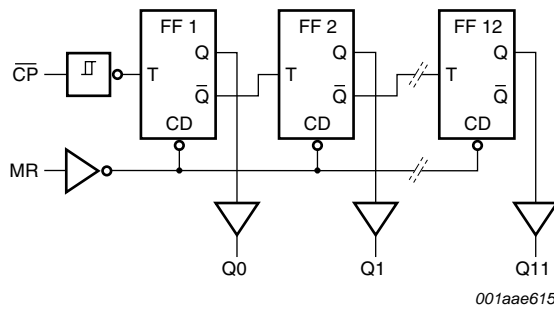


Fig 2. Logic diagram

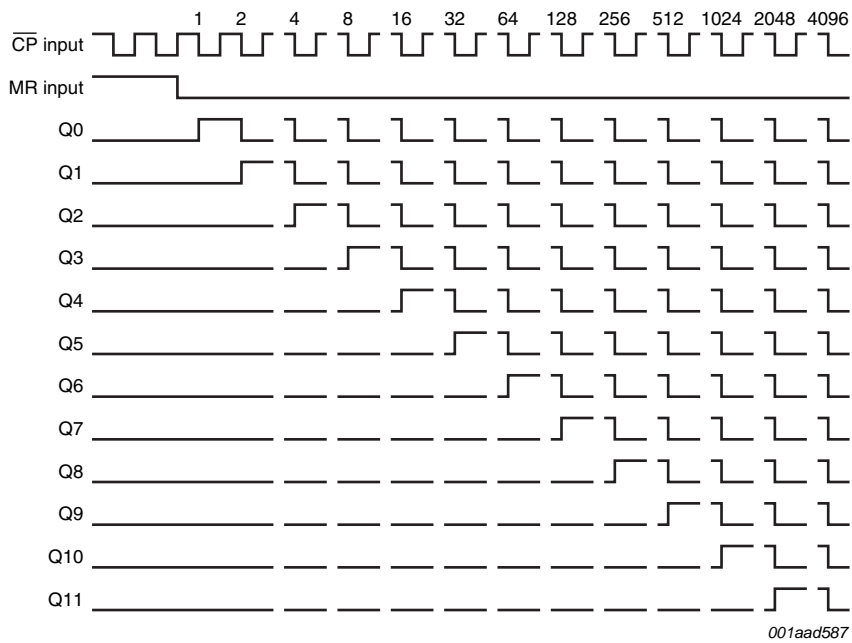
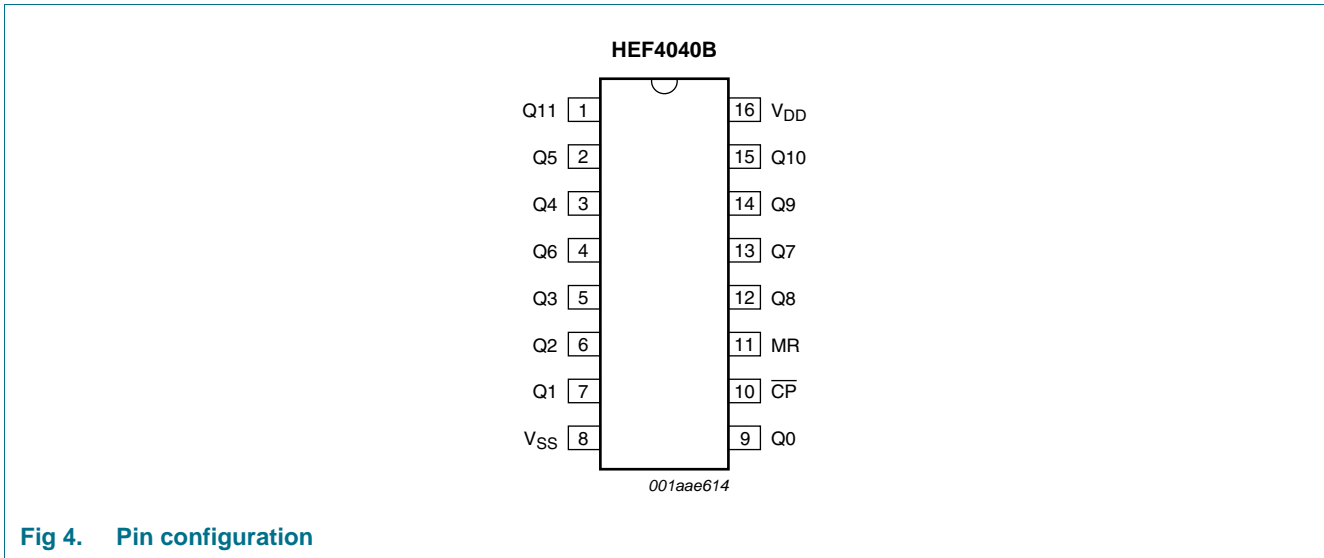


Fig 3. Timing diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
V <sub>SS</sub>	8	ground supply voltage
Q0 to Q11	9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	parallel output
$\overline{CP}$	10	clock input (HIGH-to-LOW edge-triggered)
MR	11	master reset input (active HIGH)
V <sub>DD</sub>	16	supply voltage

## 7. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	DIP16 package	[1] -	750	mW
		SO16 package	[2] -	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For DIP16 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 8. Recommended operating conditions

**Table 4. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

**Table 5. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V

**Table 5. Static characteristics ...continued**  
 $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = 25\text{ }^{\circ}\text{C}$		$T_{amb} = 85\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-1.7	-	-1.4	-	-1.1	-	mA
		$V_O = 4.6\text{ V}$	5 V	-0.52	-	-0.44	-	-0.36	-	mA
		$V_O = 9.5\text{ V}$	10 V	-1.3	-	-1.1	-	-0.9	-	mA
		$V_O = 13.5\text{ V}$	15 V	-3.6	-	-3.0	-	-2.4	-	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_{LI}$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	7.5	-	-	pF	

## 10. Dynamic characteristics

**Table 6. Dynamic characteristics**  
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified; for test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit	
$t_{PHL}$	HIGH to LOW propagation delay	$\overline{CP} \rightarrow Q_0$ see <a href="#">Figure 5</a>	5 V	$78\text{ ns} + (0.55\text{ ns/pF})C_L$	-	105	210	ns	
			10 V	$34\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns	
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns	
		$Q_n \rightarrow Q_n + 1$		5 V	<sup>[2]</sup> $(0.55\text{ ns/pF})C_L$	-	35	70	ns
				10 V	<sup>[2]</sup> $(0.23\text{ ns/pF})C_L$	-	15	30	ns
				15 V	<sup>[2]</sup> $(0.16\text{ ns/pF})C_L$	-	10	20	ns
		$MR \rightarrow Q_n$ see <a href="#">Figure 5</a>		5 V	$63\text{ ns} + (0.55\text{ ns/pF})C_L$	-	90	180	ns
				10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
				15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
$t_{PLH}$	LOW to HIGH propagation delay	$\overline{CP} \rightarrow Q_0$ see <a href="#">Figure 5</a>	5 V	$58\text{ ns} + (0.55\text{ ns/pF})C_L$	-	85	170	ns	
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns	
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns	
		$Q_n \rightarrow Q_n + 1$		5 V	<sup>[2]</sup> $(0.55\text{ ns/pF})C_L$	-	35	70	ns
				10 V	<sup>[2]</sup> $(0.23\text{ ns/pF})C_L$	-	15	30	ns
				15 V	<sup>[2]</sup> $(0.16\text{ ns/pF})C_L$	-	10	20	ns

**Table 6. Dynamic characteristics ...continued**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified; for test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_t$	transition time	see <a href="#">Figure 5</a>	5 V	<sup>[3]</sup> $10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
$t_w$	pulse width	CP input HIGH; minimum width; see <a href="#">Figure 5</a>	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		MR input HIGH; minimum width; see <a href="#">Figure 5</a>	5 V		40	20	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
$t_{rec}$	recovery time	MR input; see <a href="#">Figure 5</a>	5 V		40	20	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
$f_{max}$	maximum frequency	CP input; see <a href="#">Figure 5</a>	5 V		10	20	-	MHz
			10 V		15	30	-	MHz
			15 V		25	50	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF)

[2] For loads other than 50 pF at the  $n^{\text{th}}$  output, use the slope given.

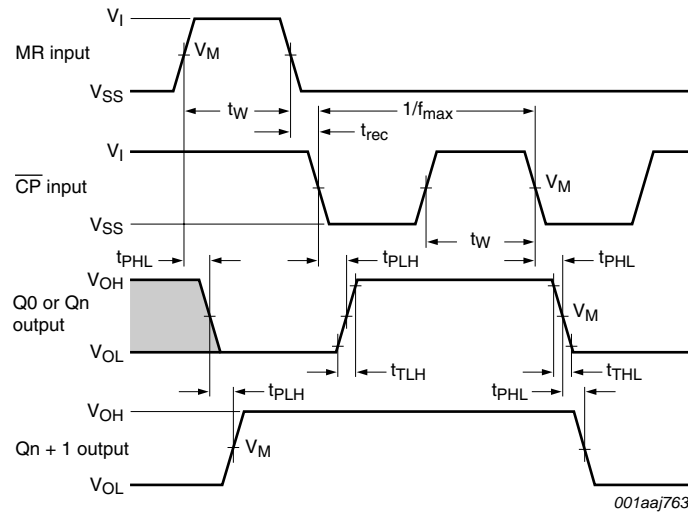
[3]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

**Table 7. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz,
		10 V	$P_D = 2000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_o$ = output frequency in MHz,
		15 V	$P_D = 5200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.

11. Waveforms

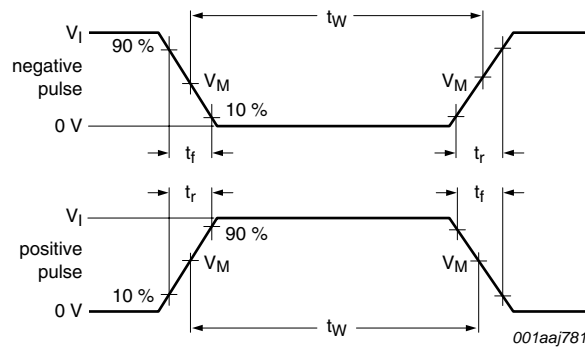


Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.  
 Transition times: transition time ( $t_t$ ) = HIGH LOW ( $t_{THL}$ ) or LOW HIGH ( $t_{TLH}$ ) transition times.  
 Measurement points are given in [Table 8](#), test circuit in [Figure 6](#) and test data in [Table 9](#)

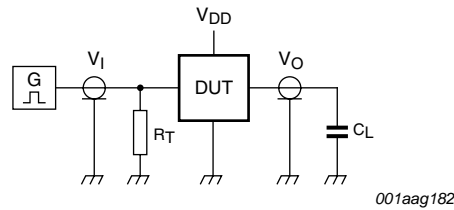
Fig 5. Waveforms showing propagation delays for MR to Qn and CP to Q0, minimum MR and CP pulse widths

Table 8. Measurement points

Supply voltage	Input		Output
$V_{DD}$	$V_I$	$V_M$	$V_M$
5 V to 15 V	$V_{DD}$ or $V_{SS}$	$0.5V_{DD}$	$0.5V_{DD}$



a. Input waveforms



b. Test circuit

Test data is given in [Table 9](#).

Definitions test circuit:

DUT = Device Under Test;

$C_L$  = load capacitance, including the jig and probe capacitance;

$R_L$  = load resistance, which should be equal to the output impedance of the pulse generator.

Fig 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	50 pF
	$t_r, t_f$	$\leq 20$ ns



12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

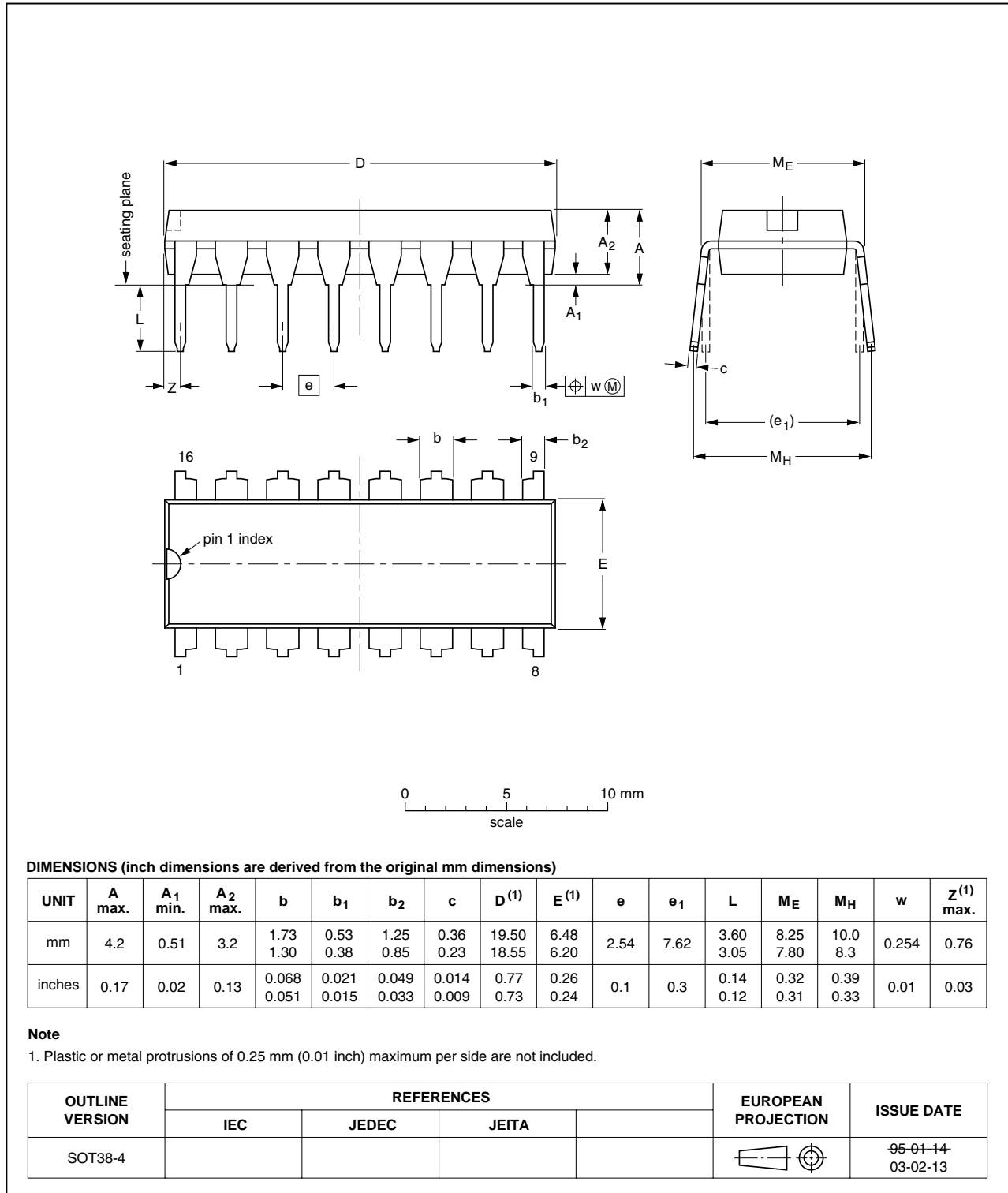


Fig 7. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

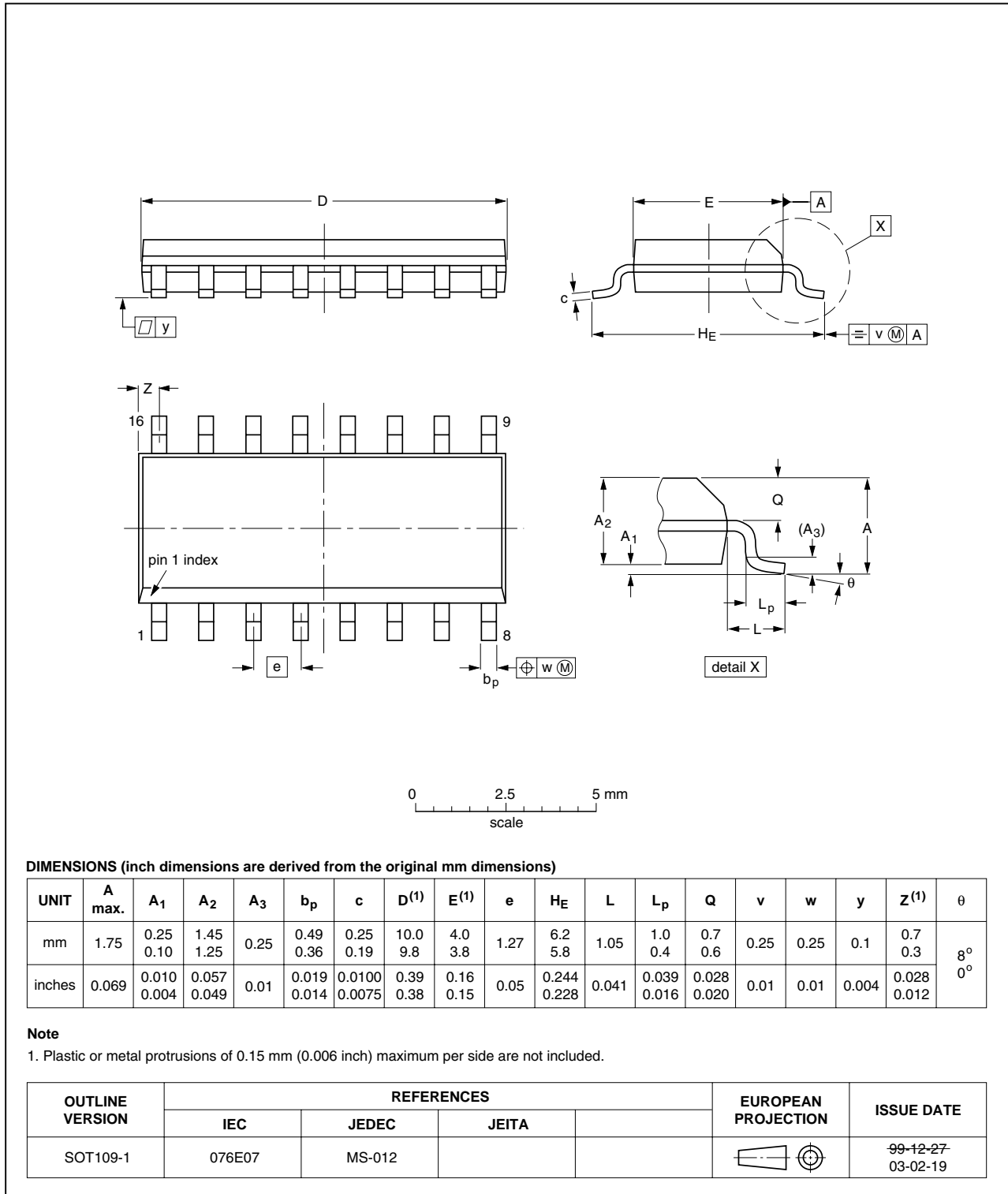


Fig 8. Package outline SOT109-1 (SO16)

## 13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4040B_6	20091125	Product data sheet	-	HEF4040B_5
Modifications:	• <a href="#">Section 2 "Features"</a> , $\Delta t/\Delta V$ values updated.			
HEF4040B_5	20090709	Product data sheet	-	HEF4040B_4
HEF4040B_4	20090304	Product data sheet	-	HEF4040B_CNV_3
HEF4040B_CNV_3	19950101	Product specification	-	HEF4040B_CNV_2
HEF4040B_CNV_2	19950101	Product specification	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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