
ST-NXP Wireless

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As from August 2nd 2008, the wireless operations of NXP have moved to a new company, ST-NXP Wireless.

As a result, the following changes are applicable to the attached document.

- **Company name - NXP B.V.** is replaced with **ST-NXP Wireless**.
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- **Web site** - <http://www.nxp.com> is replaced with <http://www.stnwireless.com>
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ST-NXP Wireless



ISP1302

Universal Serial Bus On-The-Go transceiver with carkit support

Rev. 01 — 24 May 2007

Product data sheet



1. General description

The ISP1302 is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver device that supports *USB Carkit Specification (CEA-936-A), November 2005*. It is fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB Specification Rev. 1.2*. The ISP1302 can transmit and receive serial data at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates.

The ISP1302 is available in HVQFN24 and WLCSP25 packages.

2. Features

- Fully complies with:
 - ◆ *Universal Serial Bus Specification Rev. 2.0*
 - ◆ *On-The-Go Supplement to the USB Specification Rev. 1.2*
 - ◆ *On-The-Go Transceiver Specification (CEA-2011)*
 - ◆ *USB Carkit Specification (CEA-936-A), November 2005*
- Can transmit and receive serial data at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates
- Supports OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Supports I²C-bus (up to 400 kHz) serial interface to access control and status registers
- Supports Universal Asynchronous Receiver-Transmitter (UART) pass-through on the DP and DM lines
- Supports service mode with 2.8 V UART signaling on the DP and DM lines
- Built-in analog switches to support analog audio signals multiplexed on the DP and DM lines
- Built-in DC biasing for audio signals on the DP and DM lines
- Supports both 4-wire and 5-wire signaling protocol for carkit application
- Supports data-during-audio mode for smart carkit application
- Built-in charge pump regulator outputs 5 V at current up to 50 mA
- 3.0 V to 4.5 V power supply input range (V_{CC})
- Supports wide range digital interfacing I/O voltage ($V_{CC(I/O)}$) 1.4 V to 3.6 V
- Full industrial grade operation from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Available in small HVQFN24 and WLCSP25 halogen-free and lead-free packages

3. Applications

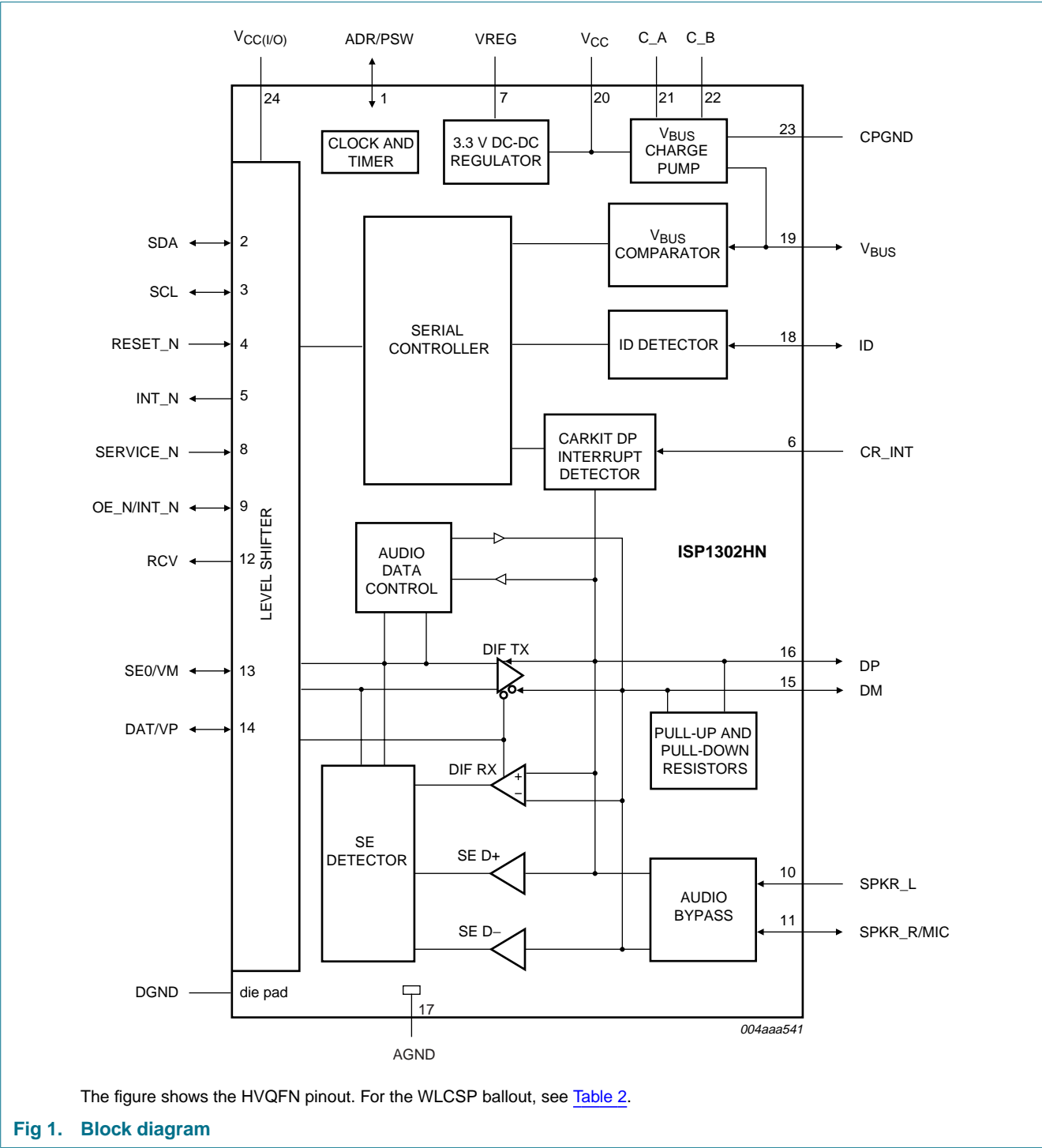
- Mobile phones
- Digital camera
- Personal digital assistant

4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-------------|---------|--|-----------|
| | Name | Description | Version |
| ISP1302HN | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body $4 \times 4 \times 0.85$ mm | SOT616-3 |
| ISP1302UK | WLCSP25 | wafer level chip-size package; 25 bumps; $2.5 \times 2.5 \times 0.6$ mm | ISP1302UK |

5. Block diagram

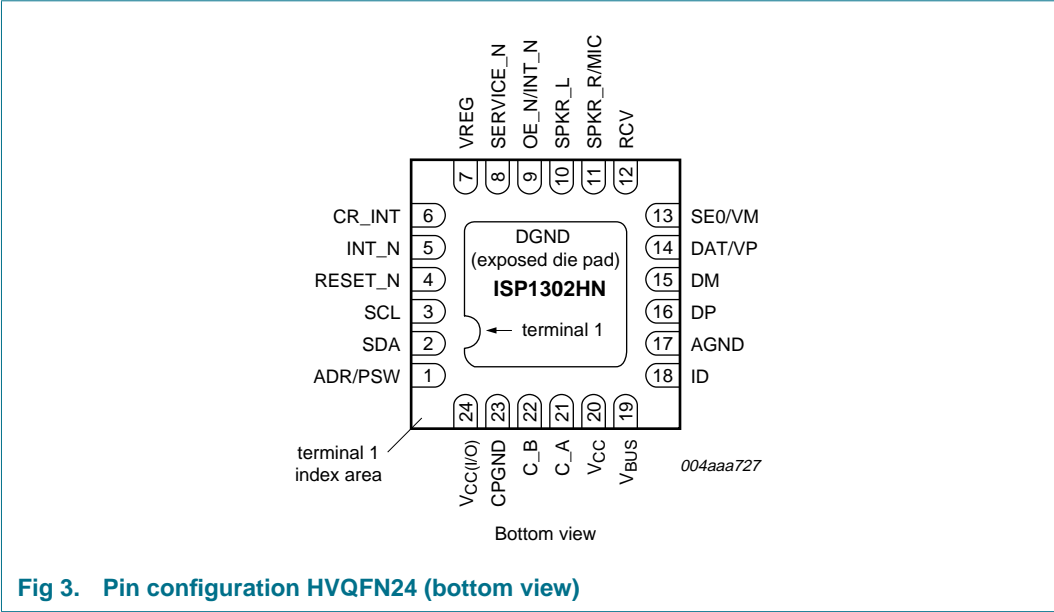
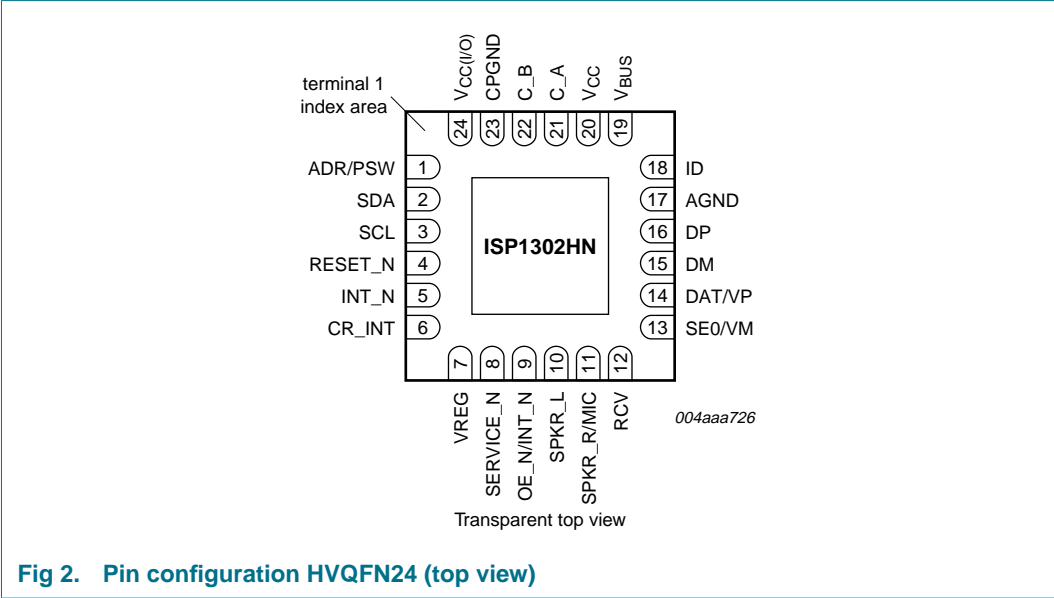


The figure shows the HVQFN pinout. For the WLCSP ballout, see [Table 2](#).

Fig 1. Block diagram

6. Pinning information

6.1 Pinning



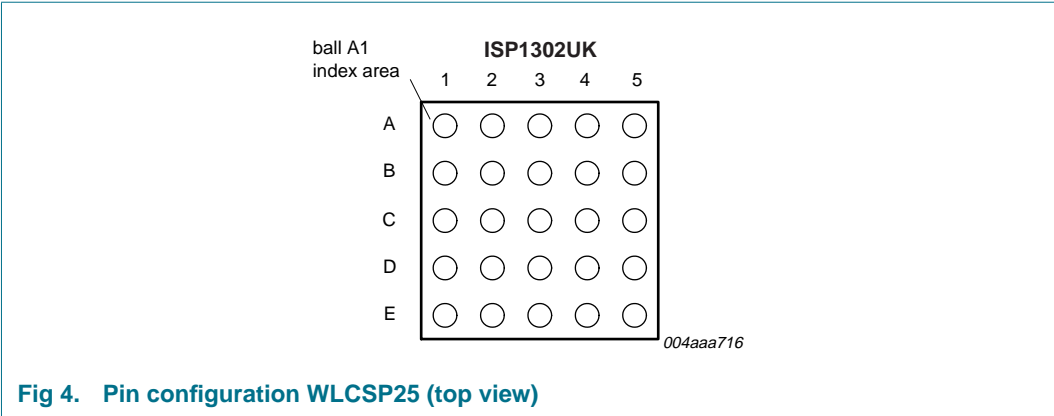


Fig 4. Pin configuration WLCSP25 (top view)

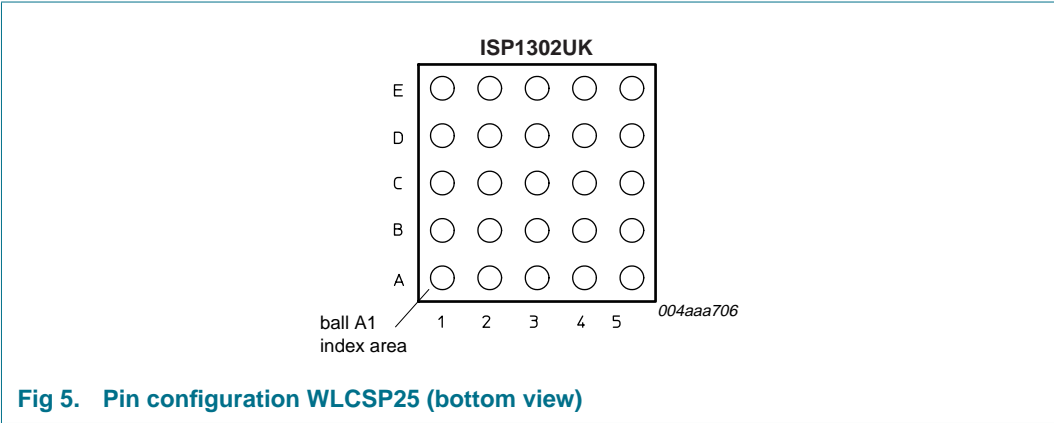


Fig 5. Pin configuration WLCSP25 (bottom view)

6.2 Pin description

Table 2. Pin description

| Symbol ^[1] | Pin HVQFN24 | Ball WLCSP25 | Type ^[2] | Reset value | Description |
|-----------------------|-------------|--------------|---------------------|-------------|--|
| ADR/PSW | 1 | C1 | I/O | high-Z | ADR input — Sets the least-significant I ² C-bus address bit of the ISP1302; latched on the rising edge of the RESET_N pin PSW output — Enables or disables the external charge pump after reset An internal series resistor is implemented for this pin. If the PSW (output) function is not used, then this pin can directly be connected to DGND or VREG. This pin will output 3.3 V when driven HIGH. For details, see Section 7.13 . bidirectional; push-pull input; 3-state output |
| SDA | 2 | D2 | I/OD | high-Z | serial I ² C-bus data input and output bidirectional; push-pull input; open-drain output |
| SCL | 3 | D3 | I/OD | high-Z | serial I ² C-bus clock input and output bidirectional; push-pull input; open-drain output |
| RESET_N | 4 | C2 | I | - | asynchronous reset input, active LOW |
| INT_N | 5 | B1 | OD | high-Z | interrupt output; active LOW open-drain output |

Table 2. Pin description ...continued

| Symbol ^[1] | Pin HVQFN24 | Ball WLCSP25 | Type ^[2] | Reset value | Description |
|-----------------------|----------------|-----------------|---------------------|----------------|--|
| CR_INT | 6 | C4 | AI | - | directly connect to the DP pin of the USB connector; if the carkit feature is not used, this pin can be connected to ground |
| VREG | 7 | A2 | P | - | output of the voltage regulator; place a 0.1 μ F capacitor between this pin and ground |
| SERVICE_N | 8 | A1 | I | - | input; sets default operation mode of the ISP1302: <ul style="list-style-type: none"> If a LOW is latched on reset (including power-on reset), default mode is UART with 2.8 V signaling. If a HIGH is latched on reset (including power-on reset), default mode is USB with 3.3 V signaling. Operation mode can be changed after reset by changing the value of the Mode register bits. |
| OE_N/INT_N | 9 | B3 | I/O | high-Z | this pin can be programmed as: <p>OE_N input — Enables driving DP and DM when in USB mode</p> <p>INT_N output — Indicates interrupt when bit OE_INT_EN = 1 and SUSPEND_REG = 1</p> bidirectional; push-pull input; 3-state output |
| SPKR_L | 10 | A3 | AI | - | analog audio input signal for the left speaker channel; connect to ground if not in use |
| SPKR_R/MIC | 11 | A4 | AI/O | - | analog audio input signal for the right speaker channel or audio output signal for the microphone channel; connect to ground if not in use |
| RCV | 12 | A5 | O | 0 | differential receiver output; reflects the differential value of DP and DM push-pull output |
| SE0/VM | 13 | B4 | I/O | high-Z | SE0 input and output — SE0 functions in DAT_SE0 USB mode VM input and output — VM functions in VP_VM USB mode TxD input — UART mode bidirectional; push-pull input; 3-state output |
| DAT/VP | 14 | B5 | I/O | high-Z | DAT input and output — DAT functions in DAT_SE0 USB mode VP input and output — VP functions in VP_VM USB mode RxD output — UART mode bidirectional; push-pull input; 3-state output |
| DM | 15 | D5 | AI/O | high-Z | this pin can be programmed as: <ul style="list-style-type: none"> USB D– (data minus pin) transparent UART TxD or transparent audio SPKR_L |
| DP | 16 | D4 | AI/O | high-Z | this pin can be programmed as: <ul style="list-style-type: none"> USB D+ (data plus pin) transparent UART RxD or transparent audio SPKR_R/MIC |
| AGND | 17 | C3 | P | - | analog ground |

Table 2. Pin description ...continued

| Symbol ^[1] | Pin HVQFN24 | Ball WLCSP25 | Type ^[2] | Reset value | Description |
|-----------------------|--------------------|-----------------|---------------------|----------------|--|
| ID | 18 | C5 | AI/O | - | identification detector input and output; connected to the ID pin of the USB mini receptacle; internal 100 k Ω pull-up resistor |
| V _{BUS} | 19 | E5 | AI/O | high-Z | V _{BUS} line input and output of the USB interface; charge pump output; place an external decoupling capacitor of 0.1 μ F close to this pin |
| V _{CC} | 20 | E4 | P | - | supply voltage (3.0 V to 4.5 V) |
| C_A | 21 | E3 | AI/O | - | charge pump flying capacitor pin 2; connect a 220 nF capacitor between C_B and C_A for 50 mA output current |
| C_B | 22 | E2 | AI/O | - | charge pump flying capacitor pin 1; connect a 220 nF capacitor between C_B and C_A for 50 mA output current |
| CPGND | 23 | E1 | P | - | ground for the charge pump |
| V _{CC(I/O)} | 24 | D1 | P | - | supply voltage for the I/O interface logic signals (1.4 V to 3.6 V) |
| DGND | exposed die pad | B2 | P | - | digital ground |

[1] Symbol names ending with underscore N (for example, NAME_N) indicate active LOW signals.

[2] AI = analog input; AI/O = analog input/output; I = input; O = output; I/O = digital input/output; I/OD = input/open-drain output; OD = open-drain output; P = power or ground.

7. Functional description

7.1 Serial controller

The serial controller includes the following functions:

- Serial controller interface
- Device identification registers
- Control registers
- Interrupt registers
- Interrupt generator

The serial controller acts as an I²C-bus slave, and uses the SCL and SDA pins to communicate with the OTG Controller.

For details on the serial controller, see [Section 9](#).

7.2 V_{BUS} charge pump

The charge pump supplies current to the V_{BUS} line. It can operate in any of the following modes:

- Output 5 V at current above 50 mA
- Pull-up V_{BUS} to 3.3 V through a resistor (R_{UP(VBUS)}) to initiate V_{BUS} pulsing SRP
- Pull-down V_{BUS} to ground through a resistor (R_{DN(VBUS)}) to discharge V_{BUS}

7.3 V_{BUS} comparators

V_{BUS} comparators provide indications regarding the voltage level on V_{BUS}.

7.3.1 V_{BUS} valid comparator

This comparator is used by an A-device to determine whether the voltage on V_{BUS} is at a valid level for operation. The minimum threshold for the V_{BUS} valid comparator is 4.4 V. Any voltage on V_{BUS} below this threshold is considered a fault. A hardware debounce timer (t_{d(VA_VBUS_VLD)}) is implemented for the V_{BUS} valid comparator. This timer is enabled when the internal charge pump is turned on (bit VBUS_DRV = 1) and is disabled when the internal charge pump is turned off (bit VBUS_DRV = 0). During power-up, it is expected that the comparator output will be ignored.

7.3.2 Session valid comparator

The session valid comparator is used to determine when V_{BUS} is high enough for a session to start. Both the A-device and the B-device use this comparator to detect when a session is started. These devices also use this comparator to indicate when a session is completed. The session valid threshold is between 0.8 V to 2.0 V for A-device, and between 0.8 V to 4.0 V for B-device.

7.3.3 Session end comparator

The session end comparator determines when V_{BUS} is below the B-device session end threshold of 0.2 V to 0.8 V.

7.4 ID detector

In normal power mode (when both V_{CC} and $V_{CC(I/O)}$ are present), the ID detector senses the condition of the ID line and can differentiate between the following conditions:

- The ID pin is floating (bit ID_FLOAT = 1).
- The ID pin is shorted to ground (bit ID_GND = 1).
- The ID pin is connected to ground through resistor $R_{DN(ID)} = 102\text{ k}\Omega$ (bit ID_102K = 1).
- The ID pin is connected to ground through resistor $R_{DN(ID)} = 200\text{ k}\Omega$ (bit ID_200K = 1).
- The ID pin is connected to ground through resistor $R_{DN(ID)} = 440\text{ k}\Omega$ (bit ID_440K = 1).

In power-down mode, only ID_FLOAT detector is active and can wake-up the chip. The remaining detectors are turned off.

[Table 3](#) shows the type of device connected, depending on the status of the ID and V_{BUS} pins.

Table 3. ID pin status for various applications

| SESS_VLD | ID_FLOAT | ID_GND | ID_102K | ID_200K | ID_440K | Device connected |
|----------|----------|--------|---------|---------|---------|-------------------|
| 0 | 1 | 0 | 0 | X | X | nothing connected |
| 0 | 0 | 1 | 0 | 0 | 0 | OTG A-device |
| 0 | 0 | 0 | 1 | 0 | 0 | phone accessory |
| 1 | 0 | 0 | 0 | 1 | 0 | charger type 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | charger type 2 |
| 1 | 1 | 0 | 0 | 0 | 0 | carkit or PC |

The recommended procedure to detect the ID status using software is:

1. When nothing is connected, ID is floating and ID_FLOAT = 1. The chip can be set in power-down mode.
2. Enable the ID_FLOAT (rising edge and falling edge) and SESS_VLD (rising edge) interrupts.
3. If a plug that causes a change in ID_FLOAT or SESS_VLD is inserted, an interrupt occurs. Interrupt Latch register bit ID_FLOAT or SESS_VLD is set.
4. The software waits for sometime, for example: 100 ms, to allow mechanical debounce.
5. The software reads the Interrupt Source register and the OTG Status register, and checks bits SESS_VLD, ID_GND, ID_102K, ID_200K and ID_440K.
6. The device type is determined according to [Table 3](#).

The ID detector has a switch that can be used to ground pin ID. This switch is controlled by bit ID_PULLDN of the OTG Control register, and bits PH_ID_INT and PH_ID_ACK of the Audio Control register. See [Table 4](#).

Table 4. ID pull-down control

| ID_PULLDN | PH_ID_ACK | PH_ID_INT | Switch between ID and ground |
|-----------|-----------|-----------|--|
| 0 | 0 | 0 | off |
| 0 | 0 | 1 | on for time $t_{PH_ID_INT}$, then off and bit PH_ID_INT autoclears to 0 |
| 0 | 1 | 0 | wait for time $t_{PH_ID_WT}$, turn on the switch for $t_{PH_ID_INT}$, then off and bit PH_ID_ACK autoclears to 0 |
| 0 | 1 | 1 | not defined |
| 1 | X | X | on |

7.5 Pull-up and pull-down resistors

[Figure 6](#) shows the switchable pull-up and pull-down resistors that are internally connected to the DP and DM lines. The DP pull-up resistor (SW1) is controlled by bit DP_PULLUP of the OTG Control register.

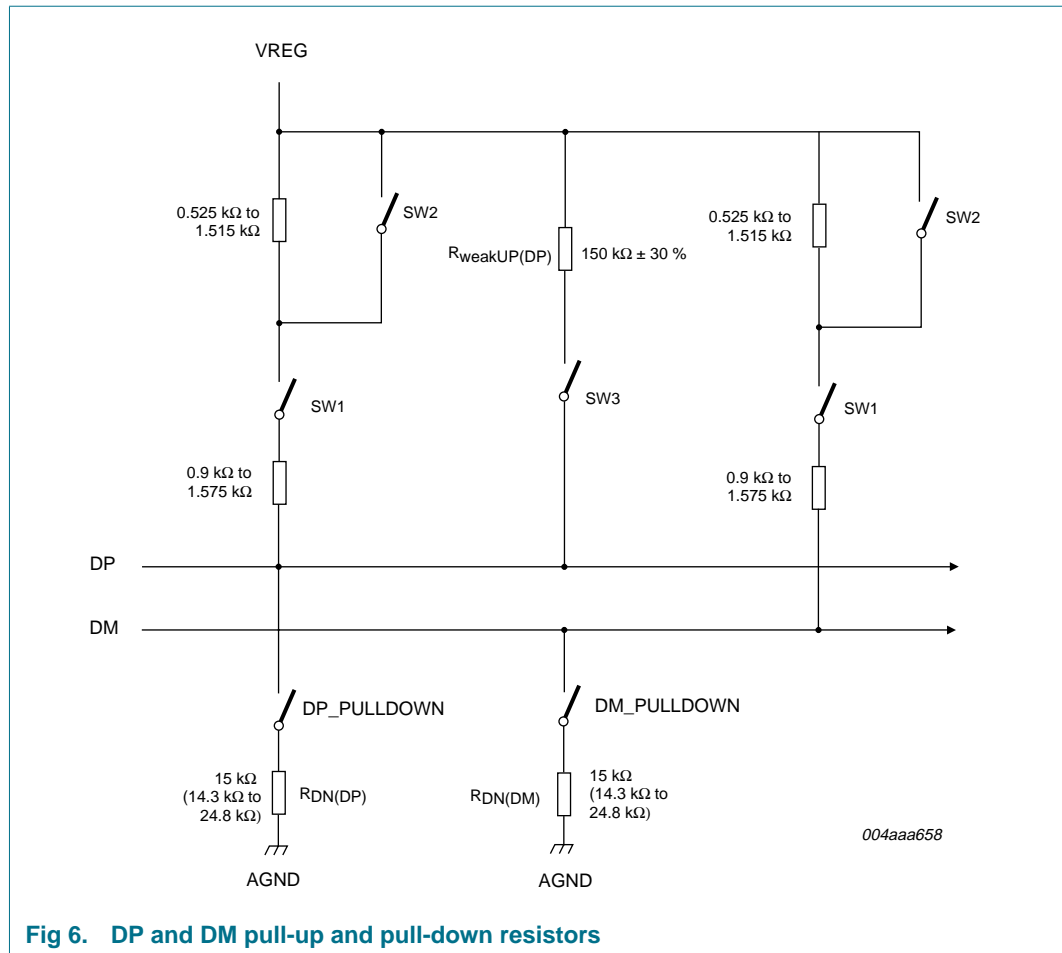
The pull-up resistor is context variable as described in document *ECN_27%_Resistor*. The pull-up resistor value depends on the USB bus condition:

- When the bus is idle, the resistor is 900 Ω to 1575 Ω (SW2 = on).
- When the bus is transmitting or receiving, the resistor is 1425 Ω to 3090 Ω (SW2 = off).

DP also implements a weak pull-up resistor ($R_{weakUP(DP)}$) that is controlled using bit DP_WKPU_EN of the Misc Control register.

The DP pull-down resistor ($R_{DN(DP)}$) is connected to the DP line, if bit DP_PULLDOWN in the OTG Control register is set.

The DM pull-down resistor ($R_{DN(DM)}$) is connected to the DM line, if bit DM_PULLDOWN in the OTG Control register is set.



7.6 3.3 V DC-DC regulator

The built-in DC-DC regulator conditions the input power supply (V_{CC}) for use in the core of the ISP1302.

When V_{CC} is greater than 3.6 V, the regulator will output $3.3 \text{ V} \pm 10 \%$.

When V_{CC} is less than 3.6 V and bit `REG_BYPASS_DIS` = 0, the regulator will be automatically bypassed so that pin VREG will be shorted to pin V_{CC} .

When V_{CC} is less than 3.6 V and bit `REG_BYPASS_DIS` = 1, the regulator will output a voltage between V_{CC} and $V_{CC} - 0.2 \text{ V}$.

The output of the regulator can be monitored on pin VREG. A capacitor (0.1 μF) must be connected between pin VREG and ground.

7.7 Carkit DP interrupt detector

The carkit DP interrupt detector is a comparator that detects the carkit interrupt signal on the CR_INT pin in analog audio mode. Bit `DP_INT` will be set if the voltage level on the CR_INT pin is below the carkit interrupt threshold $V_{th(DP)L}$ (0.4 V to 0.6 V).

The carkit interrupt detector is enabled in audio mode only (bit `AUDIO_EN` = 1).

7.8 Audio bypass

The audio bypass block includes audio switches and DC bias circuits, see [Figure 7](#).

Audio switches provide a low impedance path for analog audio signals from the phone processor to be routed to the DP and DM lines. The impedance of the switches will be between 50 Ω and 150 Ω . [Figure 7](#) shows audio switches and DC biasing circuits.

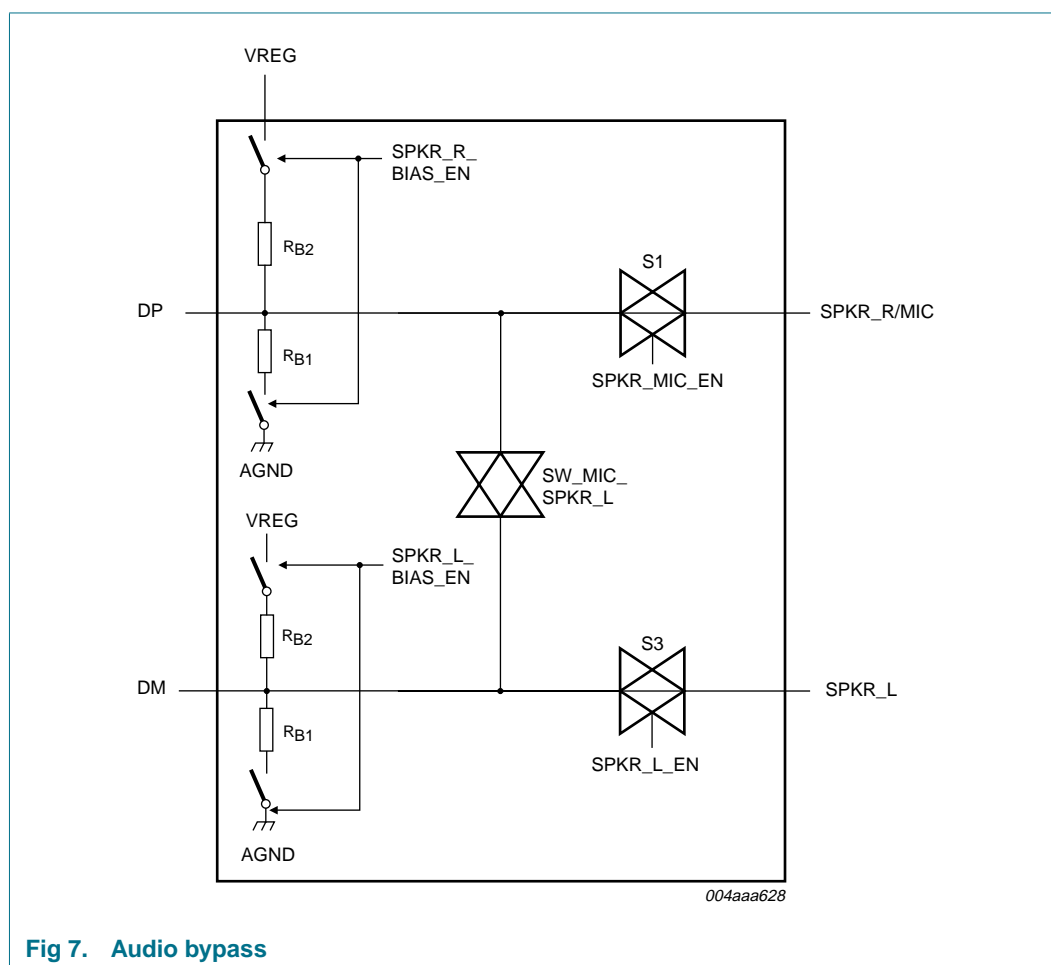


Fig 7. Audio bypass

7.9 Audio data control

[Figure 8](#) shows a diagram that includes the audio data controller. Each block within the audio data controller is described in the following subsections.

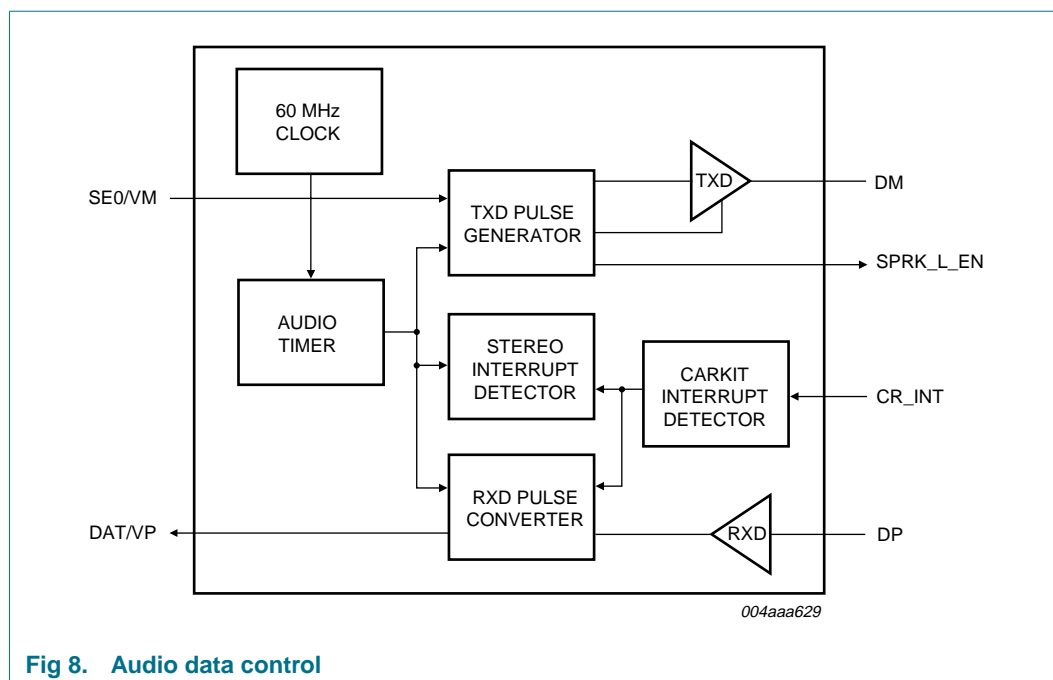


Fig 8. Audio data control

7.9.1 Audio timer

The audio timer has two main functions. The first function is to generate the timing for the positive and negative interrupt pulses. The second function is to generate a time base that can be used to detect a carkit interrupt while in stereo mode, and reset the RxD NRZ signal during data-during-audio.

7.9.2 TxD pulse generator

The TxD pulse generator is enabled when the OTG carkit transceiver is outputting data-during-audio.

When a rising or falling edge is detected on SE0/VM, the TxD pulse generator uses the AUD_TMR_OUT signal to perform the following sequence:

1. 3-state the left speaker buffer.
2. Enable the TxD buffer.
3. Output a HIGH level for the duration of the positive pulse width.
4. Output a LOW level for the duration of the negative pulse width.
5. Disable the TxD buffer.
6. Enable the left speaker buffer.

The delay between a data edge on SE0/VM and a pulse pair being output on DM will jitter by as much as one audio timer period because the audio timer is free running. This is acceptable because the audio timer period is between 200 ns to 500 ns, and the UART data rate is always less than or equal to 115 kbit/s.

7.9.3 Stereo interrupt detector

The stereo interrupt detector generates an interrupt when the CR_INT pin has been continuously below the carkit interrupt detector threshold for a time of $t_{PH_STLO_DET}$ (30 ms to 100 ms); refer to *USB Carkit Specification (CEA-936-A), November 2005*.

7.9.4 RxD pulse converter

When data-during-audio mode is enabled, the RxD pulse converter converts the negative pulses on the DP line to an NRZ signal that is output to the DAT/VP line. Each time a pulse is received, the output on DAT/VP is inverted. If DAT/VP remains at logic 0 for a time of $t_{DAT_AUD_POL}$ (20 ms to 30 ms), then the output on DAT/VP will automatically return to logic 1; refer to *USB Carkit Specification (CEA-936-A), November 2005*.

7.10 Autoconnect

The HNP in the OTG supplement specifies the following sequence of events to transfer the role of the host from the A-device to the B-device:

1. The A-device sets the bus in the suspend state.
2. The B-device simulates a disconnect by de-asserting its DP pull-up.
3. The A-device detects SE0 on the bus and asserts its DP pull-up.
4. The B-device detects that the DP line is HIGH and assumes the role of the host.

The OTG supplement specifies that the time between the B-device de-asserting its DP pull-up and the A-device asserting its pull-up must be less than 3 ms. For an A-device with a slow interrupt response time, 3 ms may not be enough to write an I²C-bus command to the ISP1302 to assert DP pull-up. An alternative method is for the A-device transceiver to automatically assert DP pull-up after detecting an SE0 from the B-device.

The sequence of events is as follows: After finishing data transfers between the A-device and the B-device and before suspending the bus, the A-device sends SOFs. The B-device receives these SOFs, and does not transmit any packet back to the A-device. During this time, the A-device sets the BDIS_ACON_EN bit in the ISP1302. This enables the ISP1302 to look for SE0 whenever the A-device is not transmitting (that is, whenever the OE_N/INT_N pin of the ISP1302 is not asserted). After the BDIS_ACON_EN bit is set, the A-device stops transmitting SOFs and allows the bus to go to the idle state. If the B-device disconnects, the bus goes to SE0, and the ISP1302 logic automatically turns on the A-device pull-up. To disable the DP pull-up resistor, clear bit BDIS_ACON_EN.

7.11 USB transceiver

7.11.1 Differential driver

The operation of the driver is described in [Table 5](#).

Table 5. Transceiver driver operating setting

| Pin | | Bit | | Differential driver |
|------------------------|------------|---------|---------|---|
| RESET_N ^[1] | OE_N/INT_N | SUSPEND | DAT_SE0 | |
| HIGH | LOW | 0 | 0 | output value from DAT/VP to DP and SE0/VM to DM |
| HIGH | LOW | 0 | 1 | output value from DAT/VP to DP and DM if SE0/VM is LOW; otherwise drive both DP and DM to LOW |
| HIGH | LOW | 1 | X | output value from DAT/VP to DP and DM |
| HIGH | HIGH | X | X | high-Z |
| LOW | X | X | X | high-Z |

[1] Include the internal power-on-reset pulse (active HIGH).

[Table 6](#) shows the behavior of the transmit operation in detail.

Table 6. USB functional mode: transmit operation

| USB mode | Inputs | | Outputs | |
|----------|--------|--------|---------|------|
| | DAT/VP | SE0/VM | DP | DM |
| DAT_SE0 | LOW | LOW | LOW | HIGH |
| DAT_SE0 | HIGH | LOW | HIGH | LOW |
| DAT_SE0 | LOW | HIGH | LOW | LOW |
| DAT_SE0 | HIGH | HIGH | LOW | LOW |
| VP_VM | LOW | LOW | LOW | LOW |
| VP_VM | HIGH | LOW | HIGH | LOW |
| VP_VM | LOW | HIGH | LOW | HIGH |
| VP_VM | HIGH | HIGH | HIGH | HIGH |

7.11.2 Differential receiver

The operation of the differential receiver is described in [Table 7](#).

Table 7. Differential receiver operation settings

| Pin | Bit | | Differential receiver |
|------------|---------|---------|--|
| OE_N/INT_N | SUSPEND | DAT_SE0 | |
| HIGH | 0 | 1 | output differential value from DP and DM to DAT/VP and RCV |
| HIGH | 0 | 0 | output differential value from DP and DM to RCV |

The detailed behavior of the receive transceiver operation is shown in [Table 8](#).

Table 8. USB functional mode: receive operation

| USB mode | Bit SUSPEND | Inputs | | Outputs | | |
|----------|-------------|--------|------|---------|--------|-------------------|
| | | DP | DM | DAT/VP | SE0/VM | RCV |
| DAT_SE0 | 0 | LOW | LOW | RCV | HIGH | last value of RCV |
| DAT_SE0 | 0 | HIGH | LOW | HIGH | LOW | HIGH |
| DAT_SE0 | 0 | LOW | HIGH | LOW | LOW | LOW |
| DAT_SE0 | 0 | HIGH | HIGH | RCV | LOW | last value of RCV |
| DAT_SE0 | 1 | LOW | LOW | LOW | HIGH | X |

Table 8. USB functional mode: receive operation ...continued

| USB mode | Bit SUSPEND | Inputs | | Outputs | | |
|----------|-------------|--------|------|---------|--------|-------------------|
| | | DP | DM | DAT/VP | SE0/VM | RCV |
| DAT_SE0 | 1 | HIGH | LOW | HIGH | LOW | X |
| DAT_SE0 | 1 | LOW | HIGH | LOW | LOW | X |
| DAT_SE0 | 1 | HIGH | HIGH | HIGH | LOW | X |
| VP_VM | 0 | LOW | LOW | LOW | LOW | last value of RCV |
| VP_VM | 0 | HIGH | LOW | HIGH | LOW | HIGH |
| VP_VM | 0 | LOW | HIGH | LOW | HIGH | LOW |
| VP_VM | 0 | HIGH | HIGH | HIGH | HIGH | last value of RCV |
| VP_VM | 1 | LOW | LOW | LOW | LOW | X |
| VP_VM | 1 | HIGH | LOW | HIGH | LOW | X |
| VP_VM | 1 | LOW | HIGH | LOW | HIGH | X |
| VP_VM | 1 | HIGH | HIGH | HIGH | HIGH | X |

7.12 Power-On Reset (POR)

When V_{CC} is powered on, an internal POR is generated. The internal POR pulse width (t_{PORP}) will typically be 200 ns. The pulse is started when V_{CC} rises above $V_{POR(trip)}$.

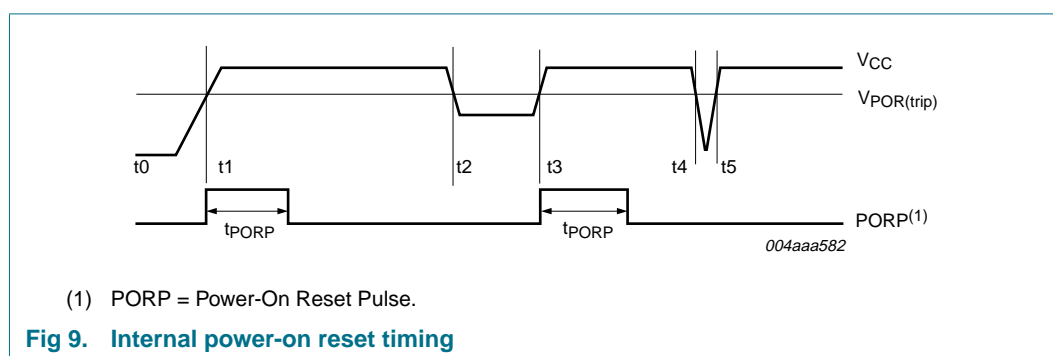
The power-on reset function can be explained by viewing the dips at t_2 to t_3 and t_4 to t_5 on the V_{CC} curve (see [Figure 9](#)).

t0 — The internal POR starts with a LOW level.

t1 — The detector will see the passing of the trip level and a delay element will add another t_{PORP} before it drops to LOW.

t2 to t3 — The internal POR pulse will be generated whenever V_{CC} drops below $V_{POR(trip)}$ for more than 11 μ s.

t4 to t5 — The dip is too short (< 11 μ s) and the internal POR pulse will not react and will remain LOW.



7.13 I²C-bus device address and external charge pump control

The ADR/PSW pin has two functions. Both functions are described as follows.

The first function of the ADR/PSW pin is to set the I²C-bus address. On the rising edge of the RESET_N pin, the level on ADR/PSW is latched and stored in ADR_REG, which represents the Least Significant Bit (LSB) of the I²C-bus address. If ADR_REG = 0, the I²C-bus address for the ISP1302 is 010 1100 (2Ch); if ADR_REG = 1, the I²C-bus address for the ISP1302 is 010 1101 (2Dh). The power-on reset value of ADR_REG = 0.

The second function of the ADR/PSW pin is to control an external charge pump. The ADR/PSW pin can be programmed as an active HIGH or active LOW PSW output. The polarity of the PSW output is determined by ADR_REG. If ADR_REG = 0, then PSW will be active HIGH; if ADR_REG = 1, then PSW will be active LOW. The PSW output will be enabled only when Mode Control 2 register bit PSW_OE = 1. By default, PSW can only drive HIGH if the hardware reset pulse is not issued on RESET_N.

The combinations of I²C-bus address and the PSW polarity are limited, as shown in [Table 9](#).

Table 9. Possible combinations of I²C-bus address and the PSW polarity

| ADR/PSW level on the rising edge of RESET_N | I ² C-bus address | PSW polarity |
|---|------------------------------|--------------|
| LOW | 2Ch | active HIGH |
| HIGH | 2Dh | active LOW |

The ISP1302 built-in charge pump supports V_{BUS} current at 50 mA. If the application needs more current support, an external charge pump may be needed. In this case, the ADR/PSW pin can act as a power switch for the external charge pump. [Figure 10](#) shows an example of using an external charge pump.

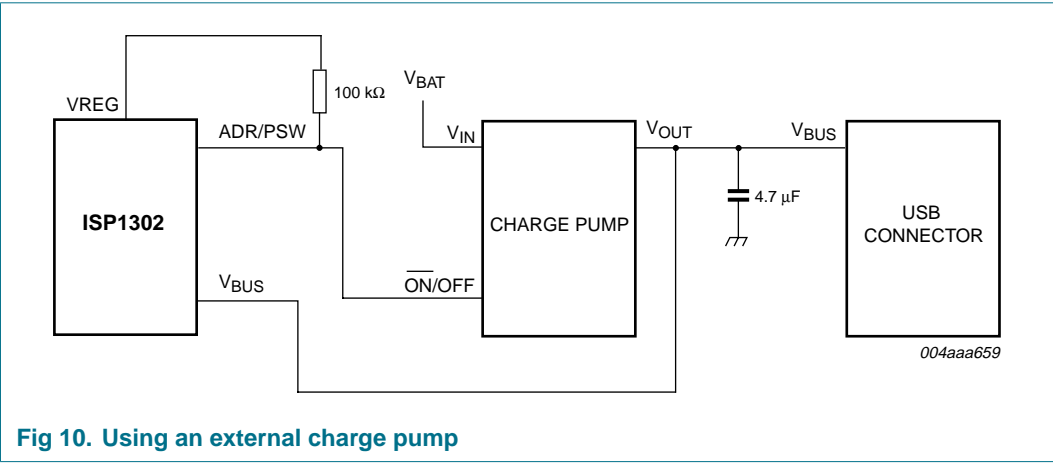


Fig 10. Using an external charge pump

8. Modes of operation

The ISP1302 supports three types of modes:

- Power modes
- USB modes
- Transparent modes

8.1 Power modes

8.1.1 Normal mode

In this mode, both V_{CC} and $V_{CC(I/O)}$ are connected and their voltage levels are within the operation range.

There are three levels of power saving schemes in the ISP1302:

- Active-power mode: power is on; all circuits are active.
- USB suspend mode: to reduce power consumption, the USB differential receiver is powered down.
- Power-down mode: set by writing logic 1 to bit PWR_DN of the Mode Control 2 register. The clock generator and all biasing circuits are turned off to reduce power consumption to the minimum possible. For details on waking up the clock, see [Section 10](#).

8.1.2 Disable mode

In disable mode, $V_{CC(I/O)}$ is cut-off and V_{CC} is powered. In this mode, the ISP1302 is in the power-down state.

The USB differential driver will be 3-stated as long as $V_{CC(I/O)}$ is not present.

8.1.3 Isolate mode

In isolate mode, V_{CC} is cut-off and $V_{CC(I/O)}$ is powered. In this mode, the ISP1302 will drive a stable level to all digital output pins, and all bidirectional digital pins will be set in 3-state.

[Table 10](#) shows a summary of power modes.

Table 10. ISP1302 power modes summary

| V_{CC} | $V_{CC(I/O)}$ | PWR_DN (bit) | $I_{CC} = I_{CC(pd)}$ | Comment |
|----------|---------------|--------------|-----------------------|------------------------------|
| Off | off | X | yes | power off |
| Off | on | X | yes | isolate mode |
| On | off | X | yes | disable mode (power-down) |
| On | on | 0 | no | normal mode (full operation) |
| On | on | 1 | yes | normal mode (power-down) |

[Table 11](#) shows the pin states in disable and isolate modes.

Table 11. ISP1302 pin states in disable and isolate modes

| Pin name | Disable mode ($V_{CC} = \text{on}$, $V_{CC(I/O)} = \text{off}$) | Isolate mode ($V_{CC} = \text{off}$, $V_{CC(I/O)} = \text{on}$) |
|--|--|--|
| V_{CC} , VREG | powered | not present |
| $V_{CC(I/O)}$ | not present | powered |
| DP | 15 k Ω pull-down resistor enabled | high-Z |
| DM | 15 k Ω pull-down resistor enabled | high-Z |
| RCV | high-Z | drive LOW |
| RESET_N, SDA, SCL, ADR/PSW, SE0/VM, DAT/VP, INT_N, OE_N/INT_N, SERVICE_N | high-Z | high-Z |
| SPKR_R/MIC, SPKR_L, ID, V_{BUS} , CR_INT, C_A, C_B | high-Z | high-Z |

8.2 USB modes

The two USB modes of the ISP1302 are:

- VP_VM bidirectional mode
- DAT_SE0 bidirectional mode

In VP_VM USB mode, pin DAT/VP is used for the VP function, pin SE0/VM is used for the VM function, and pin RCV is used for the RCV function.

In DAT_SE0 USB mode, pin DAT/VP is used for the DAT function, pin SE0/VM is used for the SE0 function, and pin RCV is not used.

[Table 12](#) specifies the functionality of the device during the two USB modes.

Table 12. USB functional modes: I/O values

| USB mode ^[1] | Bit | Pin | | | |
|-------------------------|---------|------------|---------------------|---------------------|--------------------|
| | DAT_SE0 | OE_N/INT_N | DAT/VP | SE0/VM | RCV |
| VP_VM | 0 | LOW | TxD+ ^[2] | TxD- ^[2] | RxD ^[6] |
| | | HIGH | RxD+ ^[3] | RxD- ^[3] | RxD ^[6] |
| DAT_SE0 | 1 | LOW | TxD ^[4] | FSE0 ^[5] | RxD ^[6] |
| | | HIGH | RxD ^[6] | RSE0 ^[7] | RxD ^[6] |

[1] Some of the modes and signals are provided to achieve backward compatibility with IP cores.

[2] TxD+ and TxD- are single-ended inputs to drive the DP and DM outputs, respectively, in single-ended mode.

[3] RxD+ and RxD- are the outputs of the single-ended receivers connected to DP and DM, respectively.

[4] TxD is the input to drive DP and DM in DAT_SE0 mode.

[5] FSE0 is to force an SE0 on the DP and DM lines in DAT_SE0 mode.

[6] RxD is the output of the differential receiver.

[7] RSE0 is an output, indicating that an SE0 is received on the DP and DM lines.

8.3 Transparent modes

8.3.1 Transparent UART mode

When in transparent UART mode, an SoC (with the UART controller) communicates through the ISP1302 to another UART device that is connected to its DP and DM lines. The ISP1302 operates as a logic level translator between the following pins:

- For the TxD signal: from SE0/VM ($V_{CC(I/O)}$ level) to DM (VREG level).
- For the RxD signal: from DP (VREG level) to DAT/VP ($V_{CC(I/O)}$ level).

The ISP1302 is in transparent UART mode, if bit UART_EN of the Mode Control 1 register is set.

8.3.2 Transparent audio mode

In transparent audio mode, the ISP1302 will disable its DP and DM driver. The carkit interrupt detector is enabled. Built-in analog switches, DC biasing circuits, and the data-during-audio feature can be enabled by setting corresponding bits in the Carkit Control register:

- Stereo mode: SPKR_L on DM and SPKR_R on DP.
- Mono and MIC mode: SPKR_L on DM and MIC on DP.

The ISP1302 is in transparent audio mode if bit UART_EN of the Mode Control 1 register is cleared, bit AUDIO_EN of the Mode Control 2 register is set, and bit TRANSP_EN of the Mode Control 1 register is cleared.

8.3.3 Transparent general-purpose buffer mode

In transparent general-purpose buffer mode, the DAT/VP and SE0/VM pins are connected to the DP and DM pins, respectively. The direction of the data transfer can be controlled using bits TRANSP_BDIR1 and TRANSP_BDIR0 of the Mode Control 2 register as specified in [Table 14](#).

The ISP1302 is in transparent general-purpose buffer mode, if bit UART_EN = 0, bit AUDIO_EN = 0, bit DAT_SE0 = 1 and bit TRANSP_EN = 1.

8.3.4 Data-during-audio mode

This mode is a combination of audio mode and UART mode. The SPKR_R, SPKR_L and MIC audio signals will be bypassed through the DP and DM lines. UART data bytes can be transmitted or received on the DP and DM lines when the audio signal is running.

To transmit data, if the SE0/VM input changes level (either from HIGH to LOW or from LOW to HIGH), a HIGH pulse will be generated on the DM line. The pulse voltage is above 2.9 V. The pulse width is between 200 ns and 500 ns. The data-during-audio transmitting is enabled when the ISP1302 is in transparent audio mode and bit TX_PULSE_EN = 1.

To receive data, if a LOW pulse is detected on the DP line, the ISP1302 will toggle the level on the DAT/VP pin. The data-during-audio receiving is enabled when the ISP1302 is in transparent audio mode and bit RX_PULSE_EN = 1.

[Table 13](#) provides a summary of device operating modes.

Table 13. Summary of device operating modes

| Mode | Bit | | | | Description |
|---|---------|----------|-----------|---------|---|
| | UART_EN | AUDIO_EN | TRANSP_EN | DAT_SE0 | |
| USB mode | 0 | 0 | 0 | X | USB ATX enabled |
| Transparent general-purpose buffer mode | 0 | 0 | 1 | 1 | USB ATX disabled. SE0/VM ↔ DM DAT/VP ↔ DP see Table 14 |
| Transparent audio mode | 0 | 1 | 0 | X | USB ATX disabled. SPKR_L → DM SPKR_R/MIC ↔ DP |
| Transparent UART mode | 1 | X | X | X | USB ATX disabled. SE0/VM → DM DAT/VP ← DP |

Table 14. Transparent general-purpose buffer mode

| Bit TRANSP_BDIR[1:0] | Direction of the data flow | |
|----------------------|----------------------------|-------------|
| 00 | DAT/VP → DP | SE0/VM → DM |
| 01 | DAT/VP → DP | SE0/VM ← DM |
| 10 | DAT/VP ← DP | SE0/VM → DM |
| 11 | DAT/VP ← DP | SE0/VM ← DM |

9. Serial controller

9.1 Register map

[Table 15](#) provides an overview of serial controller registers.

Table 15. Register overview

| Register | Width (bits) | Access | Memory address ^[1] | Functionality | Reference |
|---------------------------|--------------|--------|--|---------------------------------|--|
| Vendor ID | 16 | R | 00h to 01h | device identification registers | Section 9.1.1 on page 22 |
| Product ID | 16 | R | 02h to 03h | | |
| Version ID | 16 | R | 14h to 15h | | |
| Mode Control 1 | 8 | R/S/C | Set — 04h Clear — 05h | control and status registers | Section 9.1.2 on page 23 |
| Mode Control 2 | 8 | R/S/C | Set — 12h Clear — 13h | | |
| Audio Control | 8 | R/S/C | Set — 16h Clear — 17h | | |
| OTG Control | 8 | R/S/C | Set — 06h Clear — 07h | | |
| Misc Control | 8 | R/S/C | Set — 18h Clear — 19h | | |
| Carkit Control | 8 | R/S/C | Set — 1Ah Clear — 1Bh | | |
| Transmit Positive Width | 8 | R/W | 1Ch | | |
| Transmit Negative Width | 8 | R/W | 1Dh | | |
| Receive Polarity Recovery | 8 | R/W | 1Eh | | |
| Carkit Interrupt Delay | 8 | R/W | 1Fh | | |
| OTG Status | 8 | R | 10h | interrupt registers | Section 9.1.3 on page 29 |
| Interrupt Source | 8 | R | 08h | | |
| Interrupt Latch | 8 | R/S/C | Set — 0Ah Clear — 0Bh | | |
| Interrupt Enable Low | 8 | R/S/C | Set — 0Ch Clear — 0Dh | | |
| Interrupt Enable High | 8 | R/S/C | Set — 0Eh Clear — 0Fh | | |

- [1] The R/W/S/C access type represents a field that can be read, written, set or cleared (set to 0). A register can be read from either of the set or clear addresses. Writing to a write address indicates that values will be directly written to the register. Writing logic 1 to a set address sets the associated bit. Writing logic 1 to a clear address clears the associated bit. Writing logic 0 to either a set or clear address has no effect.

9.1.1 Device identification registers

9.1.1.1 Vendor ID register

[Table 16](#) provides the bit description of the Vendor ID register.

Table 16. Vendor ID register (address R = 00h to 01h) bit description

| Bit | Symbol | Access | Value | Description |
|---------|----------------|--------|-------|-------------------------------|
| 15 to 0 | VENDORID[15:0] | R | 04CCh | NXP Semiconductors' Vendor ID |

9.1.1.2 Product ID register

The bit description of the Product ID register is given in [Table 17](#).

Table 17. Product ID register (address R = 02h to 03h) bit description

| Bit | Symbol | Access | Value | Description |
|---------|-----------------|--------|-------|---------------------------|
| 15 to 0 | PRODUCTID[15:0] | R | 1302h | Product ID of the ISP1302 |

9.1.1.3 Version ID register

[Table 18](#) shows the bit allocation of the register.

Table 18. Version ID register (address R = 14h to 15h) bit allocation

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|--------|------------------|----|----|----|---------------|----|---|---|
| Symbol | PACKAGEID[3:0] | | | | LEGACYID[3:0] | | | |
| Reset | X ^[1] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Symbol | MAJORID[3:0] | | | | MINORID[3:0] | | | |
| Reset | X ^[1] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |

[1] The reset value depends on the version number of the chip.

Table 19. Version ID register (address R = 14h to 15h) bit description

| Bit | Symbol | Description |
|----------|----------------|---|
| 15 to 12 | PACKAGEID[3:0] | Package information: 0 — HVQFN24 1 — WLCSP25 |
| 11 to 8 | LEGACYID[3:0] | Legacy version ID: 0 — New method of defining the version ID 1 to 15 — Legacy method of defining the version ID |
| 7 to 4 | MAJORID[3:0] | Version ID, major number; this number starts with 1 and increments by 1 if there is a major update to the chip. |
| 3 to 0 | MINORID[3:0] | Version ID, minor number; this number starts with 0 and increments by 1 if there is a minor update to the chip. |

9.1.2 Control registers**9.1.2.1 Mode Control 1 register**

The bit allocation of the Mode Control 1 register is given in [Table 20](#).

Table 20. Mode Control 1 register (address S = 04h, C = 05h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|---------|-----------|--------------|-----------|---------|---------|-------|
| Symbol | reserved | UART_EN | OE_INT_EN | BDIS_ACON_EN | TRANSP_EN | DAT_SE0 | SUSPEND | SPEED |
| Reset | 0 | 0/1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C |

Table 21. Mode Control 1 register (address S = 04h, C = 05h) bit description

| Bit | Symbol | Description |
|-----|--------------|--|
| 7 | - | reserved |
| 6 | UART_EN | When set, the ATX is in transparent UART mode. The default value of this bit depends on the SERVICE_N pin. On reset, if SERVICE_N = HIGH, the reset value of UART_EN = 0; if SERVICE_N = LOW, the reset value of UART_EN = 1. |
| 5 | OE_INT_EN | When set and when in suspend mode, pin OE_N/INT_N becomes an output and is asserted when an interrupt occurs. |
| 4 | BDIS_ACON_EN | This bit has two functions: For an A-device, this bit works as BDIS_ACON_EN. It enables the A-device to connect if the B-device disconnect is detected; see Section 7.10 . 0 — DP pull-up resistor is controlled by the DP_PULLUP bit in the OTG Control register. 1 — DP pull-up resistor will connect on the B-device disconnect. For a B-device, this bit works as ACON_BSE0_EN. It enables the B-device to drive SE0 on DP and DM, if the A-device connect is detected. 0 — B-device will stop driving SE0. 1 — B-device will start to drive SE0, if the A-device connect is detected. |
| 3 | TRANSP_EN | When set, the ATX is in transparent general-purpose buffer mode. |
| 2 | DAT_SE0 | 0 — VP_VM mode 1 — DAT_SE0 mode |
| 1 | SUSPEND | Sets the transceiver in low-power mode. 0 — Active-power mode 1 — Low-power mode (differential receiver is disabled if SPEED = 1) |
| 0 | SPEED | Set the rise time and the fall time of the transmit driver in USB modes. 0 — Low-speed mode 1 — Full-speed mode |

9.1.2.2 Mode Control 2 register

For the bit allocation of this register, see [Table 22](#).

Table 22. Mode Control 2 register (address S = 12h, C = 13h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|--------|----------|--------------|--------------|----------|-------|--------|
| Symbol | reserved | PSW_OE | AUDIO_EN | TRANSP_BDIR1 | TRANSP_BDIR0 | reserved | | PWR_DN |
| Reset | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Access | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C |

Table 23. Mode Control 2 register (address S = 12h, C = 13h) bit description

| Bit | Symbol | Description |
|--------|-------------------|--|
| 7 | - | reserved |
| 6 | PSW_OE | 0 — ADR/PSW pin acts as an input. 1 — ADR/PSW pin is driven. |
| 5 | AUDIO_EN | Enables the ISP1302 in carkit audio mode. 0 — Audio mode disable: DP_INT detector is turned off, and single-ended receivers are turned on. 1 — Audio mode enable: DP_INT detector is turned on, and single-ended receivers are turned off. |
| 4 to 3 | TRANSP_BDIR [1:0] | Controls the direction of data transfer in transparent general-purpose buffer mode; see Table 14 |
| 2 to 1 | - | reserved |
| 0 | PWR_DN | Set to power-down mode; activities on pin SCL or the interrupt event can wake-up the chip; see Section 10 |

9.1.2.3 Audio Control register

[Table 24](#) provides the bit allocation of the register.

Table 24. Audio Control register (address S = 16h, C = 17h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------|-----------|----------|-------|-------|-------|---------------|----------|
| Symbol | PH_ID_ACK | PH_ID_INT | reserved | | | | SW_MIC_SPKR_L | reserved |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C |

Table 25. Audio Control register (address S = 16h, C = 17h) bit description

| Bit | Symbol | Description |
|--------|---------------|--|
| 7 | PH_ID_ACK | If set, wait for time $t_{PH_ID_WT}$, turn on the ID pull-down switch for $t_{PH_ID_INT}$, then turn off. Bit PH_ID_ACK aut clears to 0. See Table 4 . |
| 6 | PH_ID_INT | If set, turn on the ID pull-down switch for time $t_{PH_ID_INT}$ and then turn off. Bit PH_ID_INT aut clears to 0. See Table 4 . |
| 5 to 2 | - | reserved |
| 1 | SW_MIC_SPKR_L | Audio loopback test: 0 — Turn off the switch between the SPKR_R/MIC and SPKR_L pins. 1 — Turn on the switch between the SPKR_R/MIC and SPKR_L pins. |
| 0 | - | reserved |

9.1.2.4 OTG Control register

[Table 26](#) shows the bit allocation of the OTG Control register.

Table 26. OTG Control register (address S = 06h, C = 07h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------|--------------|----------|------------|--------------|--------------|------------|------------|
| Symbol | VBUS_CHRG | VBUS_DISCHRG | VBUS_DRV | ID_PULL_DN | DM_PULL_DOWN | DP_PULL_DOWN | DM_PULL_UP | DP_PULL_UP |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Access | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C |

Table 27. OTG Control register (address S = 06h, C = 07h) bit description

| Bit | Symbol | Description |
|-----|--------------|--|
| 7 | VBUS_CHRG | Charge V_{BUS} through a pull-up resistor ($R_{UP(VBUS)}$), which is connected to VREG. 0 — Disconnect the resistor 1 — Connect the resistor |
| 6 | VBUS_DISCHRG | Discharge V_{BUS} through a pull-down resistor ($R_{DN(VBUS)}$). 0 — Disconnect the resistor 1 — Connect the resistor |
| 5 | VBUS_DRV | Drive V_{BUS} to 5 V through the charge pump. 0 — Charge pump is disabled 1 — Charge pump is enabled |
| 4 | ID_PULLDN | Connect pin ID to ground. See Table 5 . 0 — Disconnected 1 — Connected |
| 3 | DM_PULLDOWN | Connect the DM pull-down resistor ($R_{DN(DM)}$). 0 — DM pull-down resistor is disconnected 1 — DM pull-down resistor is connected |
| 2 | DP_PULLDOWN | Connect the DP pull-down resistor ($R_{DN(DP)}$). 0 — DP pull-down resistor is disconnected 1 — DP pull-down resistor is connected |
| 1 | DM_PULLUP | Connect the DM pull-up resistor ($R_{UP(DM)}$). 0 — DM pull-up resistor is disconnected 1 — DM pull-up resistor is connected |
| 0 | DP_PULLUP | Connect the DP pull-up resistor ($R_{UP(DP)}$). 0 — DP pull-up resistor is disconnected (assuming that bit BDIS_ACON_EN is logic 0) 1 — DP pull-up resistor is connected |

9.1.2.5 Misc Control register

[Table 28](#) shows the bit allocation of the register.

Table 28. Misc Control register (address S = 18h, C = 19h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---------------|--------------|----------|-------------|----------|------------|----------|-----------------|
| Symbol | FORCE_DP_HIGH | FORCE_DP_LOW | reserved | UART_2V8_EN | IDPU_DIS | DP_WKPU_EN | SRP_INIT | REG_BY_PASS_DIS |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Access | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C |

Table 29. Misc Control register (address S = 18h, C = 19h) bit description

| Bit | Symbol | Description |
|-----|---------------|--|
| 7 | FORCE_DP_HIGH | Forces the DP pin to be driven to HIGH |
| 6 | FORCE_DP_LOW | Forces the DP pin to be driven to LOW |
| 5 | - | reserved |

Table 29. Misc Control register (address S = 18h, C = 19h) bit description ...continued

| Bit | Symbol | Description |
|-----|----------------|--|
| 4 | UART_2V8_EN | This bit indicates the output voltage level of the internal regulator. This bit is only valid when bit UART_EN is logic 1. When this bit and bit UART_EN are logic 1, the internal regulator bypass switch will always be disabled, ignoring the value of bit REG_BYPASS_DIS. This is to ensure that the internal regulator outputs +2.8 V, when V _{CC} is 3.0 V to 4.5 V. 0 — Internal regulator outputs 3.3 V 1 — Internal regulator outputs 2.8 V |
| 3 | IDPU_DIS | 0 — Internal ID pin pull-up resistor is enabled 1 — Internal ID pin pull-up resistor is disabled |
| 2 | DP_WKPU_EN | This bit will enable R _{weakUP(DP)} on the DP line. It is provided to support the detection of external accessory devices. This bit is optional. 0 — Disconnect the DP weak pull-up resistor (R _{weakUP(DP)}) 1 — Connect the DP weak pull-up resistor (R _{weakUP(DP)}) |
| 1 | SRP_INIT | 0 — No event 1 — Initialize SRP, if this bit is set, the following events occur in sequence: enable DP pull-up for 7.5 ms, enable the VBUS_CHRG resistor for 32 ms, enable the VBUS_DISCHRG resistor for 13 ms. This bit will autoclear when the sequence is complete. |
| 0 | REG_BYPASS_DIS | 0 — Internal regulator bypass switch is turned on, when V _{CC} < 3.6 V 1 — Internal regulator bypass switch is turned off |

9.1.2.6 Carkit Control register

Table 30 shows the bit allocation of this register.

Table 30. Carkit Control register (address S = 1Ah, C = 1Bh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|-------|-------------|-----------|----------------|----------------|-------------|-------------|
| Symbol | reserved | | SPKR_MIC_EN | SPKR_L_EN | SPKR_R_BIAS_EN | SPKR_L_BIAS_EN | RX_PULSE_EN | TX_PULSE_EN |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C |

Table 31. Carkit Control register (address S = 1Ah, C = 1Bh) bit description

| Bit | Symbol | Description |
|--------|----------------|--|
| 7 to 6 | - | reserved |
| 5 | SPKR_MIC_EN | Enables the speaker right or MIC line switch |
| 4 | SPKR_L_EN | Enables the speaker left line switch |
| 3 | SPKR_R_BIAS_EN | Enables the DC bias for the speaker right line |
| 2 | SPKR_L_BIAS_EN | Enables the DC bias for the speaker left line |
| 1 | RX_PULSE_EN | Enables the data-during-audio receive |
| 0 | TX_PULSE_EN | Enables the data-during-audio transmit |

9.1.2.7 Transmit Positive Width register

This register specifies the width of the positive pulse, that is, the output on the DM line when the TX_PULSE_EN bit is set. The time is measured in units of 60 MHz clock periods. The clock has a frequency in the range of $f_{clk(dda)}$. For bit description, see [Table 32](#).

Table 32. Transmit Positive Width register (address R/W = 1Ch) bit description

Legend: * reset value

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-------|-------------------------------|
| 7 to 0 | TXPOSIWIDTH[7:0] | R/W | 15h* | Transmit positive pulse width |

9.1.2.8 Transmit Negative Width register

This register specifies the width of the negative pulse, that is, the output on the DM line when the TX_PULSE_EN bit is set. The time is measured in units of 60 MHz clock periods. The clock has a frequency in the range of $f_{clk(dda)}$. For the bit description, see [Table 33](#).

Table 33. Transmit Negative Width register (address R/W = 1Dh) bit description

Legend: * reset value

| Bit | Symbol | Access | Value | Description |
|--------|-----------------|--------|-------|-------------------------------|
| 7 to 0 | TXNEGWIDTH[7:0] | R/W | 2Ah* | Transmit negative pulse width |

9.1.2.9 Receive Polarity Recovery register

The bit description of the register is shown in [Table 34](#).

Table 34. Receive Polarity Recovery register (address R/W = 1Eh) bit description

Legend: * reset value

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-------|---|
| 7 to 0 | RX_RECOVERY[7:0] | R/W | 64h* | Sets the RxD polarity recovery time in units of 0.25 ms. The timer tolerance is dictated by $f_{clk(dda)}$. Valid when bit RX_PULSE_EN is set. |

9.1.2.10 Carkit Interrupt Delay register

The bit description of the register is given in [Table 35](#).

Table 35. Carkit Interrupt Delay register (address R/W = 1Fh) bit description

Legend: * reset value

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|---|
| 7 to 0 | CR_INT_DELAY[7:0] | R/W | C8h* | Sets the carkit interrupt detection time in units of 0.25 ms. The timer tolerance is dictated by $f_{clk(dda)}$. |

9.1.2.11 OTG Status register

[Table 36](#) shows the bit allocation of the OTG Status register.

Table 36. OTG Status register (address R = 10h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|------------|----------|---|---------|---------|---------|----------|
| Symbol | reserved | B_SESS_END | reserved | | ID_102K | ID_440K | ID_200K | reserved |
| Reset | 0 | -[1] | 0 | 0 | -[1] | -[1] | -[1] | 0 |
| Access | R | R | R | R | R | R | R | R |

[1] The reset value depends on the status of the respective pin.

Table 37. OTG Status register (address R = 10h) bit description

| Bit | Symbol | Description |
|--------|------------|---|
| 7 | - | reserved |
| 6 | B_SESS_END | Set when the V_{BUS} voltage is below the B-device session end threshold (0.2 V to 0.8 V). In power-down mode, this bit is fixed as logic 0. |
| 5 to 4 | - | reserved |
| 3 | ID_102K | Indicates that pin ID is connected to ground through $R_{DN(ID)} = 102\text{ k}\Omega$. This bit indicates that the phone accessory is connected. For details, refer to <i>USB Carkit Specification (CEA-936-A)</i> . In power-down mode, this bit is fixed as logic 0. |
| 2 | ID_440K | Indicates that pin ID is connected to ground through $R_{DN(ID)} = 440\text{ k}\Omega$. This bit indicates the default current capability of the connected charger. For details, refer to <i>USB Carkit Specification (CEA-936-A)</i> . In power-down mode, this bit is fixed as logic 0. |
| 1 | ID_200K | Indicates that pin ID is connected to ground through $R_{DN(ID)} = 200\text{ k}\Omega$. This bit indicates the default current capability of the connected charger. For details, refer to <i>USB Carkit Specification (CEA-936-A)</i> . In power-down mode, this bit is fixed as logic 0. |
| 0 | - | reserved |

9.1.3 Interrupt registers

9.1.3.1 Interrupt Source register

Table 38 shows the bit allocation of this register that indicates the current state of the signals that can generate an interrupt.

Table 38. Interrupt Source register (address R = 08h) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|-----------|----------|-------|--------|-------|----------|----------|
| Symbol | DP_INT | BDIS_ACON | ID_FLOAT | DM_HI | ID_GND | DP_HI | SESS_VLD | VBUS_VLD |
| Reset | -[1] | 0 | -[1] | -[1] | -[1] | -[1] | -[1] | -[1] |
| Access | R | R | R | R | R | R | R | R |

[1] The reset value depends on the status of the respective pin.

Table 39. Interrupt Source register (address R = 08h) bit description

| Bit | Symbol | Description |
|-----|-----------|--|
| 7 | DP_INT | <p>This bit has two functions:</p> <p>When the Carkit Interrupt Delay register is 0h and the voltage on the CR_INT pin is below the carkit interrupt threshold (0.4 V to 0.6 V), this bit is set.</p> <p>0 — Voltage on the CR_INT pin is above the carkit interrupt threshold (0.4 V to 0.6 V).</p> <p>1 — Voltage on the CR_INT pin is below the carkit interrupt threshold (0.4 V to 0.6 V).</p> <p>When the Carkit Interrupt Delay register is nonzero and the voltage on the CR_INT pin is below the carkit interrupt threshold (0.4 V to 0.6 V) for a period of time defined in the Carkit Interrupt Delay register, this bit is set.</p> <p>0 — No event</p> <p>1 — The carkit stereo interrupt event is detected.</p> <p>In power-down mode, this bit is fixed as logic 0.</p> |
| 6 | BDIS_ACON | <p>Set when bit BDIS_ACON_EN is set, and the ISP1302 enables the DP pull-up resistor after detecting the B-device disconnect (SE0).</p> <p>0 — No event</p> <p>1 — BDIS_ACON is detected.</p> |
| 5 | ID_FLOAT | <p>Indicates the status of pin ID.</p> <p>0 — ID pin is not floating.</p> <p>1 — ID pin is floating.</p> |
| 4 | DM_HI | <p>DM single-ended receiver output.</p> <p>0 — LOW</p> <p>1 — HIGH</p> |
| 3 | ID_GND | <p>Indicates the status of pin ID:</p> <p>0 — ID pin is not grounded.</p> <p>1 — ID pin is grounded.</p> <p>In power-down mode, this bit is fixed as logic 0.</p> |
| 2 | DP_HI | <p>DP single-ended receiver output.</p> <p>0 — LOW</p> <p>1 — HIGH</p> |
| 1 | SESS_VLD | <p>V_{BUS} session valid detector.</p> <p>0 — V_{BUS} is lower than V_{A_SESS_VLD} (bit ID_GND = 1) or V_{B_SESS_VLD} (bit ID_GND = 0).</p> <p>1 — V_{BUS} is higher than V_{A_SESS_VLD} (bit ID_GND = 1) or V_{B_SESS_VLD} (bit ID_GND = 0).</p> |
| 0 | VBUS_VLD | <p>This bit has two functions:</p> <p>For the A-device (bit ID_GND = 1), it acts as the V_{BUS} valid detector.</p> <p>0 — V_{BUS} is lower than the V_{BUS} valid threshold.</p> <p>1 — V_{BUS} is higher than the V_{BUS} valid threshold.</p> <p>For the B-device (bit ID_GND = 0), it acts as B_SESS_END (B-device session end detector).</p> <p>0 — V_{BUS} is above the B-device session end threshold (0.2 V to 0.8 V).</p> <p>1 — V_{BUS} is below the B-device session end threshold (0.2 V to 0.8 V).</p> <p>In power-down mode, this bit is fixed as logic 0.</p> |

9.1.3.2 Interrupt Latch register

This register indicates the source that generates an interrupt. For the bit allocation, see [Table 40](#).

Table 40. Interrupt Latch register (address S = 0Ah, C = 0Bh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|---------------|--------------|-----------|------------|-----------|--------------|--------------|
| Symbol | DP_INT_INT | BDIS_ACON_INT | ID_FLOAT_INT | DM_HI_INT | ID_GND_INT | DP_HI_INT | SESS_VLD_INT | VBUS_VLD_INT |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C |

Table 41. Interrupt Latch register (address S = 0Ah, C = 0Bh) bit description

| Bit | Symbol | Description |
|-----|---------------|--|
| 7 | DP_INT_INT | 0 — No interrupt 1 — Interrupt on the DP_INT status change |
| 6 | BDIS_ACON_INT | 0 — No interrupt 1 — Interrupt on the BDIS_ACON status change |
| 5 | ID_FLOAT_INT | 0 — No interrupt 1 — Interrupt on the ID_FLOAT status change |
| 4 | DM_HI_INT | 0 — No interrupt 1 — Interrupt on the DM_HI status change |
| 3 | ID_GND_INT | 0 — No interrupt 1 — Interrupt on the ID_GND status change |
| 2 | DP_HI_INT | 0 — No interrupt 1 — Interrupt on the DP_HI status change |
| 1 | SESS_VLD_INT | 0 — No interrupt 1 — Interrupt on the SESS_VLD status change |
| 0 | VBUS_VLD_INT | 0 — No interrupt 1 — Interrupt on the VBUS_VLD status change |

9.1.3.3 Interrupt Enable Low register

The bits in this register enable interrupts when the corresponding bits in the Interrupt Source register change from logic 1 to logic 0. [Table 42](#) shows the bit allocation of the register.

Table 42. Interrupt Enable Low register (address S = 0Ch, C = 0Dh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|----------|--------------|-----------|------------|-----------|--------------|--------------|
| Symbol | DP_INT_IEL | reserved | ID_FLOAT_IEL | DM_HI_IEL | ID_GND_IEL | DP_HI_IEL | SESS_VLD_IEL | VBUS_VLD_IEL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C |

Table 43. Interrupt Enable Low register (address S = 0Ch, C = 0Dh) bit description

| Bit | Symbol | Description |
|-----|--------------|---------------------------|
| 7 | DP_INT_IEL | 0 — Disable 1 — Enable |
| 6 | - | reserved |
| 5 | ID_FLOAT_IEL | 0 — Disable 1 — Enable |
| 4 | DM_HI_IEL | 0 — Disable 1 — Enable |
| 3 | ID_GND_IEL | 0 — Disable 1 — Enable |
| 2 | DP_HI_IEL | 0 — Disable 1 — Enable |
| 1 | SESS_VLD_IEL | 0 — Disable 1 — Enable |
| 0 | VBUS_VLD_IEL | 0 — Disable 1 — Enable |

9.1.3.4 Interrupt Enable High register

The bits in this register enable interrupts when the corresponding bits in the Interrupt Source register change from logic 0 to logic 1. For the bit allocation, see [Table 44](#).

Table 44. Interrupt Enable High register (address S = 0Eh, C = 0Fh) bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|------------|---------------|--------------|-----------|------------|-----------|--------------|--------------|
| Symbol | DP_INT_IEH | BDIS_ACON_IEH | ID_FLOAT_IEH | DM_HI_IEH | ID_GND_IEH | DP_HI_IEH | SESS_VLD_IEH | VBUS_VLD_IEH |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C | R/S/C |

Table 45. Interrupt Enable High register (address S = 0Eh, C = 0Fh) bit description

| Bit | Symbol | Description |
|-----|---------------|---------------------------|
| 7 | DP_INT_IEH | 0 — Disable 1 — Enable |
| 6 | BDIS_ACON_IEH | 0 — Disable 1 — Enable |
| 5 | ID_FLOAT_IEH | 0 — Disable 1 — Enable |
| 4 | DM_HI_IEH | 0 — Disable 1 — Enable |
| 3 | ID_GND_IEH | 0 — Disable 1 — Enable |

Table 45. Interrupt Enable High register (address S = 0Eh, C = 0Fh) bit description

| Bit | Symbol | Description |
|-----|--------------|---------------------------|
| 2 | DP_HI_IEH | 0 — Disable 1 — Enable |
| 1 | SESS_VLD_IEH | 0 — Disable 1 — Enable |
| 0 | VBUS_VLD_IEH | 0 — Disable 1 — Enable |

9.2 Interrupts

Any of the Interrupt Source register signals given in Table 38 can generate an interrupt, when the signal becomes either LOW or HIGH. After an interrupt is generated, the SoC should be able to read the status of each signal and the bit that indicates whether that signal generated the interrupt. A bit in the Interrupt Latch register is set when any of the following events occurs:

- Writing logic 1 to a set address sets the corresponding bit.
- The corresponding bit in the Interrupt Enable High register is set, and the associated signal changes from LOW to HIGH.
- The corresponding bit in the Interrupt Enable Low register is set, and the associated signal changes from HIGH to LOW.
- The INT_N pin will be asserted if one or more bits in the Interrupt Latch register are set. The INT_N pin will be de-asserted if all the bits in the Interrupt Latch register are cleared by software.

9.3 I²C-bus protocol

For detailed information, refer to *The I²C-bus specification; ver. 2.1*.

9.3.1 I²C-bus byte transfer format

Table 46. I²C-bus byte transfer format

| S ^[1] | Byte 1 | A ^[2] | Byte 2 | A ^[2] | Byte 3 | A ^[2] | .. | A ^[2] | P ^[3] |
|------------------|--------|------------------|--------|------------------|--------|------------------|----|------------------|------------------|
| | 8 bits | | 8 bits | | 8 bits | | .. | | |

[1] S = Start.

[2] A = Acknowledge.

[3] P = Stop.

9.3.2 I²C-bus device address

Table 47. I²C-bus slave address bit allocation

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----|----|----|----|----|----|----------------|-----|
| Symbol | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| Value | 0 | 1 | 0 | 1 | 1 | 0 | ^[1] | X |

[1] Determined by the status of the ADR/PSW pin on the rising edge of RESET_N. If ADR/PSW = HIGH, bit A0 = 1; if ADR/PSW = LOW, bit A0 = 0. Bit A0 will be zero if there is no hardware reset pulse on the RESET_N pin after power on.

Table 48. I²C-bus slave address bit description

| Bit | Symbol | Description |
|--------|--------|--|
| 7 to 1 | A[6:0] | Device Address: The device address of the ISP1302 is 01 0110 (A0), where A0 is determined by pin ADR/PSW. |
| 0 | R/W | Read or write command. 0 — Write 1 — Read |

9.3.3 Write format

A write operation can be performed as:

- One-byte write to the specified register address.
- Multiple-byte write to N consecutive registers, starting from the specified start address. N defines the number of registers to write. If N = 1, only the start register is written.

9.3.3.1 One-byte write

[Table 49](#) describes the transfer format for a one-byte write.

Table 49. Transfer format description for a one-byte write

| Byte | Description |
|--------------------|---|
| S | master starts with a START condition |
| Device select | master transmits the device address and write command bit R/W = 0 |
| ACK | slave generates an acknowledgment |
| Register address K | master transmits the address of register K |
| ACK | slave generates an acknowledgment |
| Write data K | master writes data to register K |
| ACK | slave generates an acknowledgment |
| P | master generates a STOP condition |

9.3.3.2 Multiple-byte write

[Table 50](#) describes the transfer format for multiple-byte write.

Table 50. Transfer format description for a multiple-byte write

| Byte | Description |
|--------------------|---|
| S | master starts with a START condition |
| Device select | master transmits the device address and write command bit R/W = 0 |
| ACK | slave generates an acknowledgment |
| Register address K | master transmits the address of register K. This is the start address for writing multiple data bytes to consecutive registers. After a byte is written, the register address is automatically incremented by 1. Remark: If the master writes to a nonexistent register, the slave must send a 'not ACK' and also must not increment the index address. |
| ACK | slave generates an acknowledgment |
| Write data K | master writes data to register K |
| ACK | slave generates an acknowledgment |
| Write data K + 1 | master writes data to register K + 1 |

Table 50. Transfer format description for a multiple-byte write ...continued

| Byte | Description |
|----------------------|---|
| ACK | slave generates an acknowledgment |
| : | : |
| Write data K + N – 1 | master writes data to register K + N – 1. When the incremented address K + N – 1 becomes > 255, the register address rolls over to 0. Therefore, it is possible that some registers may be overwritten, if the transfer is not stopped before the rollover. |
| ACK | slave generates an acknowledgment |
| P | master generates a STOP condition |

Figure 11 illustrates the write format for a one-byte write and a multiple-byte write.

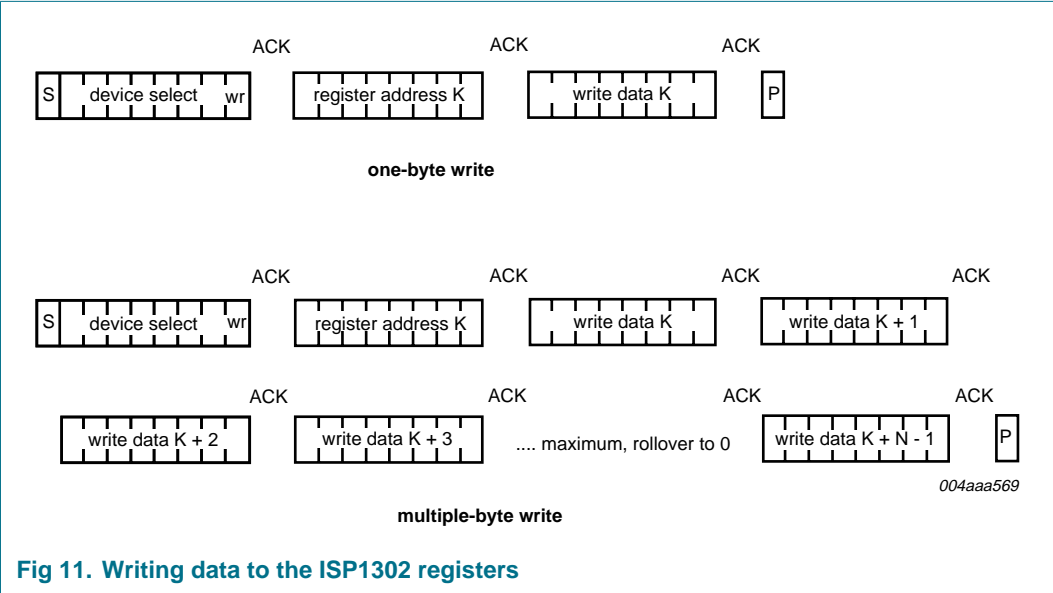


Fig 11. Writing data to the ISP1302 registers

9.3.4 Read format

A read operation can be performed in two ways:

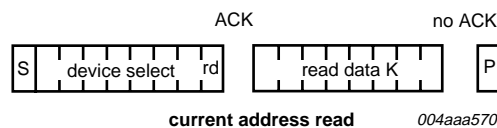
- Current address read: To read the register at the current address.
 - Single register read
- Random address read: To read N registers starting at a specified address. N defines the number of registers to be read. If N = 1, only the start register is read.
 - Single register read
 - Multiple register read

9.3.4.1 Current address read

The transfer format description for a current address read is given in Table 51. For the illustration, see Figure 12.

Table 51. Transfer format description for current address read

| Byte | Description |
|---------------|---|
| S | master starts with a START condition |
| Device select | master transmits the device address and read command bit R/W = 1 |
| ACK | slave generates an acknowledgment |
| Read data K | slave transmits and master reads data from register K. If the start address is not specified, the read operation starts from where the index register is pointing to because of a previous read or write operation. |
| No ACK | master terminates the read operation by generating a no acknowledgement |
| P | master generates a stop condition |

**Fig 12. Current address read**

9.3.4.2 Random address read: single read

[Table 52](#) describes the transfer format for a single-byte read. [Figure 13](#) illustrates the byte sequence.

Table 52. Transfer format description for a single-byte read

| SDA line | Description |
|--------------------|---|
| S | master starts with a START condition |
| Device select | master transmits the device address and write command bit R/W = 0 |
| ACK | slave generates an acknowledgment |
| Register address K | master transmits (start) address of register K from which to be read |
| ACK | slave generates an acknowledgment |
| S | master restarts with a START condition |
| Device select | master transmits the device address and read command bit R/W = 1 |
| ACK | slave generates an acknowledgment |
| Read data K | slave transmits and master reads data from register K |
| No ACK | master terminates the read operation by generating a no acknowledgement |
| P | master generates a STOP condition |

9.3.4.3 Random address read: multiple read

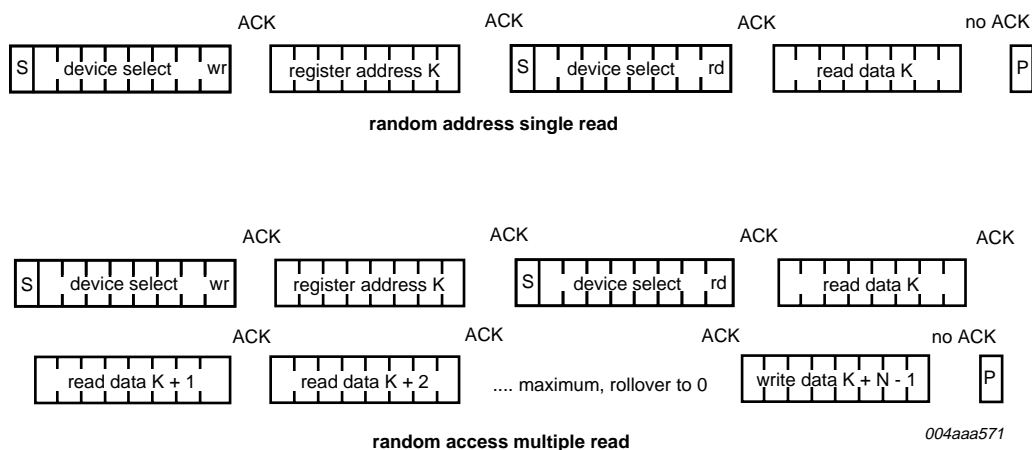
The transfer format description for a multiple-byte read is given in [Table 53](#). [Figure 13](#) illustrates the byte sequence.

Table 53. Transfer format description for a multiple-byte read

| SDA line | Description |
|--------------------|--|
| S | master starts with a START condition |
| Device select | master transmits the device address and write command bit R/W = 0 |
| ACK | slave generates an acknowledgment |
| Register address K | master transmits (start) address of register K from which to be read |

Table 53. Transfer format description for a multiple-byte read ...continued

| SDA line | Description |
|---------------------|--|
| ACK | slave generates an acknowledgment |
| S | master restarts with a START condition |
| Device select | master transmits the device address and read command bit R/W = 1 |
| ACK | slave generates an acknowledgment |
| Read data K | slave transmits and master reads data from register K. After a byte is read, the address is automatically incremented by 1. |
| ACK | master generates an acknowledgment |
| Read data K + 1 | slave transmits and master reads data from register K + 1 |
| ACK | master generates an acknowledgment |
| : | : |
| Read data K + N – 1 | slave transmits and master reads data register K + N – 1. This is the last register to read. After incrementing, the address rolls over to 0. Here, N represents the number of addresses available in the slave. |
| No ACK | master terminates the read operation by generating a no acknowledgement |
| P | master generates a STOP condition |

**Fig 13. Random address read**

10. Clock wake-up scheme

The following subsections explain the ISP1302 clock stop timing, events triggering the clock to wake up, and the timing of the clock wake-up.

10.1 Power-down event

The internal clock (LazyClock and/or I²C-bus clock) is stopped when bit PWR_DN is set. It takes $t_{d(\text{clkstp})}$ for the clock to stop from the time the power-down condition is detected. The clock always stops at its falling edge.

The internal clock must be woken up first before any register read or write operation.

10.2 Clock wake-up event

The clock wakes up when any of the following events occurs on the ISP1302 pins:

- Pin SCL goes LOW.
- Pin V_{BUS} goes above the session valid threshold, provided bit `SESS_VLD_IEH` of the Interrupt Enable High register is set.
- Status bit `ID_FLOAT` changes from logic 1 to logic 0, provided bit `ID_FLOAT_IEL` of the Interrupt Enable Low register is set.
- Status bit `ID_FLOAT` changes from logic 0 to logic 1, provided bit `ID_FLOAT_IEH` of the Interrupt Enable High register is set.
- DP goes HIGH provided the `DP_HI_IEH` bit in the Interrupt Enable High register is set.
- DM goes HIGH provided the `DM_HI_IEH` bit in the Interrupt Enable High register is set.

The event triggers the clock to start. The clock start-up time is $t_{startup(lclk)}$. A stable clock is guaranteed after six clock cycles. The clock will always start at its rising edge.

When an event is triggered and the clock is started, the clock will remain active for $t_{d(clkstp)}$. If bit `PWR_DN` is not cleared within this period, the clock will stop. If the clock wakes up because of any event other than SCL going LOW, an interrupt will be generated once the clock is active.

11. Limiting values

Table 54. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------------|---------------------------------------|--|-------------------|----------------------------|------|
| Voltage | | | | | |
| V _{CC} | supply voltage | | −0.5 | +5.5 ^[1] | V |
| V _{CC(I/O)} | input/output supply voltage | | −0.5 | +4.6 | V |
| V _I | input voltage | on digital pins ADR/PSW, SERVICE_N and RESET_N | −0.5 | +4.6 | V |
| | | on all other digital pins | −0.5 | V _{CC(I/O)} + 0.5 | V |
| | | on analog pins DP and DM | −0.5 | +4.6 ^[2] | V |
| | | on analog pins SPKR_L and SPKR_R/MIC | −0.5 | +4.6 | V |
| | | | | | |
| V _{I(VBUS)} | input voltage on pin V _{BUS} | | −0.5 | +7.0 ^[3] | V |
| V _{I(ID)} | input voltage on pin ID | | −0.5 | +5.5 | V |
| V _{ESD} | electrostatic discharge voltage | I _{LI} < 1 μA | | | |
| | | Human Body Model (JESD22-A114D) | ^[4] −2 | +2 | kV |
| | | Machine Model (JESD22-A115-A) | −200 | +200 | V |
| | | Charge Device Model (JESD22-C101-C) | −500 | +500 | V |
| | | | | | |
| Current | | | | | |
| I _{lu} | latch-up current | | - | 100 | mA |
| Temperature | | | | | |
| T _{stg} | storage temperature | | −60 | +125 | °C |
| T _j | junction temperature | | −40 | +125 | °C |

[1] When the charge pump is enabled, +5.5 V is only allowed for short period of time ≤ 1 second.

[2] The ISP1302 has been tested according to *Universal Serial Bus Specification Rev. 2.0, Section 7.1.1*. The DP and DM lines were shorted to V_{BUS}/GND for 24 hours with 50 % transmit/receive duty cycle. The ISP1302 operated normally after this test and is therefore compliant to the requirement.

[3] When an external series resistor is added to the V_{BUS} pin, it can withstand higher voltages for longer periods of time because the resistor limits the current flowing into the V_{BUS} pad. For example, with an external 1 kΩ resistor, V_{BUS} can tolerate 10 V for at least 5 seconds. If an external resistor is used, the internal charge pump must never be used, and other OTG functions must be verified in the customer application.

[4] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model).

12. Recommended operating conditions

Table 55. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|-----------------------------|------------|-----|-----|--------------------|------|
| Voltage | | | | | | |
| V _{CC} | supply voltage | | 3.0 | - | 4.5 | V |
| V _{CC(I/O)} | input/output supply voltage | | 1.4 | - | 3.6 ^[1] | V |

Table 55. Recommended operating conditions ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|----------------------------|---|-----|-----|----------------------|------|
| V _I | input voltage | digital pins ADR/PSW, SERVICE_N and RESET_N | 0 | - | 3.6 | V |
| | | on all other digital pins | 0 | - | V _{CC(I/O)} | V |
| | | on analog pins DP and DM | 0 | - | 3.6 | V |
| | | on analog pins SPKR_L and SPKR_R/MIC | 0 | - | 3.6 | V |
| V _{(pu)OD} | open-drain pull-up voltage | | 1.4 | - | 3.6 | V |
| Temperature | | | | | | |
| T _{amb} | ambient temperature | | -40 | - | +85 | °C |

[1] V_{CC(I/O)} should be less than or equal to V_{CC}.

13. Static characteristics

Table 56. Static characteristics: supply pins

V_{CC} = 3.0 V to 4.5 V; V_{CC(I/O)} = 1.4 V to 3.6 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Typical values are at V_{CC} = 3.3 V; V_{CC(I/O)} = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|--|--|--------|-----|------|-------|
| Voltage | | | | | | |
| V _{O(VREG)} | output voltage on pin VREG | bit UART_2V8_EN = 0; I _{load} ≤ 300 μA[1] | 3.0[2] | - | 3.6 | V |
| | | bit UART_2V8_EN = 1 and bit UART_EN = 1; I _{load} ≤ 10 mA | 2.35 | - | 2.85 | V |
| V _{POR(trip)} | power-on reset trip voltage | | 1.5 | - | 2.5 | V |
| Current | | | | | | |
| I _{CC} | supply current | transmitting and receiving at 12 Mbit/s; C _L = 50 pF on pins DP and DM | [3] | - | 5 | 8 mA |
| I _{CC(I/O)} | supply current on pin V _{CC(I/O)} | transmitting and receiving at 12 Mbit/s | [3] | - | 1 | 2 mA |
| I _{CC(I/O)(isol)} | isolate mode supply current on pin V _{CC(I/O)} | V _{CC} not connected | - | - | 10 | μA |
| I _{CC(idle)} | idle and SE0 supply current | idle: V _{DP} > 2.7 V, V _{DM} < 0.3 V; SE0: V _{DP} < 0.3 V, V _{DM} < 0.3 V | [4] | - | 0.5 | 1 mA |
| I _{CC(I/O)(stat)} | static supply current on pin V _{CC(I/O)} | idle, SE0 or suspend | - | - | 20 | μA |
| I _{CC(stat)} | static supply current | bit PWR_DN = 1, bit SUSPEND = 1 or V _{CC(I/O)} = 0 V | [4] | - | 12 | 25 μA |

[1] I_{load} includes the DP pull-up resistor current.

[2] In power-down mode, the minimum voltage is 2.7 V.

[3] Maximum value characterized only, not tested in production.

[4] Excluding any load current to the 1.5 kΩ and 15 kΩ pull-up and pull-down resistors (200 μA typical).

Table 57. Static characteristics: digital pins

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|---------------------------|--------------------------|--------------------------------|-----|-------------------------|------|
| Input level voltage | | | | | | |
| V _{IL} | LOW-level input voltage | | - | - | 0.3V _{CC(I/O)} | V |
| V _{IH} | HIGH-level input voltage | | 0.7V _{CC(I/O)} | - | - | V |
| Output level voltage | | | | | | |
| V _{OL} | LOW-level output voltage | I _{OL} = 2 mA | - | - | 0.4 | V |
| | | I _{OL} = 100 μA | - | - | 0.15 | V |
| V _{OH} | HIGH-level output voltage | I _{OH} = 2 mA | [1] V _{CC(I/O)} – 0.4 | - | - | V |
| | | I _{OH} = 100 μA | V _{CC(I/O)} – 0.15 | - | - | V |
| Leakage current | | | | | | |
| I _{LI} | input leakage current | | –1 | - | +1 | μA |
| Open-drain output current | | | | | | |
| I _{OZ} | off-state output current | | –5 | - | +5 | μA |
| Capacitance | | | | | | |
| C _{in} | input capacitance | pin to ground | - | - | 10 | pF |

[1] Not applicable for open-drain outputs.

Table 58. Static characteristics: analog I/O pins DP and DM

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|--|--|---------|-----|------|------------------|
| Input level voltage | | | | | | |
| V_{DI} | differential input sensitivity | $ V_{DP} - V_{DM} $ | 0.2 | - | - | V |
| V_{CM} | differential common mode voltage range | includes V_{DI} range | 0.8 | - | 2.35 | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| Output level voltage | | | | | | |
| V_{OL} | LOW-level output voltage | R_L of $1.5\text{ k}\Omega$ to $+3.6\text{ V}$ | - | - | 0.3 | V |
| V_{OH} | HIGH-level output voltage | R_L of $15\text{ k}\Omega$ to ground | 2.8 | - | 3.6 | V |
| Voltage | | | | | | |
| $V_{th(DP)L}$ | DP LOW threshold voltage | | 0.4 | - | 0.6 | V |
| V_{TERM} | termination voltage | | [1] 3.0 | - | 3.6 | V |
| Leakage current | | | | | | |
| I_{LZ} | off-state leakage current | | -1 | - | +1 | μA |
| Capacitance | | | | | | |
| C_{in} | input capacitance | pin to AGND | - | - | 10 | pF |
| Resistance | | | | | | |
| $R_{DN(DP)}$ | pull-down resistance on pin DP | | 14.25 | - | 24.8 | $\text{k}\Omega$ |
| $R_{DN(DM)}$ | pull-down resistance on pin DM | | 14.25 | - | 24.8 | $\text{k}\Omega$ |

Table 58. Static characteristics: analog I/O pins DP and DM ...continued

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-----------------------------------|--------------------|--------|-----|------|------------|
| $R_{UP(DP)}$ | pull-up resistance on pin DP | bus idle | 900 | - | 1575 | Ω |
| | | bus driven | 1425 | - | 3090 | Ω |
| $R_{weakUP(DP)}$ | weak pull-up resistance on pin DP | | 105 | 150 | 195 | k Ω |
| Z_{DRV} | driver output impedance | steady-state drive | [2] 34 | - | 44 | Ω |
| Z_{INP} | input impedance | | 1 | - | - | M Ω |

[1] For the upstream port pull-up resistance (R_{PU}).

[2] Includes external series resistances of $33\text{ }\Omega \pm 5\%$ each on DP and DM.

Table 59. Static characteristics: analog I/O pin ID

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|---------------------------------------|---|-----|-----|-----|------------|
| Resistance | | | | | | |
| $R_{UP(int)(ID)}$ | internal pull-up resistance on pin ID | | 70 | - | 130 | k Ω |
| $R_{DN(ID)}$ | pull-down resistance on pin ID | bit ID_PULLDOWN = 1; output pull-down resistance | - | - | 50 | Ω |
| | | bit ID_102K = 1; external 102 k Ω pull-down resistance | 101 | 102 | 103 | k Ω |
| | | bit ID_200K = 1; external 200 k Ω pull-down resistance | 198 | 200 | 202 | k Ω |
| | | bit ID_440K = 1; external 440 k Ω pull-down resistance | 436 | 440 | 444 | k Ω |
| | | bit ID_FLOAT = 1; external pull-down resistance on pin ID for mini-B plug | 105 | - | - | k Ω |
| | | bit ID_GND = 1; external pull-down resistance on pin ID for mini-A plug | - | - | 10 | Ω |

Table 60. Static characteristics: charge pump

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|----------------------------------|---|-----|-----|------|------|
| Current | | | | | | |
| I_{load} | load current | $C_{ext} = 220\text{ nF}$; $V_{BUS} > V_{A_VBUS_VLD}$ | 50 | - | - | mA |
| Voltage | | | | | | |
| $V_{O(VBUS)}$ | output voltage on pin V_{BUS} | $I_{load} = 50\text{ mA}$; $C_{ext} = 220\text{ nF}$ | 4.4 | 5 | 5.25 | V |
| $V_{L(VBUS)}$ | leakage voltage on pin V_{BUS} | charge pump disabled | - | - | 0.2 | V |
| $V_{A_VBUS_VLD}$ | A-device V_{BUS} valid voltage | | 4.4 | - | 4.7 | V |

Table 60. Static characteristics: charge pump ...continued

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---|---|-----------------------|-----|------|------|
| V _{B_SESS_END} | B-device session end voltage | | 0.2 | - | 0.8 | V |
| V _{A_SESS_VLD} | A-device session valid voltage | bit ID_GND = 1 | 0.8 | - | 2.0 | V |
| V _{B_SESS_VLD} | B-device session valid voltage | bit ID_GND = 0 | 0.8 | - | 4.0 | V |
| V _{hys(A_SESS_VLD)} | A-device session valid hysteresis voltage | | - | 80 | - | mV |
| V _{hys(B_SESS_VLD)} | B-device session valid hysteresis voltage | | - | 80 | - | mV |
| η _{cp} | charge pump efficiency | I _{load} = 50 mA; V _{CC} = 3 V | [1] - | 75 | - | % |
| Resistance | | | | | | |
| R _{UP(VBUS)} | pull-up resistance on pin V _{BUS} | connect to VREG when bit VBUS_CHRG = 1 | 460 | - | 1000 | Ω |
| R _{DN(VBUS)} | pull-down resistance on pin V _{BUS} | connect to ground when bit VBUS_DISCHRG = 1 | 660 | - | 1200 | Ω |
| R _{I(idle)(VBUS)} | idle input resistance on pin V _{BUS} | bit ID_GND = 1 and bit VBUS_DRV = 0 | 52.5 | 70 | 100 | kΩ |
| | | bit ID_GND = 0, bit VBUS_DRV = 1, or V _{CC} and V _{CC(I/O)} are not powered | 130 | 200 | 270 | kΩ |
| Capacitance | | | | | | |
| C _{ext} | external capacitance | I _{load} = 8 mA | 20 | - | - | nF |
| | | I _{load} = 20 mA | 61 | - | - | nF |
| | | I _{load} = 25 mA | 90 | - | - | nF |
| | | I _{load} = 50 mA | 198 | - | - | nF |

[1] Efficiency when loaded.

Table 61. Static characteristics: analog I/O pins SPKR_R/MIC and SPKR_L

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|----------------------------------|-------------|-----|-----|-----|------------|
| Capacitance | | | | | | |
| C_{in} | input capacitance | pin to AGND | - | - | 10 | pF |
| Resistance | | | | | | |
| $Z_{asw(on)}$ | audio switch ON state impedance | | 50 | - | 150 | Ω |
| $Z_{asw(off)}$ | audio switch OFF state impedance | | 2 | - | - | M Ω |
| R_{B1} | bias resistance 1 | | 7 | 10 | 13 | k Ω |
| R_{B2} | bias resistance 2 | | 14 | 20 | 26 | k Ω |
| M_R | resistance matching | | - | - | 1 | % |

14. Dynamic characteristics

Table 62. Dynamic characteristics: reset and clock

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.
Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|--|-----------------|--------|-----|------|---------------|
| Reset | | | | | | |
| $t_{W(RES\overline{E}T_N)}$ | external RESET_N pulse width | | 10 | - | - | μs |
| Internal clock | | | | | | |
| f_{clk} | clock frequency | bit PWR_DN = 0 | [1] 70 | 110 | 150 | kHz |
| f_{clk_I2C} | I ² C-bus clock frequency | | 3.5 | 5.0 | 7.0 | MHz |
| $f_{clk(dda)}$ | data-during-audio clock frequency | TX_PULSE_EN = 1 | 35 | - | 80 | MHz |
| $t_{d(PD-CLKstop)}$ | delay time from power-down to clock stop | | 5.6 | 8 | 10.4 | ms |
| $t_{startup(lclk)}$ | LazyClock start-up time | | 7 | 10 | 13 | μs |
| $t_{d(clkstp)}$ | clock stop delay time | | 5.6 | 8 | 10.4 | ms |

[1] LazyClock for interrupts, registers, and power-down and wake-up timer.

Table 63. Dynamic characteristics: V_{BUS} comparator timing

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.
Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|------------------------------------|------------|-----|-----|-----|---------------|
| $t_{d(VA_VBUS_VLD)}$ | V _{A_VBUS_VLD} delay time | | 20 | - | 300 | μs |

Table 64. Dynamic characteristics: bus turnaround timing (USB bidirectional mode)

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $C_L = 50\text{ pF}$; $R_{PU} = 1.5\text{ k}\Omega$ on DP to V_{TERM} ; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------------|--|-----|-----|-----|------|
| t_{TOI} | bus turnaround time (O/I) | OE_N/INT_N to DAT/VP and SE0/VM; see Figure 18 | 0 | - | 5 | ns |
| t_{TIO} | bus turnaround time (I/O) | OE_N/INT_N to DAT/VP and SE0/VM; see Figure 18 | 0 | - | 5 | ns |

Table 65. Dynamic characteristics: analog I/O pins DP and DM

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $C_L = 50\text{ pF}$; $R_{PU} = 1.5\text{ k}\Omega$ on DP to V_{TERM} ; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|----------------------------|--|-----|-----|-----|------|
| Driver characteristics (low-speed) | | | | | | |
| t_{LR} | transition time: rise time | $C_L = 200\text{ pF to }600\text{ pF}$; 1.5 k Ω pull-up on pin DM enabled; 10 % to 90 % of $ V_{OH} - V_{OL} $; see Figure 14 | 75 | - | 300 | ns |
| t_{LF} | transition time: fall time | $C_L = 200\text{ pF to }600\text{ pF}$; 1.5 k Ω pull-up on pin DM enabled; 90 % to 10 % of $ V_{OH} - V_{OL} $; see Figure 14 | 75 | - | 300 | ns |

Table 65. Dynamic characteristics: analog I/O pins DP and DM ...continued

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $C_L = 50\text{ pF}$; $R_{PU} = 1.5\text{ k}\Omega$ on DP to V_{TERM} ; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|--|--------|-----|-------|------|
| FRFM | differential rise time/fall time matching | excluding the first transition from idle state | [1] 80 | - | 125 | % |
| V_{CRS} | output signal crossover voltage | excluding the first transition from idle state; see Figure 15 | 1.3 | - | 2.0 | V |
| Driver characteristics (full-speed) | | | | | | |
| t_{FR} | rise time | $C_L = 50\text{ pF}$; 10 % to 90 % of $ V_{OH} - V_{OL} $; see Figure 14 | 4 | - | 20 | ns |
| t_{FF} | fall time | $C_L = 50\text{ pF}$; 90 % to 10 % of $ V_{OH} - V_{OL} $; see Figure 14 | 4 | - | 20 | ns |
| FRFM | differential rise time/fall time matching | excluding the first transition from idle state | [1] 90 | - | 111.1 | % |
| V_{CRS} | output signal crossover voltage | excluding the first transition from idle state; see Figure 15 | 1.3 | - | 2.0 | V |
| Driver timing | | | | | | |
| $t_{PLH(drv)}$ | driver propagation delay (LOW to HIGH) | DAT/VP, SE0/VM to DP, DM; see Figure 15 and Figure 19 | - | - | 18 | ns |
| $t_{PHL(drv)}$ | driver propagation delay (HIGH to LOW) | DAT/VP, SE0/VM to DP, DM; see Figure 15 and Figure 19 | - | - | 18 | ns |
| t_{PHZ} | HIGH to OFF-state propagation delay | OE_N/INT_N to DP, DM; see Figure 16 and Figure 20 | - | - | 15 | ns |
| t_{PLZ} | LOW to OFF-state propagation delay | OE_N/INT_N to DP, DM; see Figure 16 and Figure 20 | - | - | 15 | ns |
| t_{PZH} | OFF-state to HIGH propagation delay | OE_N/INT_N to DP, DM; see Figure 16 and Figure 20 | - | - | 15 | ns |
| t_{PZL} | OFF-state to LOW propagation delay | OE_N/INT_N to DP, DM; see Figure 16 and Figure 20 | - | - | 15 | ns |
| Receiver timing | | | | | | |
| Differential receiver | | | | | | |
| $t_{PLH(rcv)}$ | receiver propagation delay (LOW to HIGH) | DP, DM to RCV; see Figure 17 and Figure 21 | - | - | 15 | ns |
| $t_{PHL(rcv)}$ | receiver propagation delay (HIGH to LOW) | DP, DM to RCV; see Figure 17 and Figure 21 | - | - | 15 | ns |
| Single-ended receiver | | | | | | |
| $t_{PLH(se)}$ | single-ended propagation delay (LOW to HIGH) | DP, DM to DAT/VP, SE0/VM; see Figure 17 and Figure 21 | - | - | 18 | ns |
| $t_{PHL(se)}$ | single-ended propagation delay (HIGH to LOW) | DP, DM to DAT/VP, SE0/VM; see Figure 17 and Figure 21 | - | - | 18 | ns |

[1] t_{FR}/t_{FF} .

Table 66. Dynamic characteristics: analog I/O pin ID

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $C_L = 50\text{ pF}$; $R_{PU} = 1.5\text{ k}\Omega$ on DP to V_{TERM} ; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|--------------------------|------------|-----|-----|-----|------|
| $t_{PH_ID_INT}$ | ID interrupt pulse width | | 4 | - | 8 | ms |
| $t_{PH_ID_WT}$ | ID interrupt wait time | | 4 | - | 8 | ms |

Table 67. Dynamic characteristics: audio switches

$V_{CC} = 3.0\text{ V to }4.5\text{ V}$; $V_{CC(I/O)} = 1.4\text{ V to }3.6\text{ V}$; $C_L = 50\text{ pF}$; $R_{PU} = 1.5\text{ k}\Omega$ on DP to V_{TERM} ; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Typical values are at $V_{CC} = 3.3\text{ V}$; $V_{CC(I/O)} = 3.3\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|-------------------------------------|--|-----|-----|-----|------|
| PSRR | power supply rejection ratio | noise on $V_{CC} = 0.5\text{ V (p-p)}$ at $f = 217\text{ Hz}$ over audio range of $20\text{ Hz to }20\text{ kHz}$; see Section 14.1 | - | - | -80 | dB |
| $\alpha_{ct(audio)}$ | crosstalk audio | audio voltage = 1 V , $f = 1\text{ kHz}$; see Section 14.2 | - | - | -66 | dB |
| THD | total harmonic distortion | audio voltage = 2.3 V , $f = 1\text{ kHz}$; see Section 14.1 | - | - | 1 | % |
| | | audio voltage = 2.0 V , $f = 1\text{ kHz}$; see Section 14.1 | - | - | 0.3 | % |
| $\alpha_{iso(d-a)}$ | data to audio isolation | USB 12 Mbit/s active on DP and DM, $< 20\text{ kHz}$ signal components observed on the SPKR_L and SPKR_R/MIC pins; see Section 14.3 | - | - | -70 | dB |
| $V_{io(audio)}$ | audio input or output voltage range | | 0.1 | - | 2.3 | V |

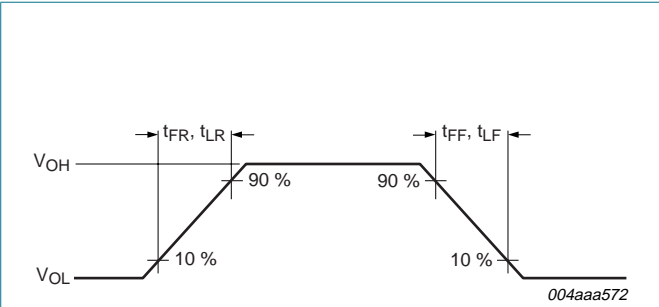


Fig 14. Rise time and fall time

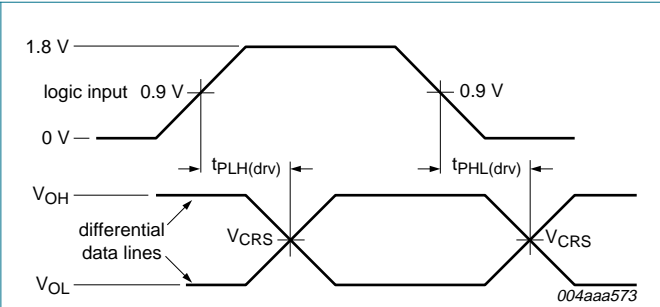


Fig 15. Timing of DAT/VP and SE0/VM to DP and DM

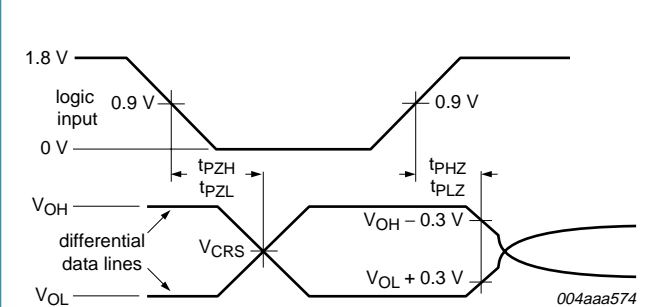


Fig 16. Timing of OE_N/INT_N to DP and DM

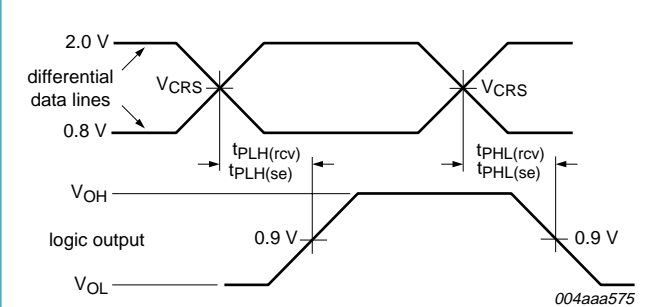


Fig 17. Timing of DP and DM to RCV, DAT/VP and SE0/VM

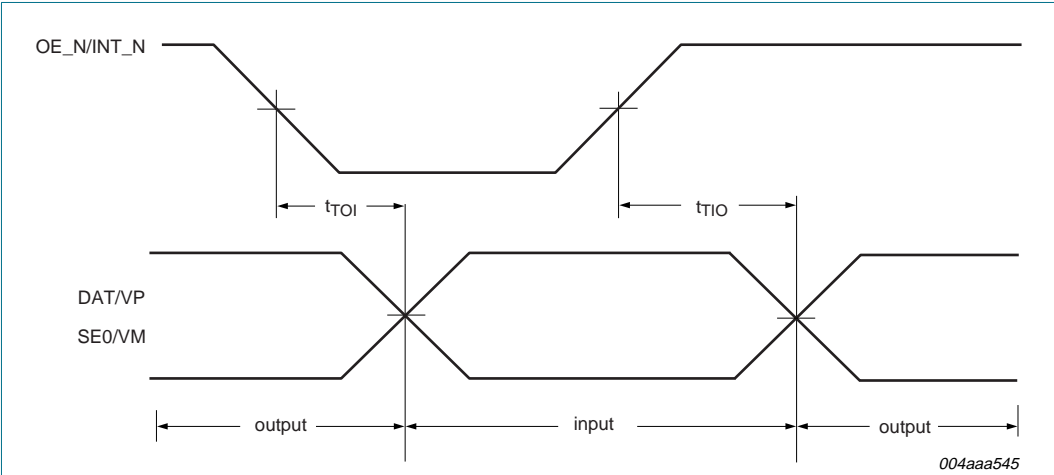
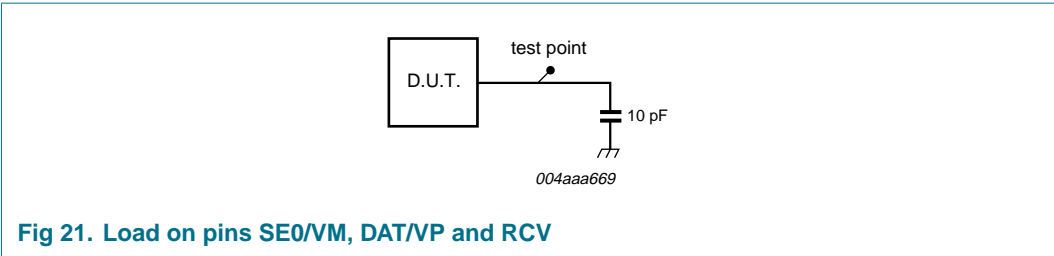
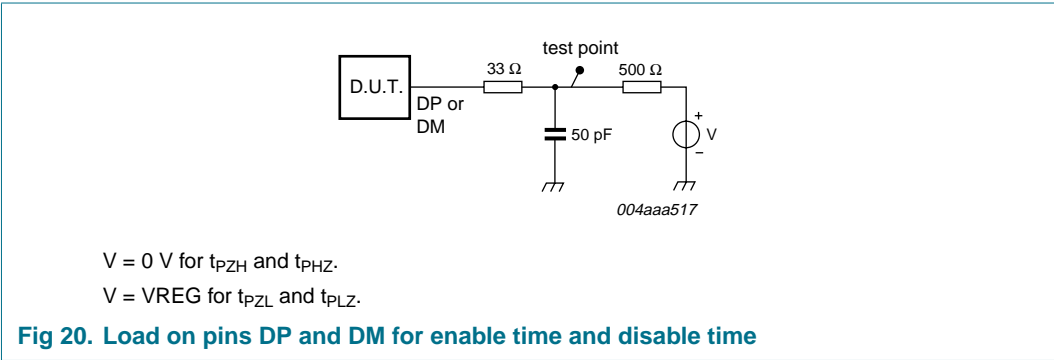
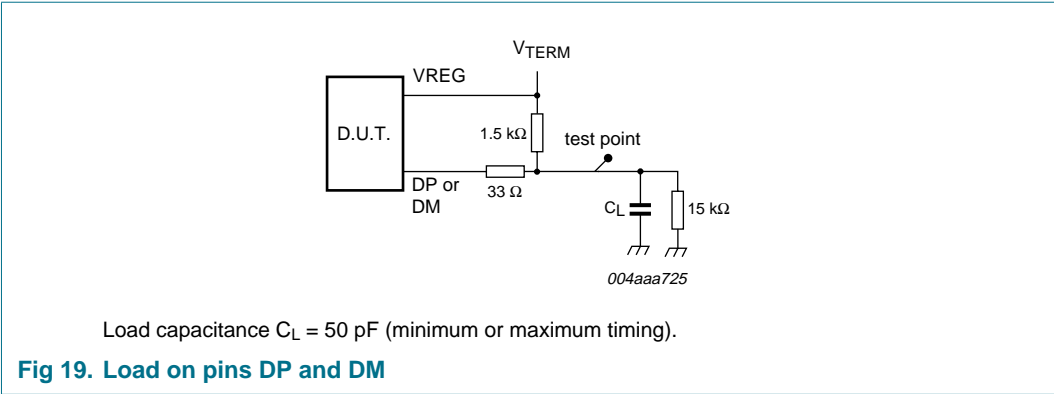


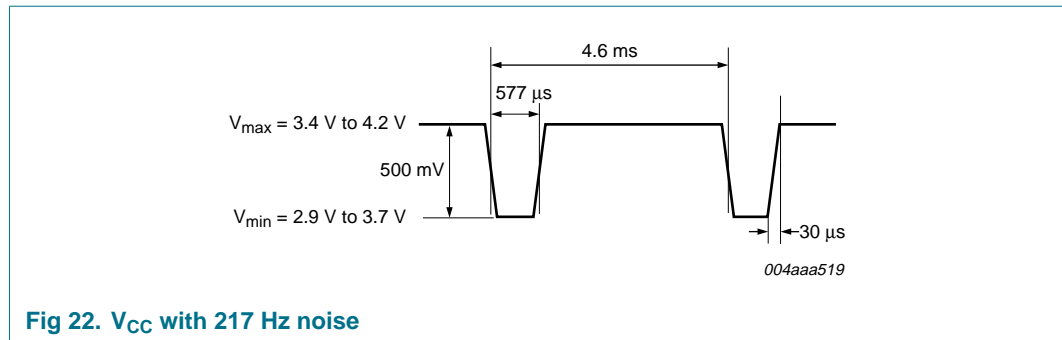
Fig 18. SIE interface bus turnaround timing



14.1 Test configurations

Table 68. Test configurations

| Parameter | Pins or switches | Configuration 1 | Configuration 2 |
|------------------------|------------------|-----------------|-----------------|
| Termination impedances | DP | 60 kΩ | 200 Ω, 1.4 V DC |
| | DM | 60 kΩ | 60 kΩ |
| | SPKR_R | 200 Ω | 200 Ω, 1.4 V DC |
| | SPKR_L | 200 Ω | 200 Ω, 1.4 V DC |
| | MIC | 10 kΩ | 10 kΩ |
| Switch positions | S1 | on | off |
| | S2 | off | on |
| | S3 | on | on |
| Measured ports | - | DP | MIC |
| | - | DM | DM |



14.2 Audio crosstalk test conditions

V_{CC} sweeps from 2.9 V to 4.2 V (DC waveform).

14.2.1 Test 1

- SW2 = on and SW3 = on.
- DP is terminated using a 200 Ω resistor, and DM is terminated using a 60 k Ω resistor.
- MIC is terminated using a 10 k Ω resistor, and SPKR_L is terminated using a 200 Ω resistor, 1.4 V DC.
- Drive $f = 1$ kHz, $V = 1$ V (p-p) to DP; signal on DM must be 66 dB below.

14.2.2 Test 2

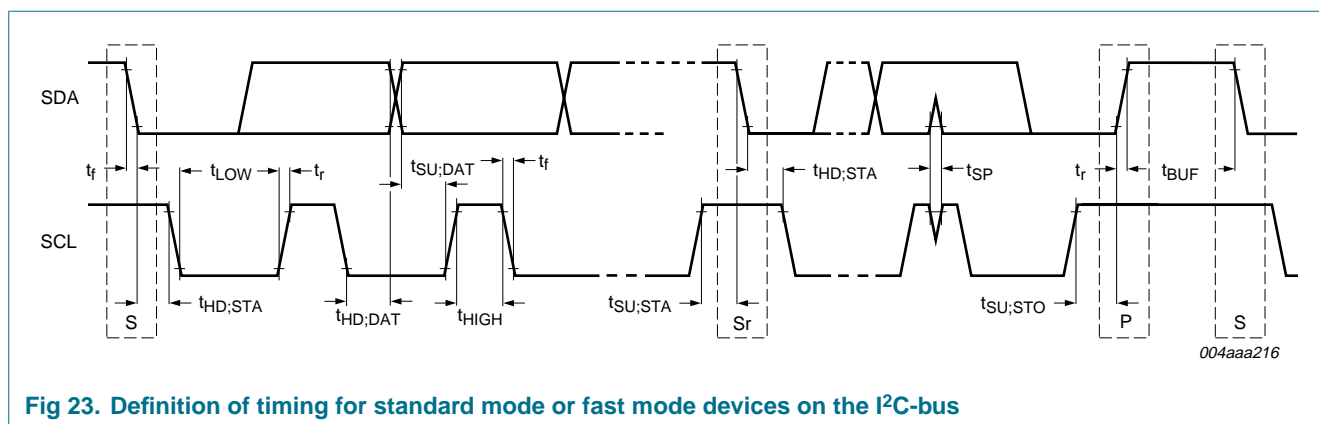
- SW1 = on and SW3 = on.
- DP and DM are terminated using a 60 k Ω resistor.
- SPKR_L and SPKR_R are terminated using a 200 Ω resistor, 1.4 V DC.
- Drive $f = 1$ kHz, $V = 1$ V (p-p) to SPKR_R; signal on DM must be 66 dB below.

14.2.3 Test 3

- SW1 = on and SW3 = on.
- DP and DM terminated using a 60 k Ω resistor.
- SPKR_L and SPKR_R terminated using a 200 Ω resistor, 1.4 V DC.
- Drive $f = 1$ kHz, $V = 1$ V (p-p) to SPKR_L; signal on DP must be 66 dB below.

14.3 Data to audio isolation test conditions

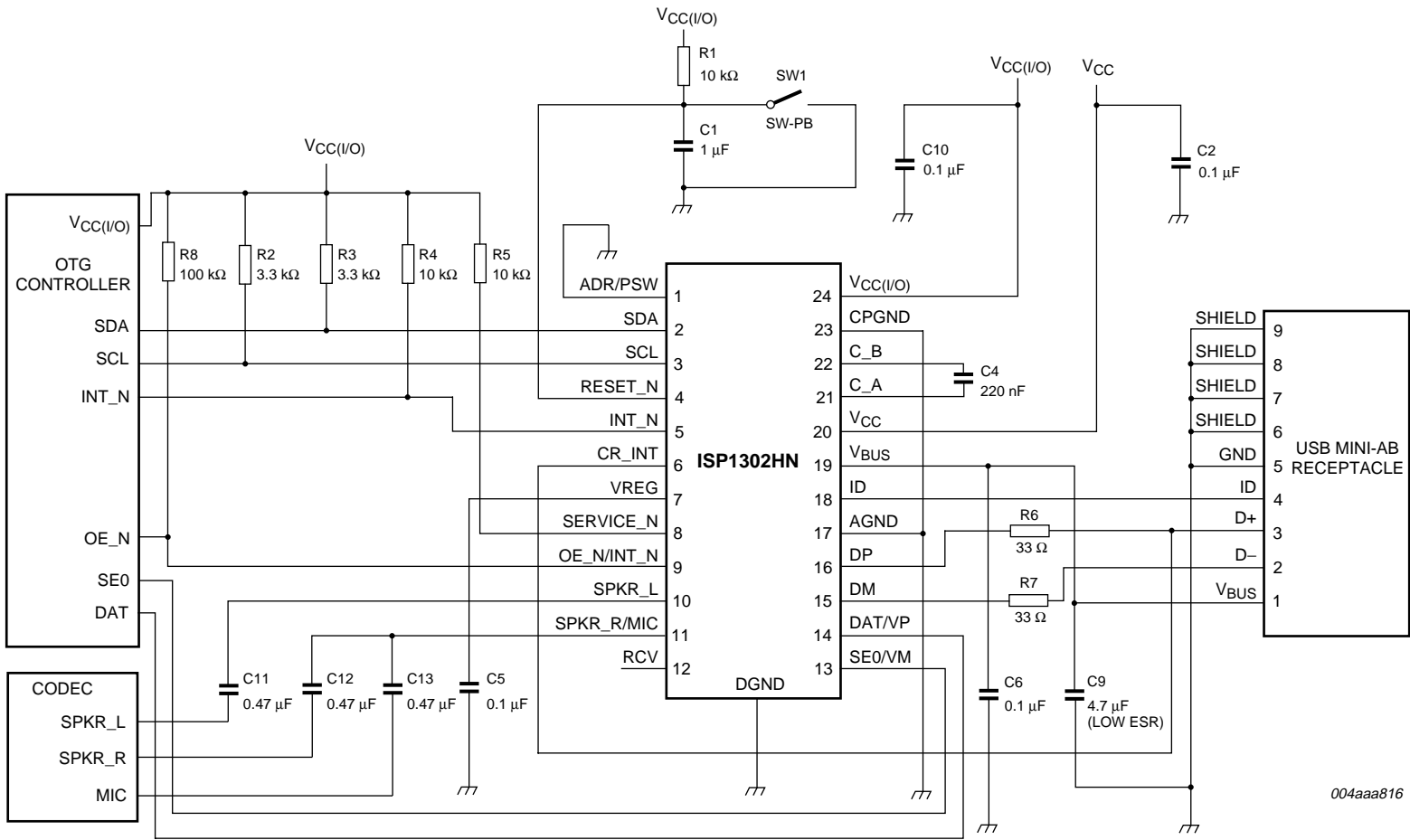
- V_{CC} is swept from 2.9 V to 4.2 V (DC waveform).
- 12 Mbit/s USB data is to be active on the DP and DM pins.
- All audio switches must be left open.
- MIC must be terminated using a 10 k Ω resistor.
- SPKR_L and SPKR_R are each to be terminated using a 200 Ω resistor.
- Taking an FFT on the SPKR_R/MIC and SPKR_L pins, USB data components below 20 kHz will be < -70 dB below the USB data level (3.6 V).

14.4 I²C-bus characteristicsFig 23. Definition of timing for standard mode or fast mode devices on the I²C-busTable 69. Characteristics of I/O stages of I²C-bus lines (SDA, SCL)

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|---------------------|---|------------|----------------|----------------|----------------------------|-----|------|
| | | | Min | Max | Min | Max | |
| f _{SCL} | SCL clock frequency | | 0 | 100 | 0 | 400 | kHz |
| t _{HD;STA} | hold time (repeated) START condition | | 4.0 | - | 0.6 | - | μs |
| t _{LOW} | LOW period of the SCL clock | | 4.7 | - | 1.3 | - | μs |
| t _{HIGH} | HIGH period of the SCL clock | | 4.0 | - | 0.6 | - | μs |
| t _{SU;STA} | set-up time for a repeated START condition | | 4.7 | - | 0.6 | - | μs |
| t _{SU;DAT} | data set-up time | | 250 | - | 100 | - | ns |
| t _{HD;DAT} | data hold time | | 0 | - | 0 | 0.9 | μs |
| t _r | rise time of both SDA and SCL signals | | - | 1000 | 20 + 0.1C _b [1] | 300 | ns |
| t _f | fall time of both SDA and SCL signals | | - | 300 | 20 + 0.1C _b [1] | 300 | ns |
| t _{SU;STO} | set-up time for STOP condition | | 4.0 | - | 0.6 | - | μs |
| t _{BUF} | bus free time between a STOP and START condition | | 4.7 | - | 1.3 | - | μs |
| t _{SP} | pulse width of spikes that must be suppressed by the input filter | | not applicable | not applicable | 0 | 50 | ns |

[1] C_b is the capacitance load for each bus line in pF. If mixed with high-speed mode devices, faster fall times are allowed.

15. Application information



The figure shows the HVQFN pinout. For the WLCSP ballout, see [Table 2](#).

Fig 24. Application diagram

16. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads;
 24 terminals; body 4 x 4 x 0.85 mm

SOT616-3

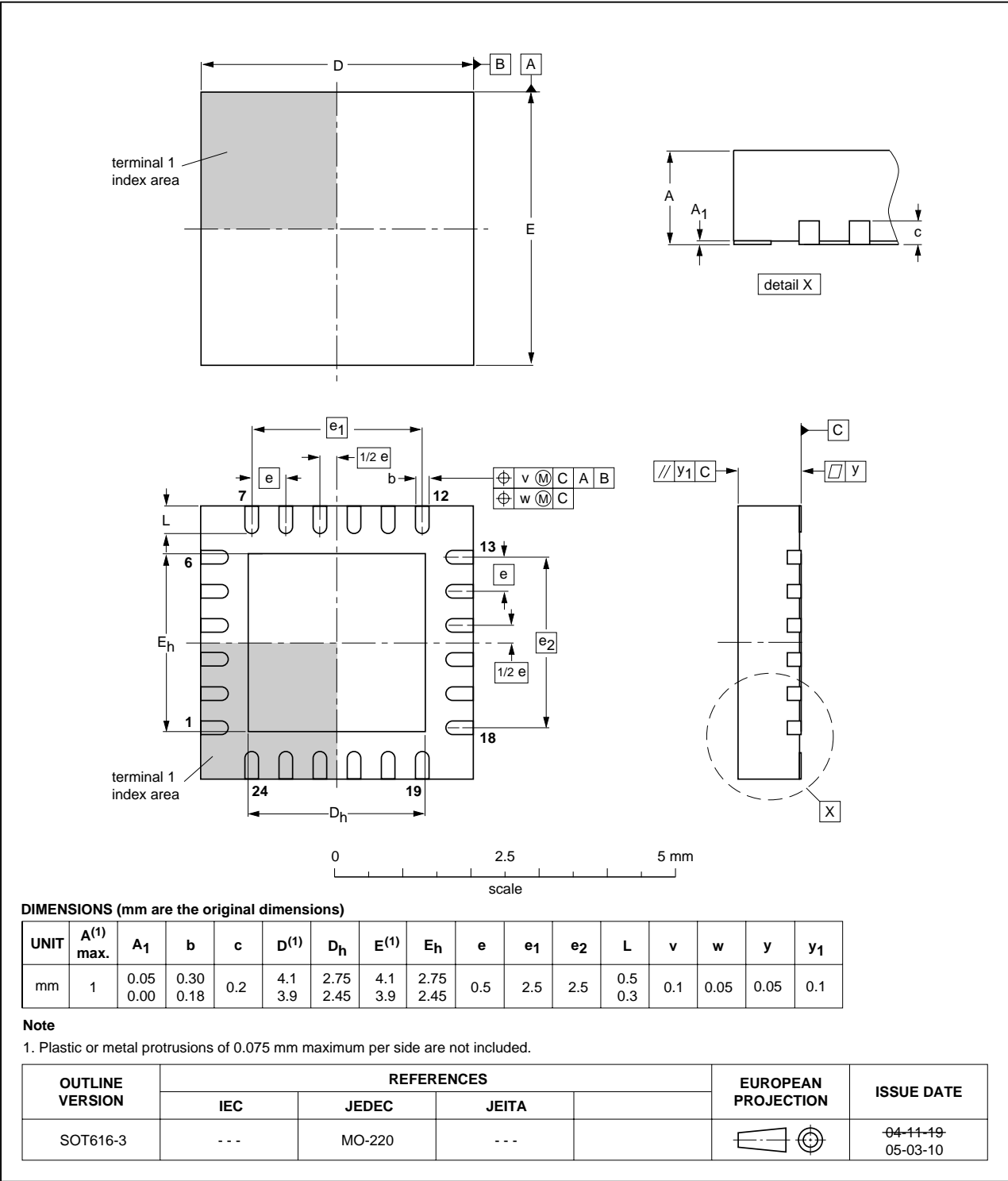


Fig 25. Package outline SOT616-3 (HVQFN24)

WLCSP25: wafer level chip-size package; 25 bumps; 2.5 x 2.5 x 0.6 mm

ISP1302UK

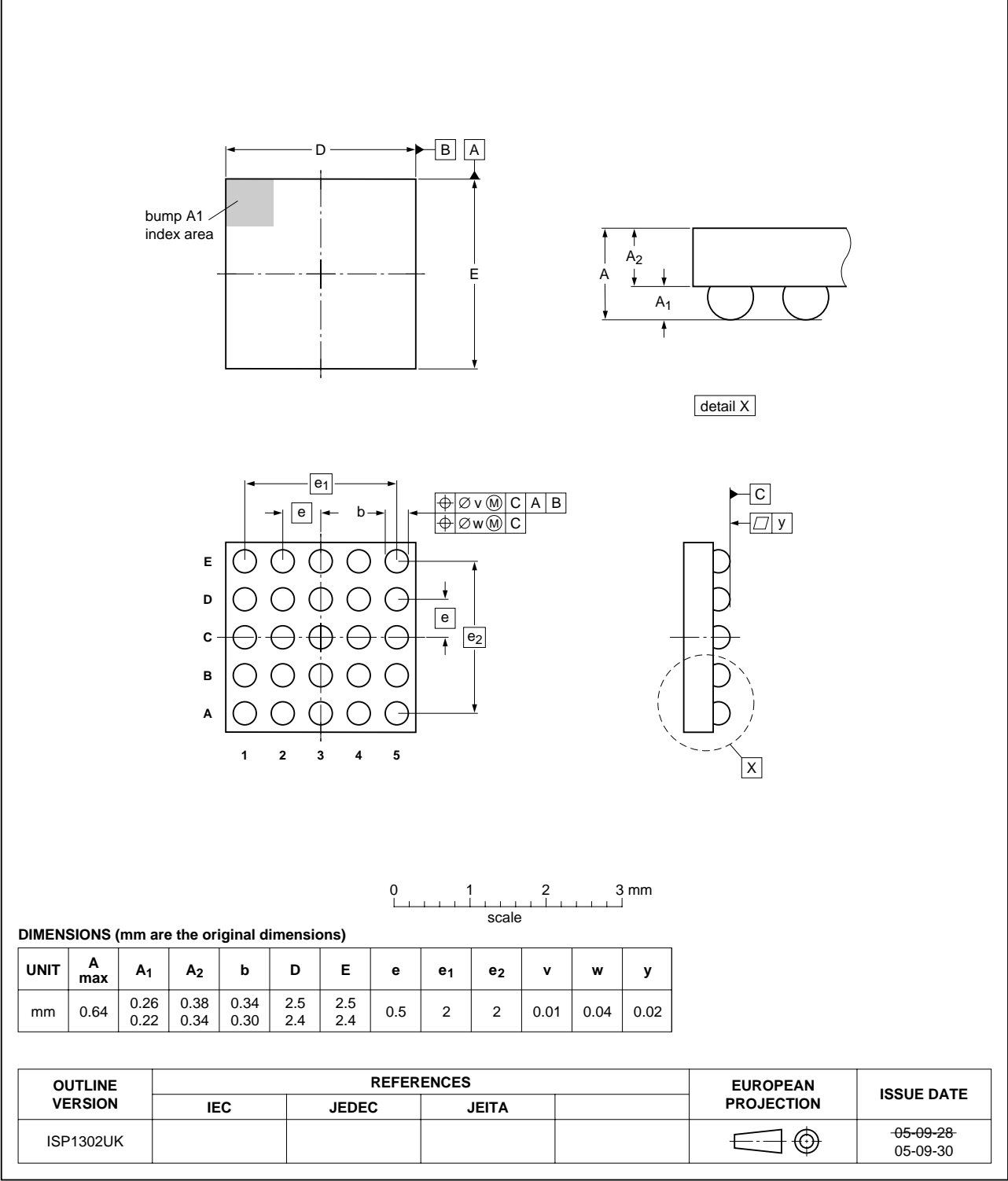


Fig 26. Package outline ISP1302UK (WLCSP25)

17. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 27](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 70](#) and [71](#)

Table 70. SnPb eutectic process (from J-STD-020C)

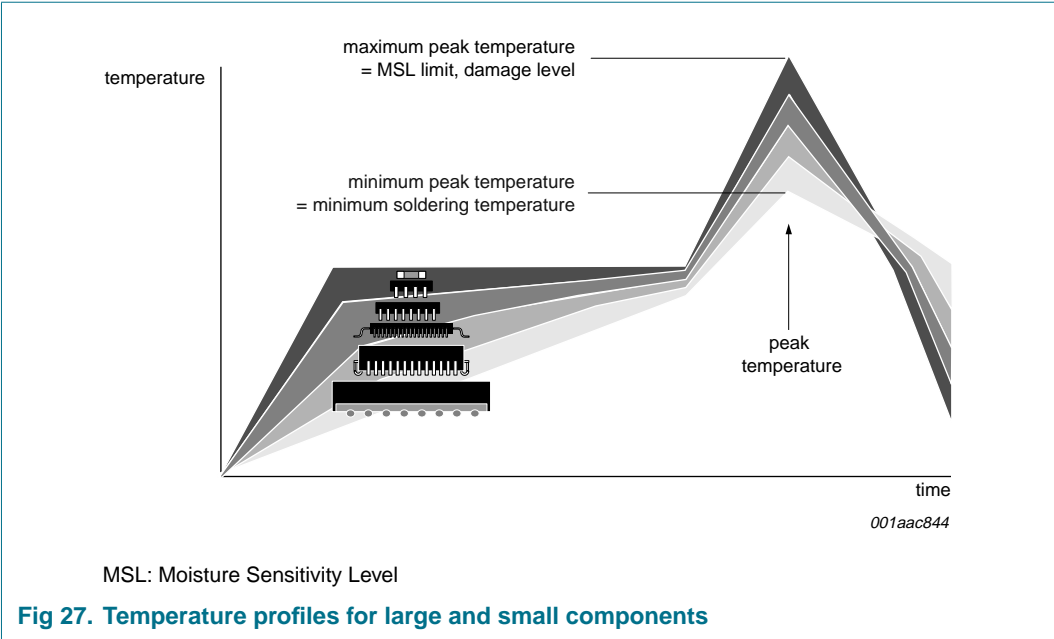
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 71. Lead-free process (from J-STD-020C)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 27](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

18. Additional soldering information

A more in-depth account of soldering WLCSP (Wafer-Level Chip-Size Package) can be found in Application Note *AN10439* “Wafer Level Chip Scale Package”.

19. Abbreviations

Table 72. Abbreviations

| Acronym | Description |
|----------------------|---------------------------|
| ATX | Analog USB Transceiver |
| FFT | Fast Fourier Transform |
| HNP | Host Negotiation Protocol |
| I ² C-bus | Inter IC-bus |
| LSB | Least Significant Bit |
| MIC | Microphone |
| NRZ | Non-Return-to-Zero |
| OTG | On-The-Go |
| POR | Power-On Reset |
| PORP | Power-On Reset Pulse |
| RxD | Receive Data |
| SE0 | Single-Ended Zero |
| SIE | Serial Interface Engine |
| SoC | System-on-a-Chip |
| SOF | Start-Of-Frame |

Table 72. Abbreviations ...continued

| Acronym | Description |
|---------|---|
| SRP | Session Request Protocol |
| TxD | Transmit Data |
| UART | Universal Asynchronous Receiver-Transmitter |
| USB | Universal Serial Bus |
| WLCSP | Wafer-Level Chip-Scale Package |

20. References

- [1] Universal Serial Bus Specification Rev. 2.0
- [2] On-The-Go Supplement to the USB Specification Rev. 1.2
- [3] On-The-Go Transceiver Specification (CEA-2011)
- [4] USB Carkit Specification (CEA-936-A), November 2005
- [5] ECN_27%_Resistor (Pull-up/pull-down Resistors ECN)
- [6] The I²C-bus specification; ver. 2.1
- [7] Human Body Model (JESD22-A114D)
- [8] Machine Model (JESD22-A115-A)
- [9] Charge Device Model (JESD22-C101-C)

21. Revision history

Table 73. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------|--------------|--------------------|---------------|------------|
| ISP1302_1 | 20070524 | Product data sheet | - | - |

22. Legal information

22.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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