

# DATA SHEET



**PBSS5240T**

40 V, 2 A

PNP low  $V_{CEsat}$  (BISS) transistor

Product data sheet  
Supersedes data of 2001 Oct 31

2004 Jan 15

**40 V, 2 A**  
**PNP low  $V_{CEsat}$  (BISS) transistor**

**PBSS5240T**

**FEATURES**

- Low collector-emitter saturation voltage
- High current capability
- Improved device reliability due to reduced heat generation
- Replacement for SOT89/SOT223 standard packaged transistor.

**APPLICATIONS**

- Supply line switching circuits
- Battery management applications
- DC/DC converter applications
- Strobe flash units
- Heavy duty battery powered equipment (motor and lamp drivers).

**DESCRIPTION**

PNP low  $V_{CEsat}$  transistor in a SOT23 plastic package.  
 NPN complement: PBSS4240T.

**MARKING**

TYPE NUMBER	MARKING CODE <sup>(1)</sup>
PBSS5240T	ZF*

**Note**

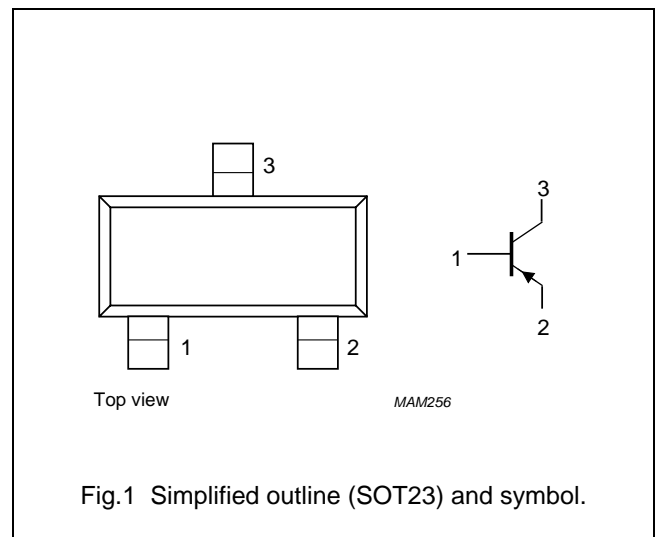
- \* = p: Made in Hong Kong.  
 \* = t: Made in Malaysia.  
 \* = W: Made in China.

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
$V_{CEO}$	collector-emitter voltage	-40	V
$I_C$	collector current (DC)	-2	A
$I_{CM}$	peak collector current	-3	A
$R_{CEsat}$	equivalent on-resistance	<220	m $\Omega$

**PINNING**

PIN	DESCRIPTION
1	base
2	emitter
3	collector



**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS5240T	-	plastic surface mounted package; 3 leads	SOT23

40 V, 2 A  
PNP low  $V_{CEsat}$  (BISS) transistor

PBSS5240T

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–40	V
$V_{CEO}$	collector-emitter voltage	open base	–	–40	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)		–	–2	A
$I_{CM}$	peak collector current		–	–3	A
$I_{BM}$	peak base current		–	–300	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	300	mW
		$T_{amb} \leq 25\text{ °C}$ ; note 2	–	480	mW
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

**Notes**

1. Device mounted on a printed-circuit board, single sided copper, tin plated, standard footprint.
2. Device mounted on a printed-circuit board, single sided copper, tin plated, mounting pad for collector 1 cm<sup>2</sup>.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	417	K/W
		in free air; note 2	260	K/W

**Notes**

1. Device mounted on a printed-circuit board, single sided copper, tin plated, standard footprint.
2. Device mounted on a printed-circuit board, single sided copper, tin plated, mounting pad for collector 1 cm<sup>2</sup>.

40 V, 2 A  
PNP low  $V_{CEsat}$  (BISS) transistor

PBSS5240T

**CHARACTERISTICS** $T_{amb} = 25\text{ °C}$  unless otherwise specified.

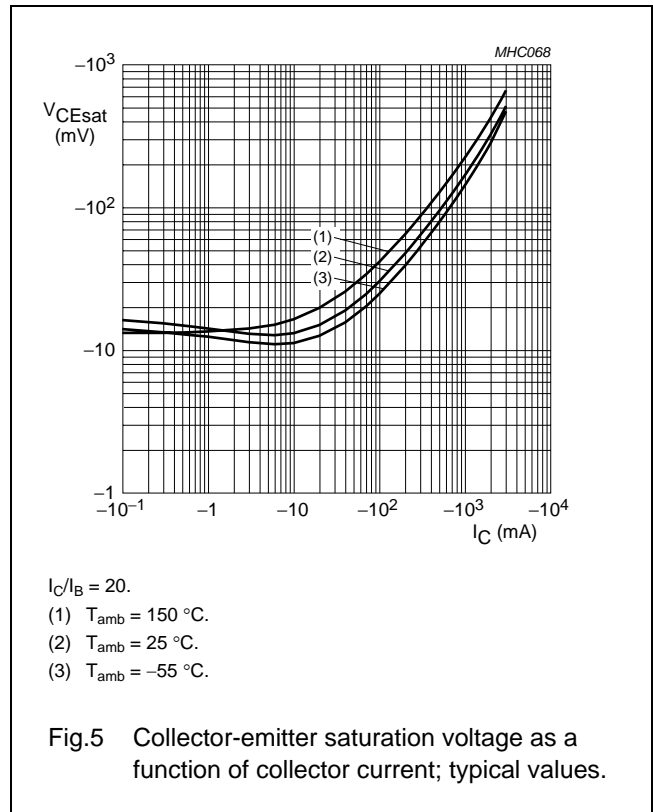
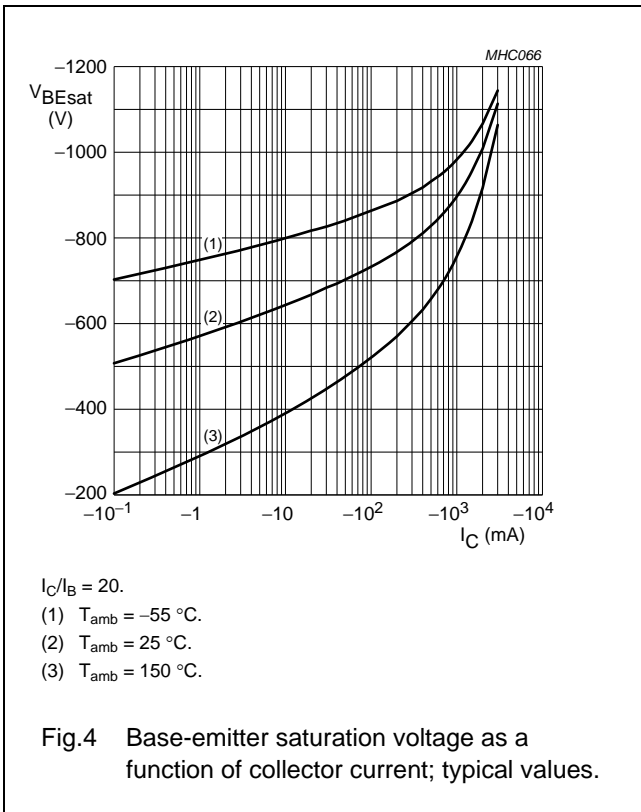
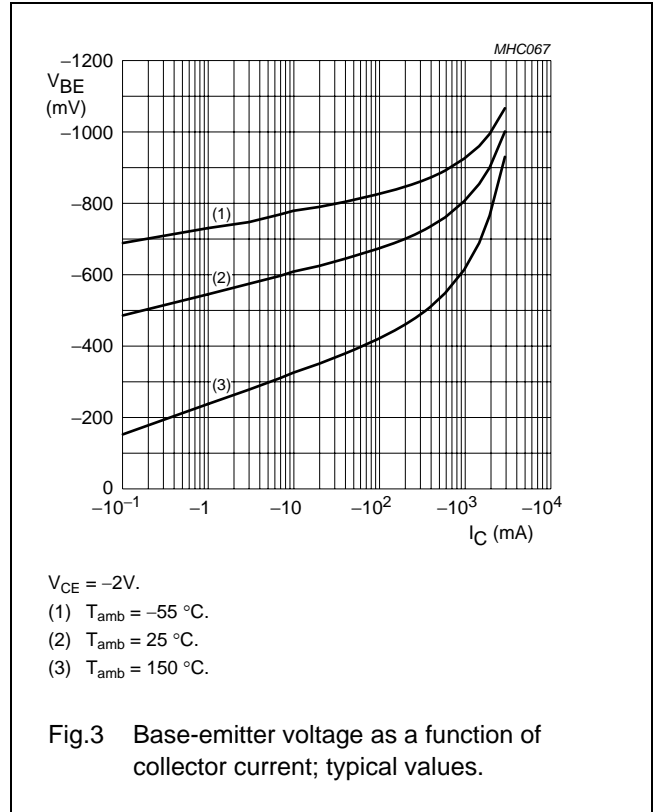
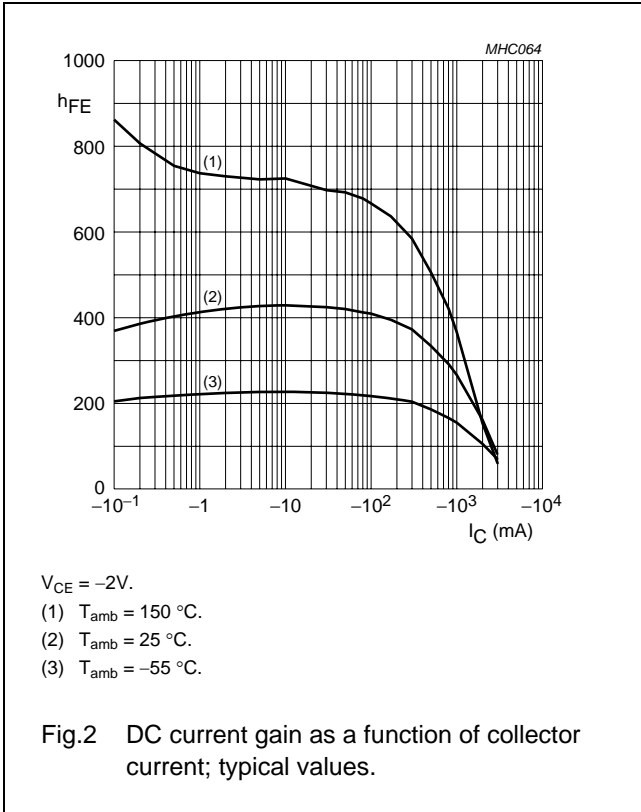
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0$	–	–	–100	nA
		$V_{CB} = -30\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	–	–50	$\mu\text{A}$
$I_{BEO}$	emitter-base cut-off current	$V_{EB} = -4\text{ V}; I_C = 0$	–	–	–100	nA
$h_{FE}$	DC current gain	$V_{CE} = -2\text{ V}$ $I_C = -100\text{ mA}$ $I_C = -500\text{ mA}$ $I_C = -1\text{ A}$ $I_C = -2\text{ A}$	300 260 210 100	450 350 290 180	– – – –	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -1\text{ mA}$	–	–55	–100	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–70	–110	mV
		$I_C = -750\text{ mA}; I_B = -15\text{ mA}$	–	–140	–225	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	–	–140	–225	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	–	–240	–350	mV
$R_{CEsat}$	equivalent on-resistance	$I_C = -500\text{ mA}; I_B = -50\text{ mA};$ note 1	–	160	<220	$\text{m}\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -2\text{ A}; I_B = -200\text{ mA}$	–	–	–1.1	V
$V_{BE(on)}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}$	–	–	–0.75	V
$f_T$	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -10\text{ V};$ $f = 100\text{ MHz}$	100	200	–	MHz
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0;$ $f = 1\text{ MHz}$	–	23	28	pF

**Note**

1. Device mounted on a printed-circuit board, single sided copper, tin plated, standard footprint.

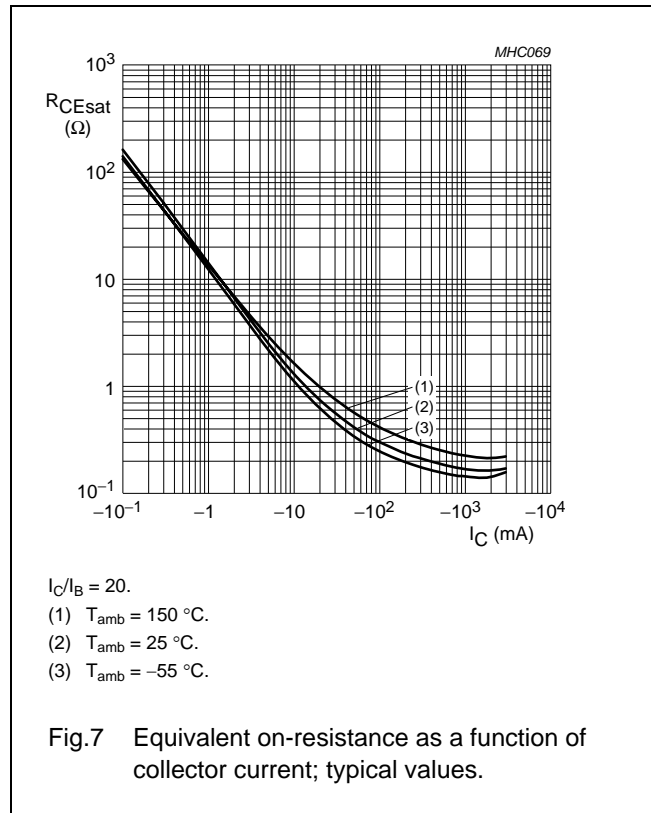
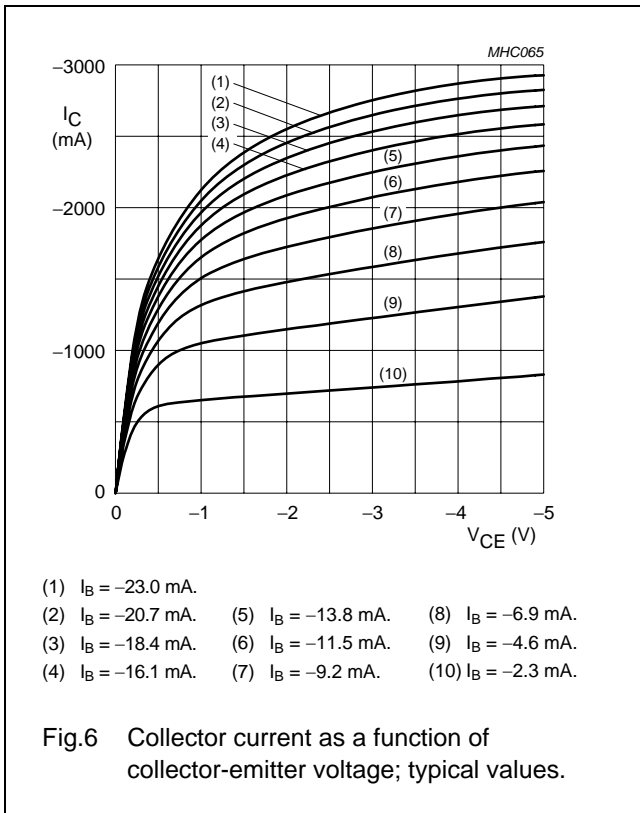
40 V, 2 A  
PNP low  $V_{CEsat}$  (BISS) transistor

PBSS5240T



40 V, 2 A  
PNP low  $V_{CEsat}$  (BISS) transistor

PBSS5240T



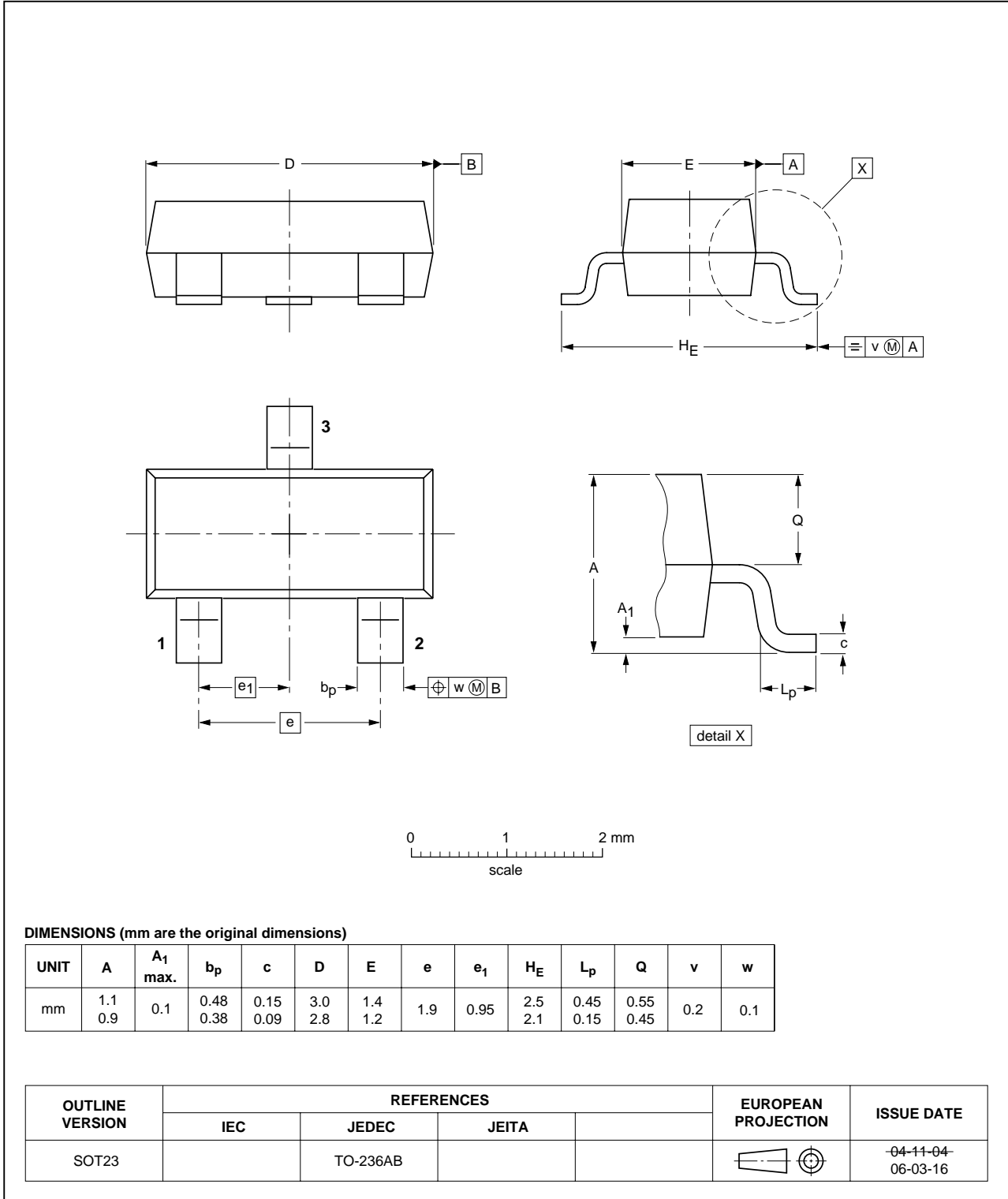
40 V, 2 A  
PNP low  $V_{CEsat}$  (BISS) transistor

PBSS5240T

PACKAGE OUTLINE

Plastic surface-mounted package; 3 leads

SOT23



40 V, 2 A  
PNP low  $V_{CEsat}$  (BISS) transistor

PBSS5240T

**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

**Notes**

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

**DISCLAIMERS**

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions

above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.



# ***NXP Semiconductors***

## **Customer notification**

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

## **Contact information**

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

© NXP B.V. 2009

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

R75/02/pp9

Date of release: 2004 Jan 15

Document order number: 9397 750 12439

