PCA9515A

I²C-bus repeater

Rev. 04 — 11 April 2008 **Product data sheet**

1. General description

The PCA9515A is a CMOS integrated circuit intended for application in I²C-bus and SMBus systems.

While retaining all the operating modes and features of the I²C-bus system, it permits extension of the I²C-bus by buffering both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400 pF.

The I²C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9515A enables the system designer to isolate two halves of a bus, thus more devices or longer length can be accommodated. It can also be used to run two buses, one at 5 V and the other at 3.3 V or a 400 kHz and 100 kHz bus, where the 100 kHz bus is isolated when 400 kHz operation of the other is required.

Two or more PCA9515A**s cannot be put in series.** The PCA9515A design does not allow this configuration. Since there is no direction pin, slightly different 'legal' low voltage levels are used to avoid lock-up conditions between the input and the output. A 'regular LOW' applied at the input of a PCA9515A will be propagated as a 'buffered LOW' with a slightly higher value. When this 'buffered LOW' is applied to another PCA9515A, PCA9516A or PCA9518/A in series, the second PCA9515A, PCA9516A or PCA9518/A will not recognize it as a 'regular LOW' and will not propagate it as a 'buffered LOW' again. The PCA9510/A, PCA9511/A, PCA9512/A, PCA9513/A, PCA9514/A cannot be used in series with the PCA9515A, PCA9516A or PCA9518/A, but can be used in series with themselves since they use shifting instead of static offsets to avoid lock-up conditions.

The output pull-down of each internal buffer is set for approximately 0.5 V, while the input threshold of each internal buffer is set about 0.07 V lower, when the output is internally driven LOW. This prevents a lock-up condition from occurring.

2. Features

- 2-channel, bidirectional buffer
- I²C-bus and SMBus compatible
- Active HIGH repeater enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I²C-bus devices and multiple masters
- Powered-off high-impedance I²C-bus pins
- Operating supply voltage range of 2.3 V to 3.6 V
- 5.5 V tolerant I²C-bus and enable pins

- 0 Hz to 400 kHz clock frequency (the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater)
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8 and TSSOP8 (MSOP8)

3. Ordering information

Table 1. Ordering information

$T_{amb} = -40\,°C$ to $+85\,°C$.

Type number	Topside mark	Package		
		Name	**Description**	**Version**
PCA9515AD	PA9515A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9515ADP	9515A	TSSOP8[1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

[1] Also known as MSOP8.

4. Functional diagram

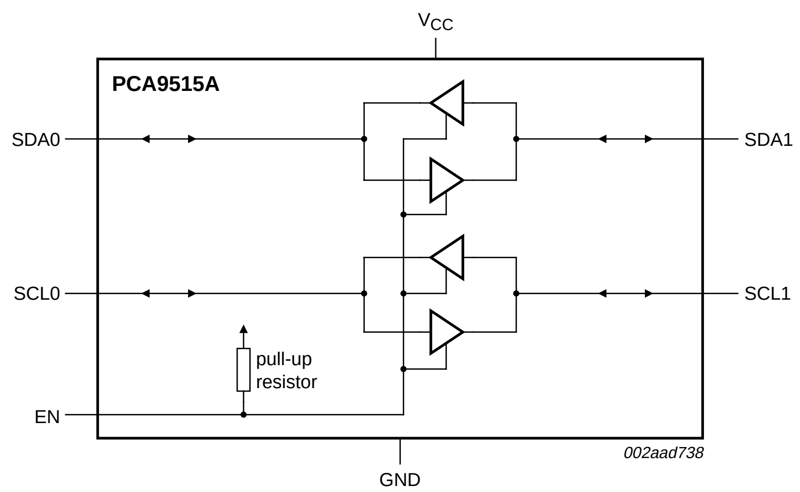


Fig 1. Functional diagram of PCA9515A

5. Pinning information

5.1 Pinning

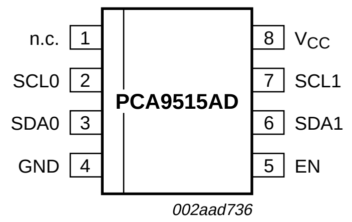


Fig 2. Pin configuration for SO8

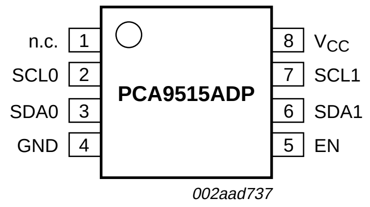


Fig 3. Pin configuration for TSSOP8 (MSOP8)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
SCL0	2	serial clock bus 0; open-drain 5 V tolerant I/O
SDA0	3	serial data bus 0; open-drain 5 V tolerant I/O
GND	4	supply ground (0 V)
EN	5	active HIGH repeater enable input (internal pull-up with 100 kΩ)
SDA1	6	serial data bus 1; open-drain 5 V tolerant I/O
SCL1	7	serial clock bus 1; open-drain 5 V tolerant I/O
V_{CC}	8	supply voltage

6. Functional description

Refer to Figure 1 "Functional diagram of PCA9515A".

The PCA9515A integrated circuit contains two identical buffer circuits which enable I^2C-bus and similar bus systems to be extended without degradation of system performance.

The PCA9515A contains two bidirectional, open-drain buffers specifically designed to support the standard LOW-level contention arbitration of the I^2C-bus. Except during arbitration or clock stretching, the PCA9515A acts like a pair of non-inverting, open-drain buffers, one for SDA and one for SCL.

6.1 Enable

The EN pin is active HIGH with an internal pull-up and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I^2C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^2C-bus parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

6.2 I^2C-bus systems

As with the standard I^2C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I^2C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard-mode and Fast-mode I^2C-bus devices in addition to SMBus devices. Standard-mode I^2C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I^2C-bus system where Standard-mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

Please see Application Note *AN255, I^2C/SMBus Repeaters, Hubs and Expanders* for additional information on sizing resistors and precautions when using more than one PCA9515A/PCA9516A in a system or using the PCA9515A/PCA9516A in conjunction with the P82B96.

7. Application design-in information

A typical application is shown in Figure 4. In this example, the system master is running on a 3.3 V I^2C-bus while the slave is connected to a 5 V bus. Both buses run at 100 kHz unless the slave bus is isolated and then the master bus can run at 400 kHz. Master devices can be placed on either bus.

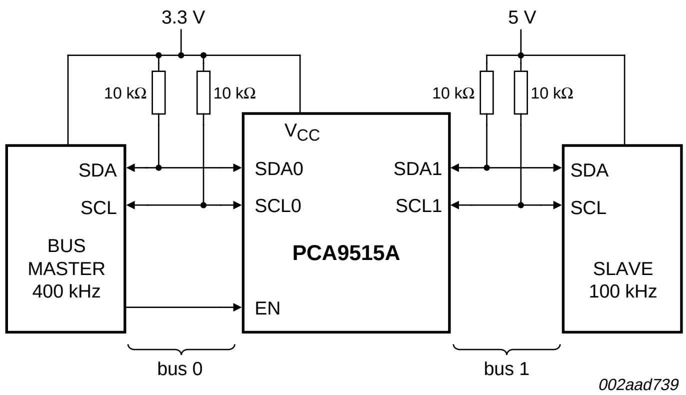


Fig 4. Typical application

The PCA9515A is 5 V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9515A is pulled LOW by a device on the I^2C-bus, a CMOS hysteresis type input detects the falling edge and causes the internal driver on the other side to turn on, thus causing the other side to also go LOW. The side driven LOW by the PCA9515A will typically be at V_{OL} = 0.5 V.

In order to illustrate what would be seen in a typical application, refer to Figure 5 and Figure 6. If the bus master in Figure 4 were to write to the slave through the PCA9515A, we would see the waveform shown in Figure 5 on bus 0. This looks like a normal I^2C-bus transmission until the falling edge of the 8^{th} clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it LOW through the PCA9515A. Because the V_{OL} of the PCA9515A is typically round 0.5 V, a step in the SDA will be seen. After the master has transmitted the 9^{th} clock pulse, the slave releases the data line.

On the bus 1 side of the PCA9515A, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9515A. After the 8^{th} clock pulse the data line will be pulled to the V_{OL} of the slave device, which is very close to ground in this example. It is important to note that any arbitration or clock stretching events on bus 1 require that the V_{OL} of the PCA9515A (see V_{OL}–V_{ILc} in Section 9 "Static characteristics") to be recognized by the PCA9515A and then transmitted to bus 0.

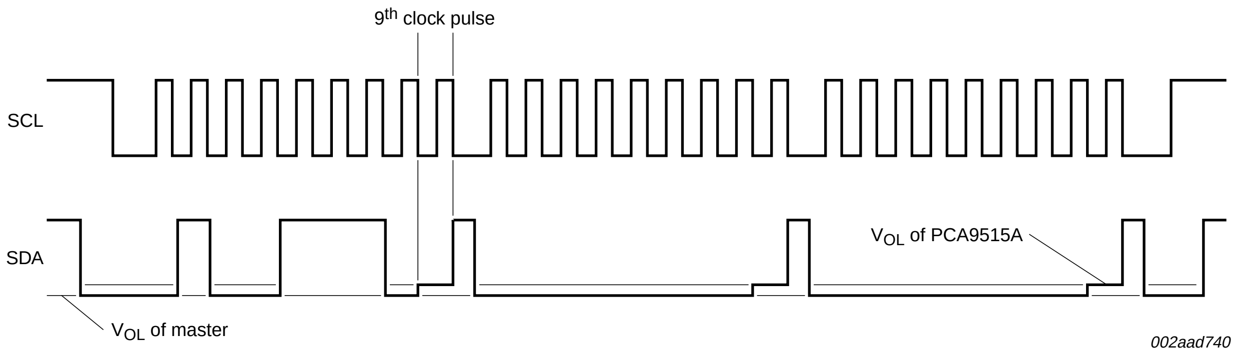


Fig 5. Bus 0 waveform

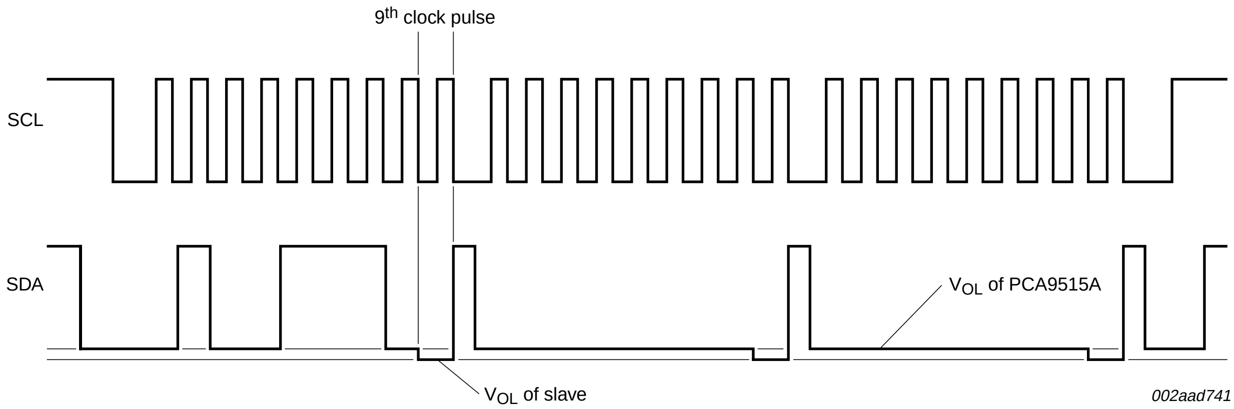


Fig 6. Bus 1 waveform

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages with respect to pin GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
V_{bus}	voltage on I^2C-bus, SCL or SDA		–0.5	+7	V
I	DC current	any pin	-	50	mA
P_{tot}	total power dissipation		-	100	mW
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature	operating in free air	–40	+85	°C

9. Static characteristics

Table 4. Static characteristics (V_{CC} = 3.0 V to 3.6 V)

V_{CC} = 3.0 V to 3.6 V[1]; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Supplies							
V_{CC}	supply voltage			3.0	-	3.6	V
I_{CCH}	HIGH-level supply current	both channels HIGH; V_{CC} = 3.6 V; SDAn = SCLn = V_{CC}		-	0.8	5	mA
I_{CCL}	LOW-level supply current	both channels LOW; V_{CC} = 3.6 V; one SDA and one SCL = GND; other SDA and SCL open		-	1.7	5	mA
I_{CCLc}	contention LOW-level supply current	V_{CC} = 3.6 V; SDAn = SCLn = GND		-	1.6	5	mA
Input SCLn; input/output SDAn							
V_{IH}	HIGH-level input voltage			$0.7V_{CC}$	-	5.5	V
V_{IL}	LOW-level input voltage		[3]	−0.5	-	$+0.3V_{CC}$	V
V_{ILc}	contention LOW-level input voltage		[3]	−0.5	-	+0.4	V
V_{IK}	input clamping voltage	I_I = −18 mA		-	-	−1.2	V
I_{LI}	input leakage current	V_I = 3.6 V		−1	-	+1	μA
I_{IL}	LOW-level input current	SDAn, SCLn; V_I = 0.2 V		-	-	5	μA
V_{OL}	LOW-level output voltage	I_{OL} = 20 μA or 6 mA		0.47	0.52	0.6	V
$V_{OL}-V_{ILc}$	difference between LOW-level output and LOW-level input voltage contention	guaranteed by design		-	-	70	mV
C_i	input capacitance	V_I = 3 V or 0 V		-	6	7	pF
Enable							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2 V		-	−10	−30	μA
I_{LI}	input leakage current			−1	-	+1	μA
C_i	input capacitance	V_I = 3.0 V or 0 V		-	6	7	pF

[1] For operation between published voltage ranges, refer to worst-case parameter in both ranges.

[2] Typical value taken at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[3] V_{IL} specification is for the first LOW level seen by the SDAn/SCLn lines. V_{ILc} is for the second and subsequent LOW levels seen by the SDAn/SCLn lines.

Table 5. Static characteristics (V_{CC} = 2.3 V to 2.7 V)

V_{CC} = 2.3 V to 2.7 V[1]; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Supplies							
V_{CC}	supply voltage			2.3	-	2.7	V
I_{CCH}	HIGH-level supply current	both channels HIGH; V_{CC} = 2.7 V; SDAn = SCLn = V_{CC}		-	0.8	5	mA
I_{CCL}	LOW-level supply current	both channels LOW; V_{CC} = 2.7 V; one SDA and one SCL = GND; other SDA and SCL open		-	1.6	5	mA
I_{CCLc}	contention LOW-level supply current	V_{CC} = 2.7 V; SDAn = SCLn = GND		-	1.6	5	mA
Input SCLn; input/output SDAn							
V_{IH}	HIGH-level input voltage			$0.7V_{CC}$	-	5.5	V
V_{IL}	LOW-level input voltage		[3]	−0.5	-	$+0.3V_{CC}$	V
V_{ILc}	contention LOW-level input voltage		[3]	−0.5	-	+0.4	V
V_{IK}	input clamping voltage	I_I = −18 mA		-	-	−1.2	V
I_{LI}	input leakage current	V_I = 2.7 V		−1	-	+1	µA
I_{IL}	LOW-level input current	SDAn, SCLn; V_I = 0.2 V		-	-	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 20 µA or 6 mA		0.47	0.52	0.6	V
$V_{OL}-V_{ILc}$	difference between LOW-level output and LOW-level input voltage contention	guaranteed by design		-	-	70	mV
C_i	input capacitance	V_I = 3 V or 0 V		-	6	7	pF
Enable							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2 V		-	−10	−30	µA
I_{LI}	input leakage current			−1	-	+1	µA
C_i	input capacitance	V_I = 3.0 V or 0 V		-	6	7	pF

[1] For operation between published voltage ranges, refer to worst-case parameter in both ranges.

[2] Typical value taken at V_{CC} = 2.5 V and T_{amb} = 25 °C.

[3] V_{IL} specification is for the first LOW level seen by the SDAn/SCLn lines. V_{ILc} is for the second and subsequent LOW levels seen by the SDAn/SCLn lines.

10. Dynamic characteristics

Table 6. Dynamic characteristics (V_{CC} = 2.3 V to 2.7 V)

V_{CC} = 2.3 V to 2.7 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay	Figure 7		45	82	130	ns
t_{PLH}	LOW-to-HIGH propagation delay	Figure 7	[2]	33	113	190	ns
t_{THL}	HIGH to LOW output transition time	Figure 7		-	57	-	ns
t_{TLH}	LOW to HIGH output transition time	Figure 7	[2]	-	148	-	ns
t_{su}	set-up time	EN HIGH before START condition		100	-	-	ns
t_h	hold time	EN HIGH after STOP condition		130	-	-	ns

[1] Typical values taken at V_{CC} = 2.5 V and T_{amb} = 25 °C.

[2] Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

Table 7. Dynamic characteristics (V_{CC} = 3.0 V to 3.6 V)

V_{CC} = 3.0 V to 3.6 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay	Figure 7		45	68	120	ns
t_{PLH}	LOW-to-HIGH propagation delay	Figure 7	[2]	33	102	180	ns
t_{THL}	HIGH to LOW output transition time	Figure 7		-	58	-	ns
t_{TLH}	LOW to HIGH output transition time	Figure 7	[2]	-	147	-	ns
t_{su}	set-up time	EN HIGH before START condition		100	-	-	ns
t_h	hold time	EN HIGH after STOP condition		100	-	-	ns

[1] Typical values taken at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

10.1 AC waveforms

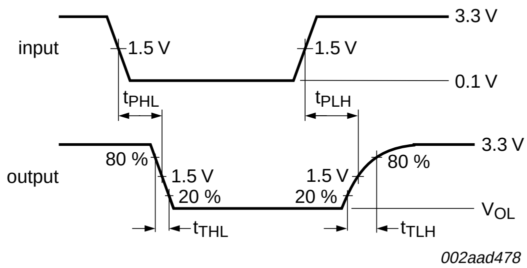
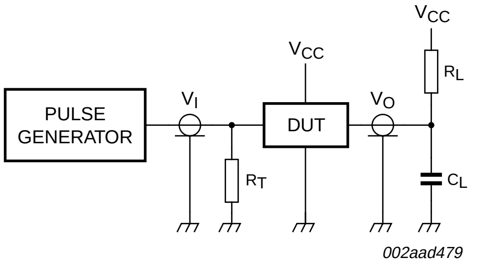


Fig 7. Propagation delay and transition times

11. Test information



R_L = load resistor; 1.35 kΩ

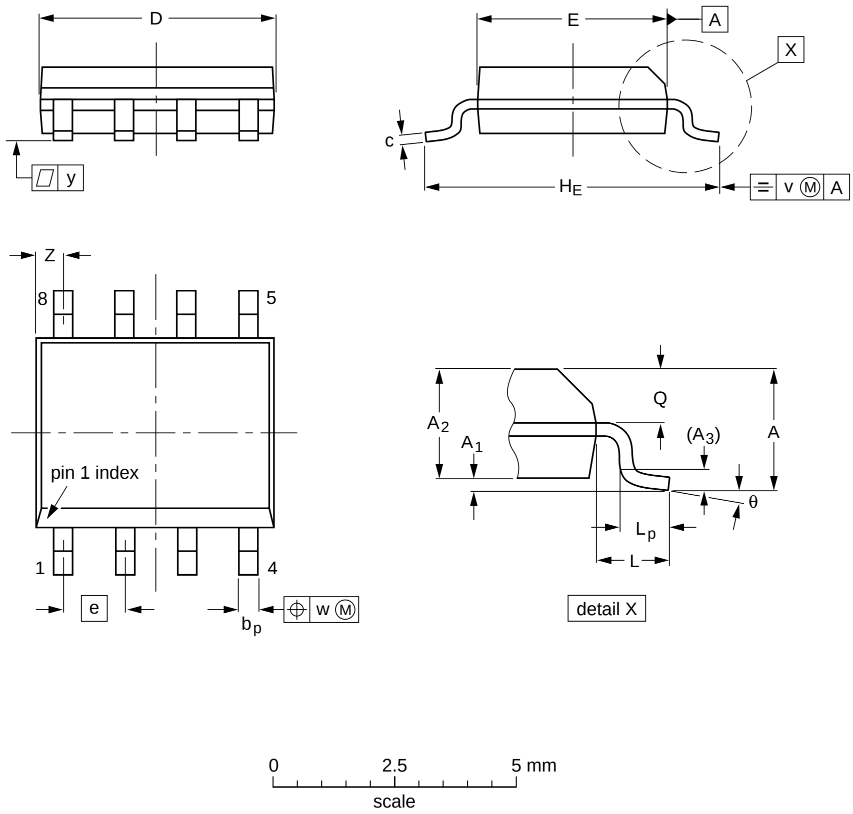
C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Fig 8. Test circuit for open-drain outputs

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

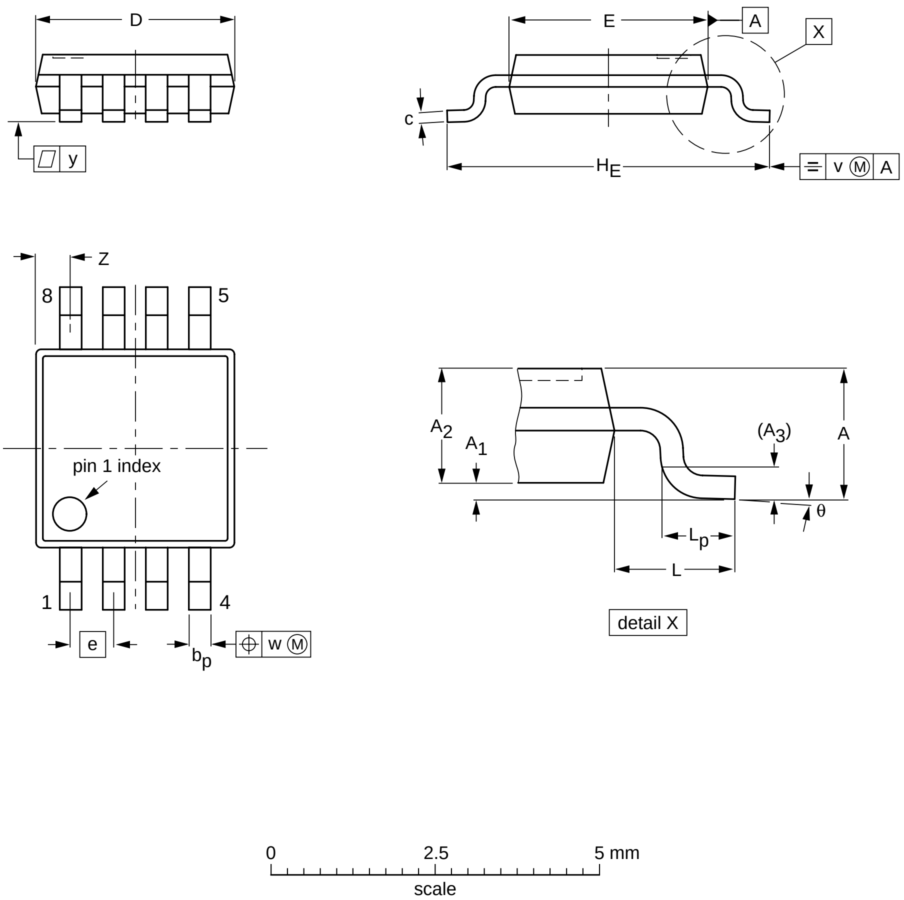
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 9. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

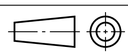
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 10. Package outline SOT505-1 (TSSOP8)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020C)

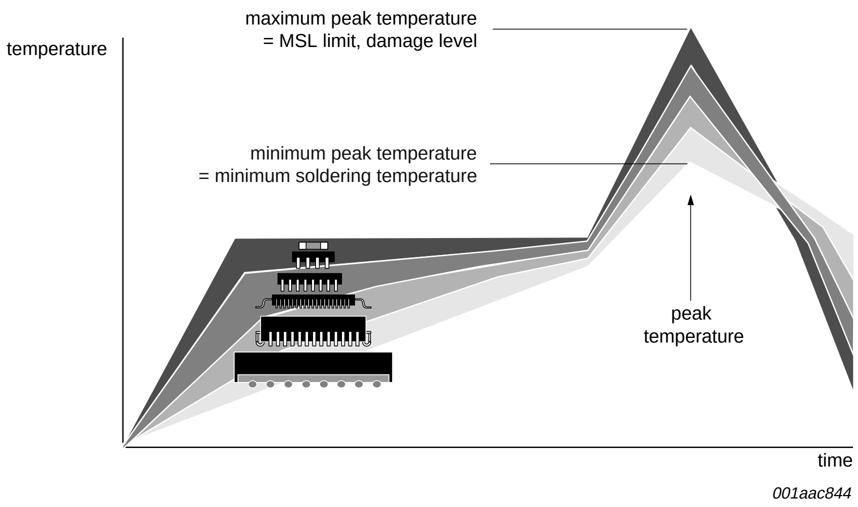
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
MM	Machine Model
SMBus	System Management Bus

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9515A_4	20080411	Product data sheet	-	PCA9515A_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 1 "General description", 4th paragraph: 5th and 6th sentences re-written • Table 2 "Pin description": – appended "open-drain 5 V tolerant I/O" to the descriptions of SCL0 (pin 2), SDA0 (pin 3), SDA1 (pin 6), and SCL1 (pin 7) – appended "(internal pull-up with 100 kΩ)" to the description of EN (pin 5) • Table 4 "Static characteristics (V_{CC} = 3.0 V to 3.6 V)" and Table 5 "Static characteristics (V_{CC} = 2.3 V to 2.7 V)": – changed parameter description for I_{CCH} from "quiescent supply current, both channels HIGH" to "HIGH-level supply current" (moved "both channels HIGH" to Conditions column) – changed parameter description for I_{CCL} from "quiescent supply current, both channels LOW" to "LOW-level supply current" (moved "both channels LOW" to Conditions column) – sub-section "Enable": changed symbol/parameter from "I_{IL}, input current LOW, EN" to "$I_{IL(EN)}$, LOW-level input current on pin EN" • Table 6 "Dynamic characteristics (V_{CC} = 2.3 V to 2.7 V)" and Table 7 "Dynamic characteristics (V_{CC} = 3.0 V to 3.6 V)": – changed symbol/parameter from "t_{SET}, Enable to Start condition" to "t_{su}, set-up time"; added "EN HIGH before START condition" to Conditions column – changed symbol/parameter from "t_{HOLD}, Enable after Stop condition" to "t_h, hold time"; added "EN HIGH after STOP condition" to Conditions column • Added SMD package soldering information • Added Section 14 "Abbreviations"			
PCA9515A_3 (9397 750 14098)	20040929	Product data sheet	-	PCA9515A_2
PCA9515A_2 (9397 750 13709)	20040709	Product data sheet	-	PCA9515A_1
PCA9515A_1 (9397 98 13237)	20040617	Objective data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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