PCA9554/PCA9554A

8-bit I^2C-bus and SMBus I/O port with interrupt

Rev. 07 — 13 November 2006 Product data sheet

1. General description

The PCA9554 and PCA9554A are 16-pin CMOS devices that provide 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I^2C-bus/SMBus applications and were developed to enhance the NXP Semiconductors family of I^2C-bus I/O expanders. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, 400 kHz clock frequency, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PCA9554/PCA9554A consist of an 8-bit Configuration register (Input or Output selection); 8-bit Input Port register, 8-bit Output Port register and an 8-bit Polarity Inversion register (active HIGH or active LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master. Although pin-to-pin and I^2C-bus address compatible with the PCF8574 series, software changes are required due to the enhancements and are discussed in *Application Note AN469*.

The PCA9554/PCA9554A open-drain interrupt output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I^2C-bus address and allow up to eight devices to share the same I^2C-bus/SMBus. The PCA9554A is identical to the PCA9554 except that the fixed I^2C-bus address is different allowing up to sixteen of these devices (eight of each) on the same I^2C-bus/SMBus.

2. Features

- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- 0 Hz to 400 kHz clock frequency

founded by Philips

- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: DIP16, SO16, SSOP16, SSOP20, TSSOP16, HVQFN16 (2 versions: 4 × 4 × 0.85 mm and 3 × 3 × 0.85 mm), and bare die

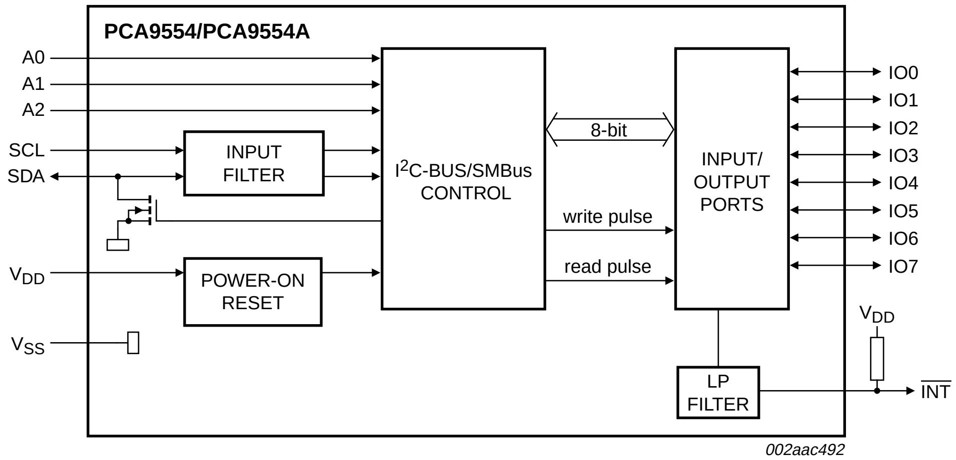
3. Ordering information

Table 1. Ordering information

T_{amb} = −40 °C to +85 °C.

Type number	Topside mark	Package		
		Name	Description	Version
PCA9554N	PCA9554N	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
PCA9554AN	PCA9554AN			
PCA9554D	PCA9554D	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA9554AD	PCA9554AD			
PCA9554DB	9554DB	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
PCA9554ADB	9554A			
PCA9554TS	PCA9554	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1
PCA9554ATS	PA9554A			
PCA9554PW	9554DH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9554APW	9554ADH			
PCA9554BS	9554	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm	SOT629-1
PCA9554ABS	554A			
PCA9554BS3	P54	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA9554ABS3	54A			
PCA9554U	-	bare die	-	-

4. Block diagram



All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCA9554/PCA9554A

5. Pinning information

5.1 Pinning

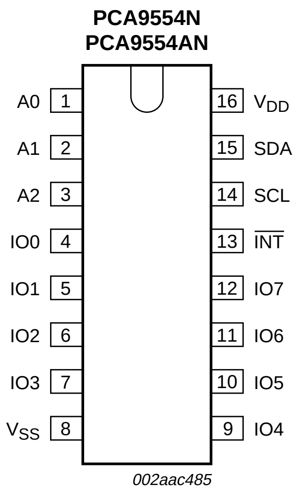


Fig 2. Pin configuration for DIP16

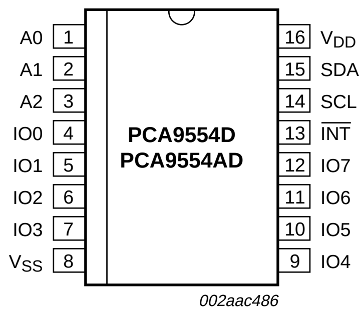


Fig 3. Pin configuration for SO16

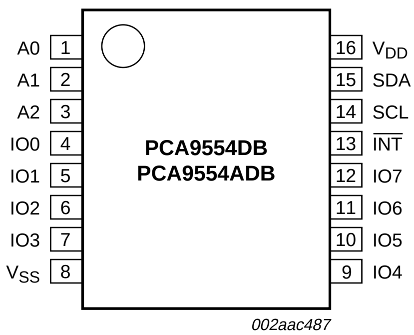


Fig 4. Pin configuration for SSOP16

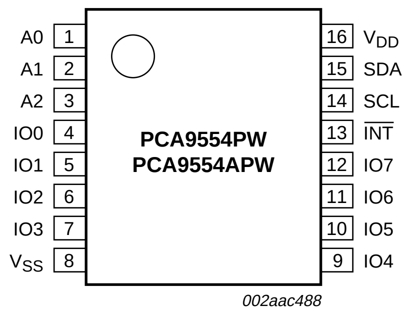


Fig 5. Pin configuration for TSSOP16

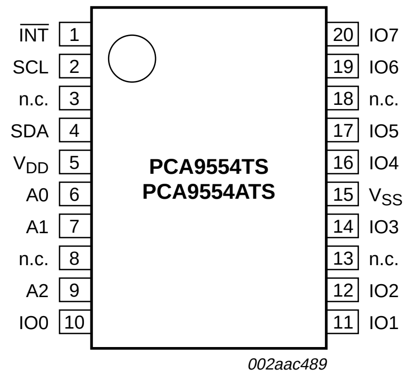


Fig 6. Pin configuration for SSOP20

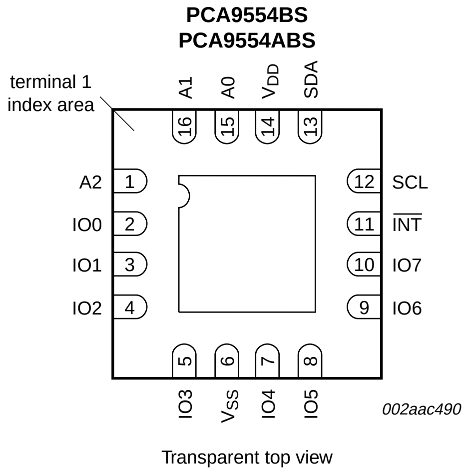


Fig 7. Pin configuration for HVQFN16 (SOT629-1)

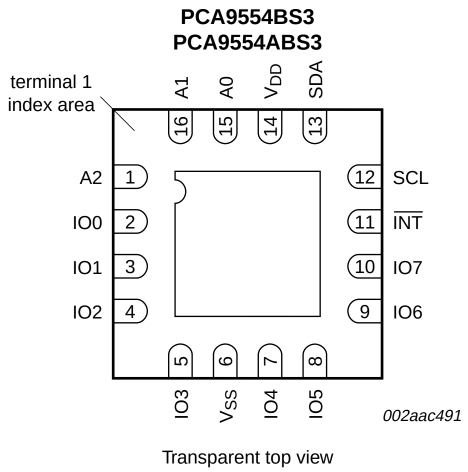


Fig 8. Pin configuration for HVQFN16 (SOT758-1)

5.2 Pin description

Table 2. Pin description

Symbol	Pin			Description
	DIP16, SO16, SSOP16, TSSOP16	HVQFN16	SSOP20	
A0	1	15	6	address input 0
A1	2	16	7	address input 1
A2	3	1	9	address input 2
IO0	4	2	10	input/output 0
IO1	5	3	11	input/output 1
IO2	6	4	12	input/output 2
IO3	7	5	14	input/output 3
V_{SS}	8	6[1]	15	supply ground
IO4	9	7	16	input/output 4
IO5	10	8	17	input/output 5
IO6	11	9	19	input/output 6
IO7	12	10	20	input/output 7
$\overline{INT}$	13	11	1	interrupt output (open-drain)
SCL	14	12	2	serial clock line
SDA	15	13	4	serial data line
V_{DD}	16	14	5	supply voltage
n.c.	-	-	3, 8, 13, 18	not connected

[1] HVQFN package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

Refer to Figure 1 “Block diagram of PCA9554/PCA9554A”.

6.1 Registers

6.1.1 Command byte

Table 3. Command byte

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

6.1.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default ‘X’ is determined by the externally applied logic level, normally ‘1’ when no external signal externally applied because of the internal pull-up resistors.

Table 4. Register 0 - Input Port register bit description

Bit	Symbol	Access	Value	Description
7	I7	read only	X	determined by externally applied logic level
6	I6	read only	X	
5	I5	read only	X	
4	I4	read only	X	
3	I3	read only	X	
2	I2	read only	X	
1	I1	read only	X	
0	I0	read only	X	

6.1.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 5. Register 1 - Output Port register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	O7	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

6.1.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with ‘1’), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a ‘0’), the Input Port data polarity is retained.

Table 6. Register 2 - Polarity Inversion register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	inverts polarity of Input Port register data 0 = Input Port register data retained (default value) 1 = Input Port register data inverted
6	N6	R/W	0*	
5	N5	R/W	0*	
4	N4	R/W	0*	
3	N3	R/W	0*	
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

6.1.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V_{DD}.

Table 7. Register 3 - Configuration register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	configures the directions of the I/O pins 0 = corresponding port pin enabled as an output 1 = corresponding port pin configured as input (default value)
6	C6	R/W	1*	
5	C5	R/W	1*	
4	C4	R/W	1*	
3	C3	R/W	1*	
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

6.2 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9554/PCA9554A in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9554/PCA9554A registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

6.3 Interrupt output

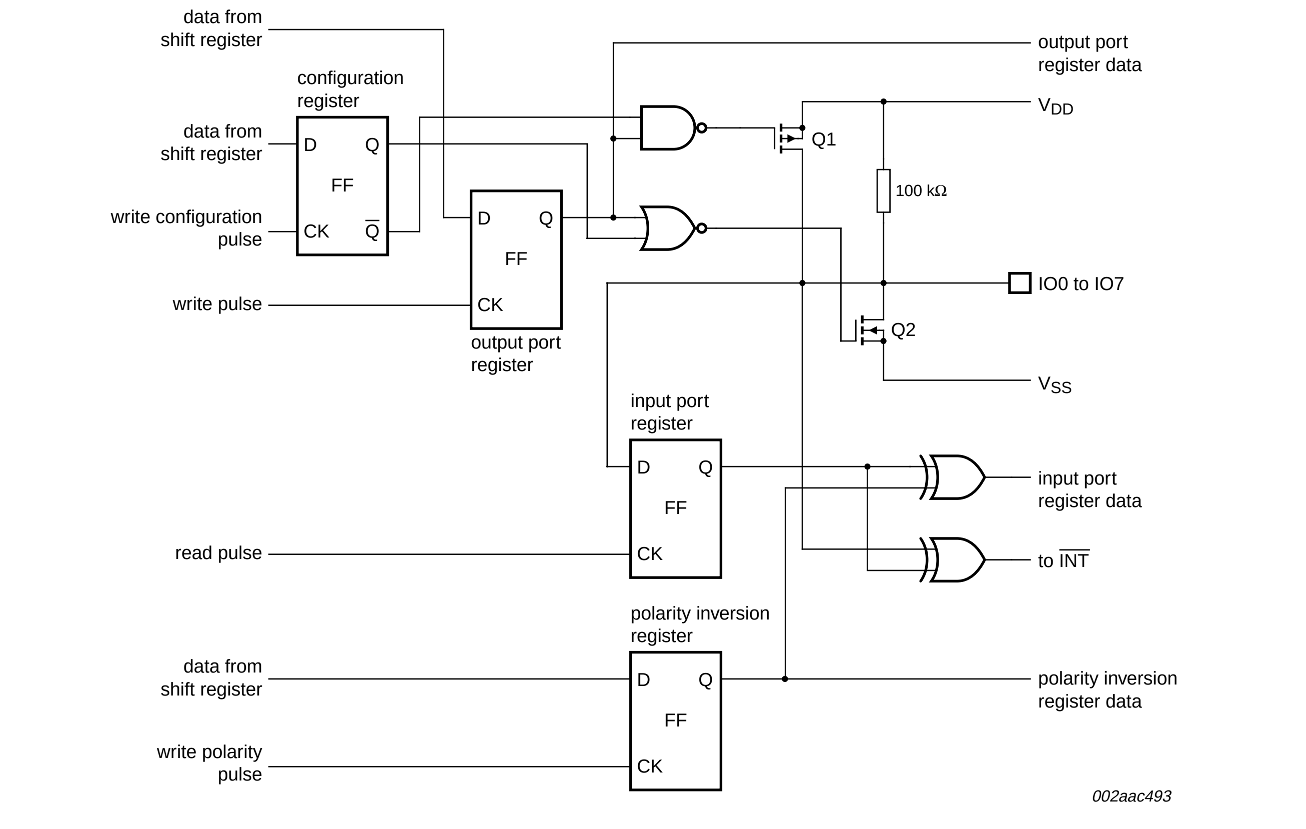
The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read.

Note that changing an I/O from and output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

6.4 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 kΩ typ.) to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either V_{DD} or V_{SS}.



Remark: At power-on reset, all registers return to default values.

Fig 9. Simplified schematic of IO0 to IO7

6.5 Device address

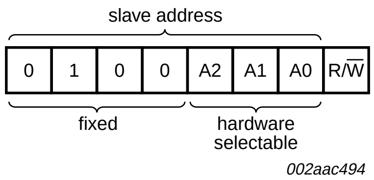


Fig 10. PCA9554 device address

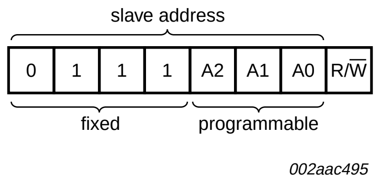


Fig 11. PCA9554A device address

6.6 Bus transactions

Data is transmitted to the PCA9554/PCA9554A registers using the Write mode as shown in Figure 12 and Figure 13. Data is read from the PCA9554/PCA9554A registers using the Read mode as shown in Figure 14 and Figure 15. These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

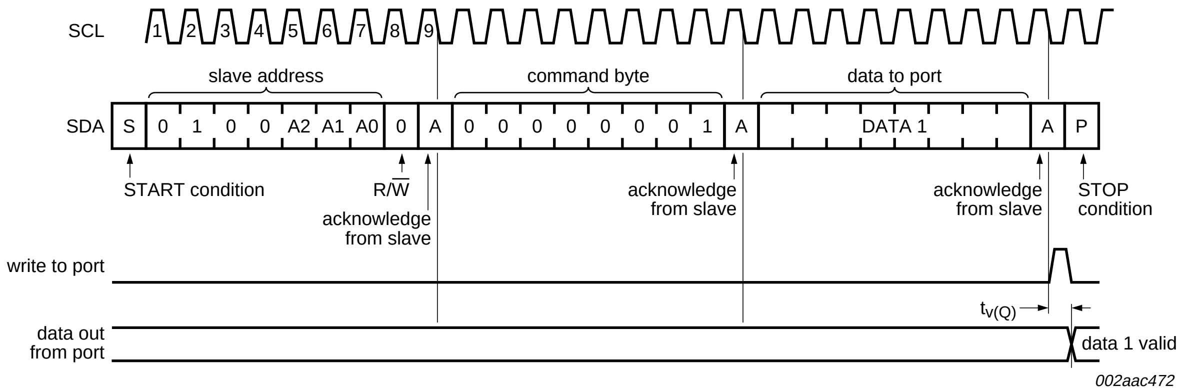


Fig 12. Write to Output Port register

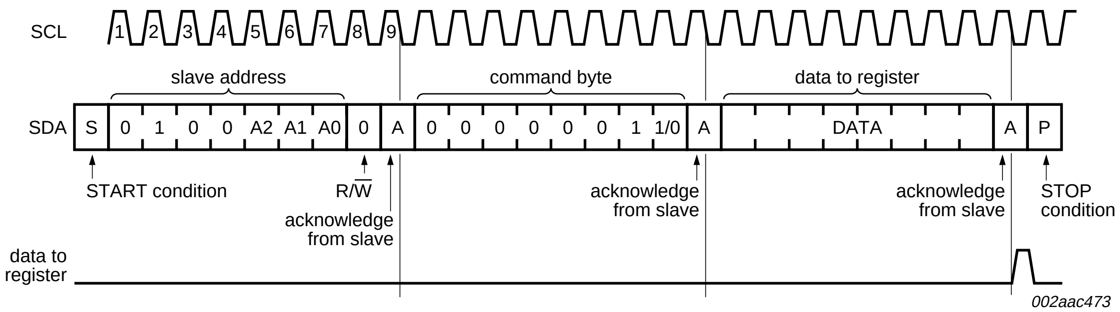


Fig 13. Write to Configuration register or Polarity Inversion register

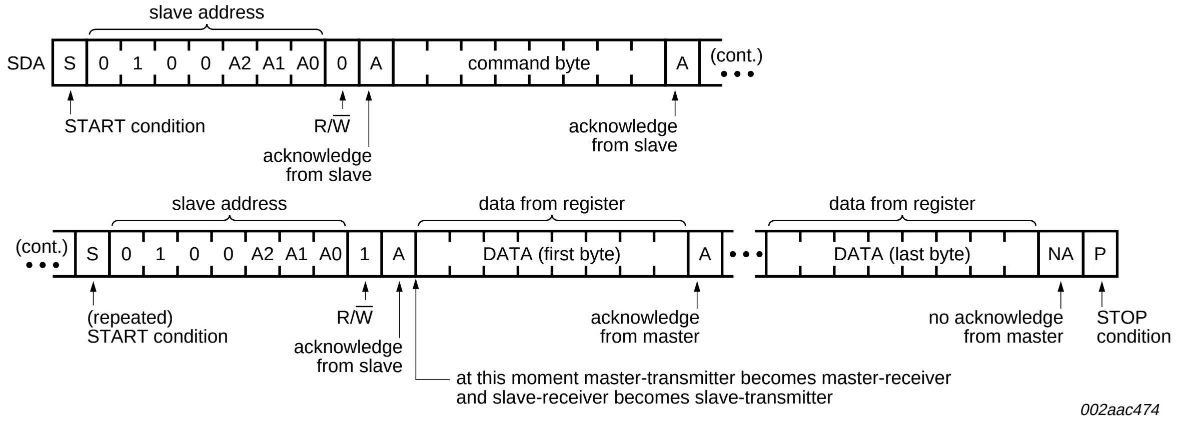
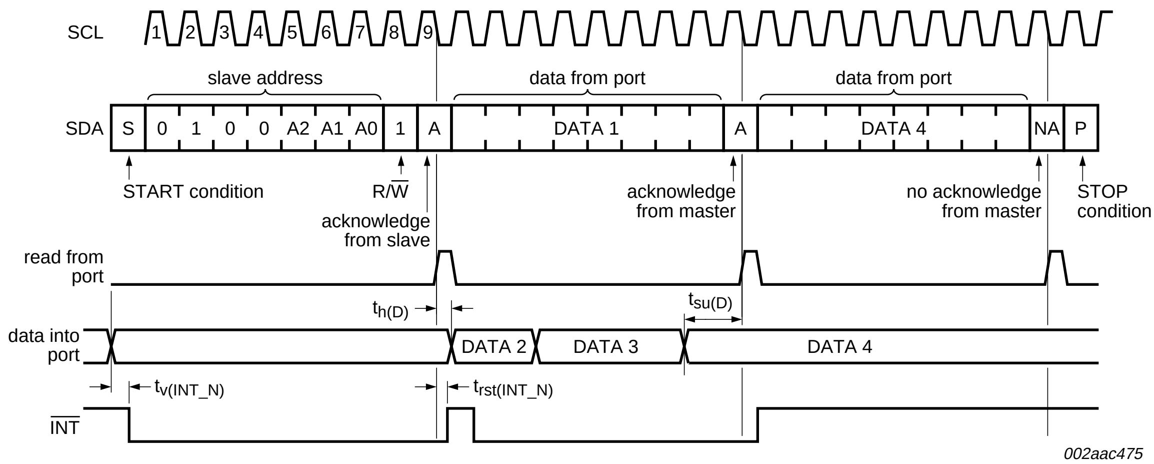


Fig 14. Read from register

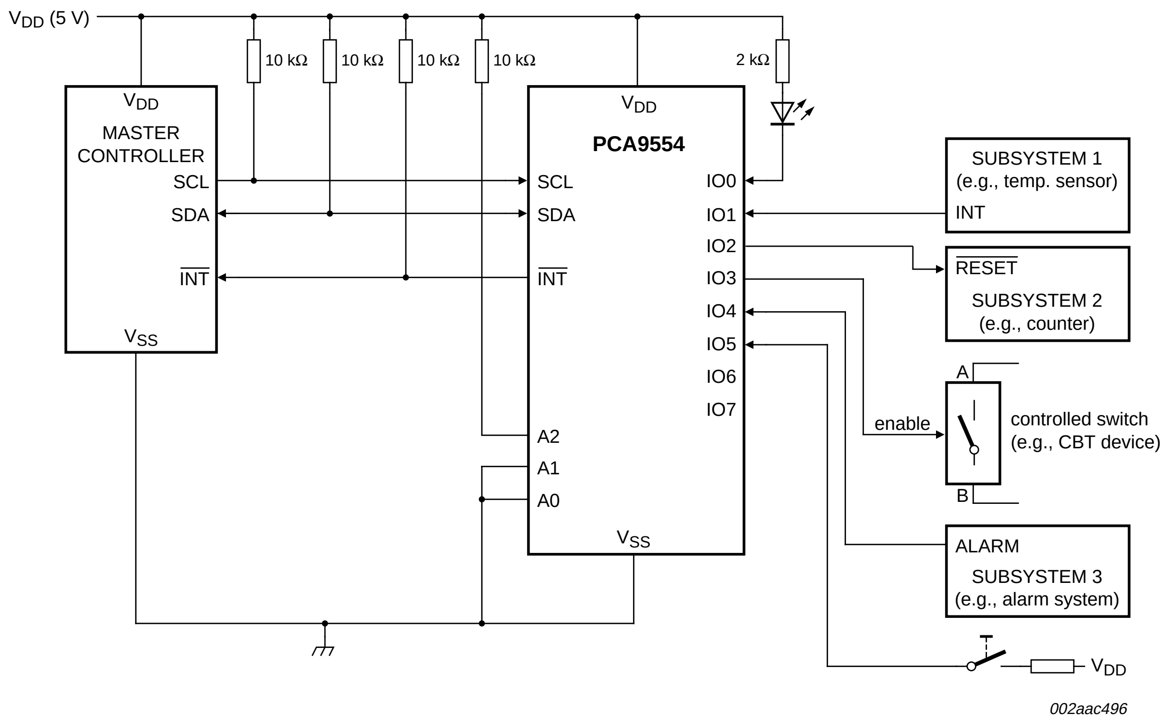


This figure assumes the command byte has previously been programmed with 00h.

Transfer of data can be stopped at any moment by a STOP condition.

Fig 15. Read Input Port register

7. Application design-in information



Device address configured as 0100 100X for this example.

IO0, IO1, IO2 configured as outputs.

IO3, IO4, IO5 configured as inputs.

IO6 and IO7 are not used and must be configured as outputs.

Fig 16. Typical application

8. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.0	V
I_I	input current		-	±20	mA
$V_{I/O}$	voltage on an input/output pin		V_{SS} – 0.5	5.5	V
$I_{O(IOn)}$	output current on pin IOn		-	±50	mA
I_{DD}	supply current		-	85	mA
I_{SS}	ground supply current		-	100	mA
P_{tot}	total power dissipation		-	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

9. Static characteristics

Table 9. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		2.3	-	5.5	V
I_{DD}	supply current	operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz	-	104	175	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	-	550	700	µA
		Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs	-	0.25	1	µA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS} [1]	-	1.5	1.65	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	6	-	mA
I_L	leakage current	$V_I = V_{DD} = V_{SS}$	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	6	10	pF
I/Os						
V_{IL}	LOW-level input voltage		−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V [2]	8	10	-	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V [2]	10	13	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V [2]	8	14	-	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V [2]	10	19	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V [2]	8	17	-	mA
		V_{OL} = 0.7 V; V_{DD} = 4.5 V [2]	10	24	-	mA
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; V_{DD} = 2.3 V [3]	1.8	-	-	V
		I_{OH} = −10 mA; V_{DD} = 2.3 V [3]	1.7	-	-	V
		I_{OH} = −8 mA; V_{DD} = 3.0 V [3]	2.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V [3]	2.5	-	-	V
		I_{OH} = −8 mA; V_{DD} = 4.75 V [3]	4.1	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.75 V [3]	4.0	-	-	V
I_{IH}	input leakage current	V_{DD} = 3.6 V; $V_I = V_{DD}$	-	-	1	µA
I_{IL}	input leakage current	V_{DD} = 5.5 V; $V_I = V_{SS}$	-	-	−100	µA
C_i	input capacitance		-	3.7	5	pF
C_o	output capacitance		-	3.7	5	pF
Interrupt $\overline{INT}$						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA

Table 9. Static characteristics *...continued*

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Select inputs A0, A1, A2						
V_{IL}	LOW-level input voltage		−0.5	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
I_{LI}	input leakage current		−1	-	1	µA

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3] The total current sourced by all I/Os must be limited to 85 mA.

10. Dynamic characteristics

Table 10. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I^2C-bus		Fast-mode I^2C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	µs
$t_{VD:ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	µs
$t_{VD;DAT}$	data valid time	[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$[3]	300	ns
t_f	fall time of both SDA and SCL signals		-	300	$20 + 0.1C_b$[3]	300	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
$t_{v(Q)}$	data output valid time		-	200	-	200	ns
$t_{su(D)}$	data input setup time		100	-	100	-	ns
$t_{h(D)}$	data input hold time		1	-	1	-	µs
Interrupt timing							
$t_{v(INT\_N)}$	valid time on pin $\overline{INT}$		-	4	-	4	µs
$t_{rst(INT\_N)}$	reset time on pin $\overline{INT}$		-	4	-	4	µs

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data output to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

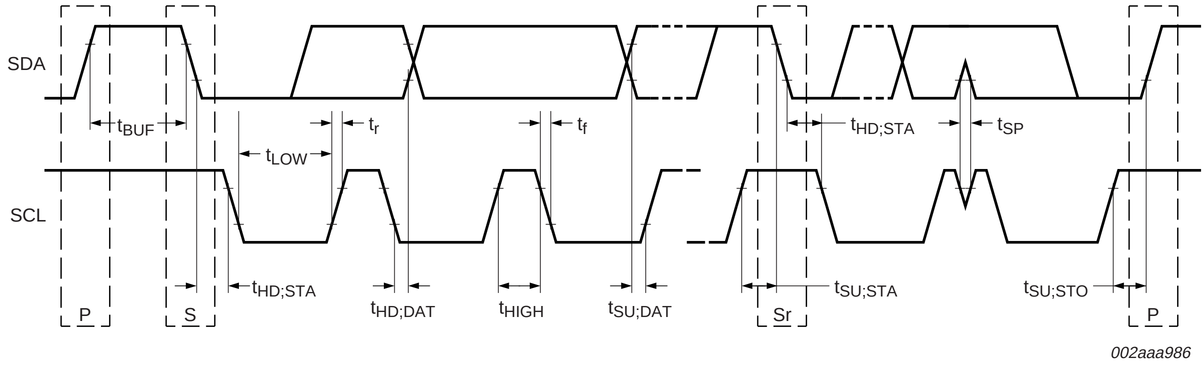
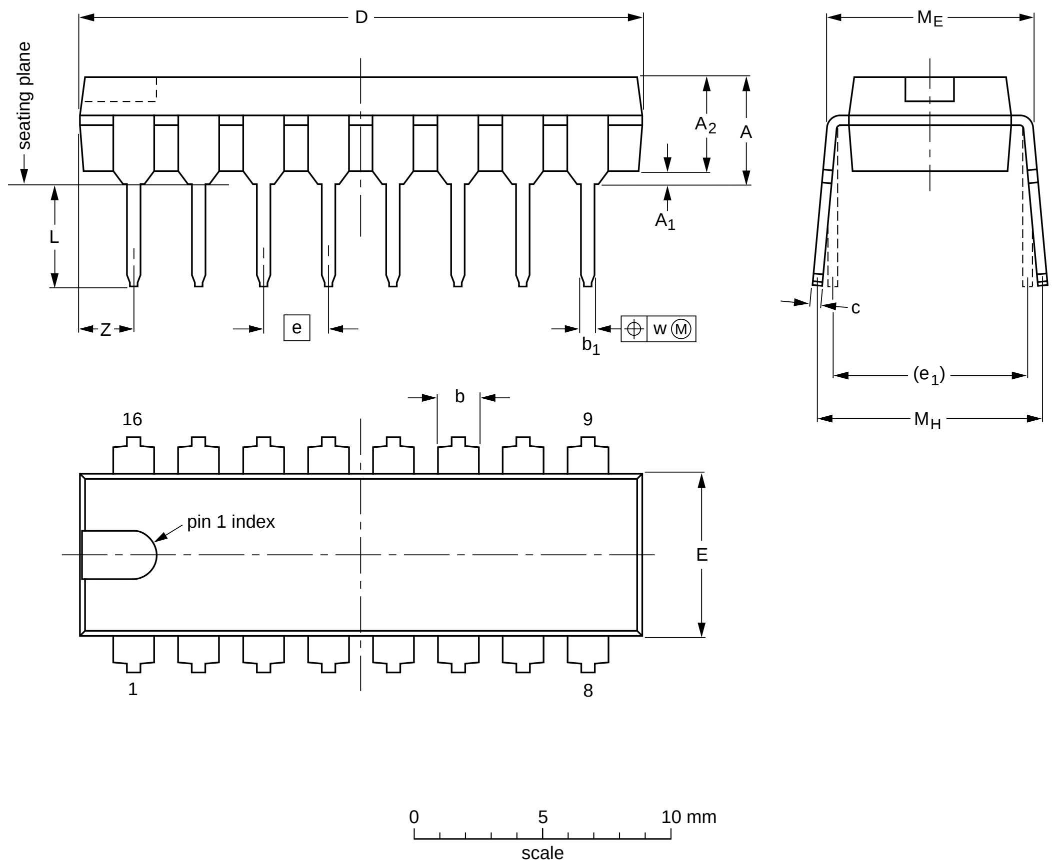


Fig 17. Definition of timing

11. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

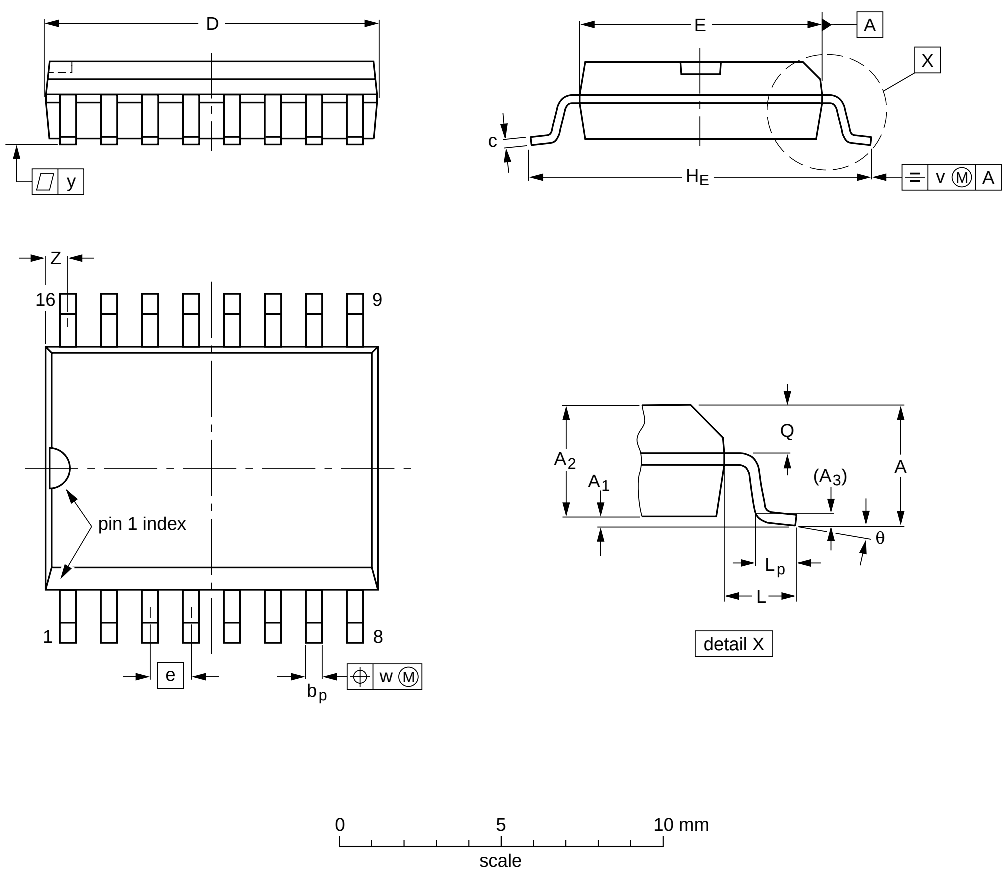
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

Fig 18. Package outline SOT38-1 (DIP16)

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

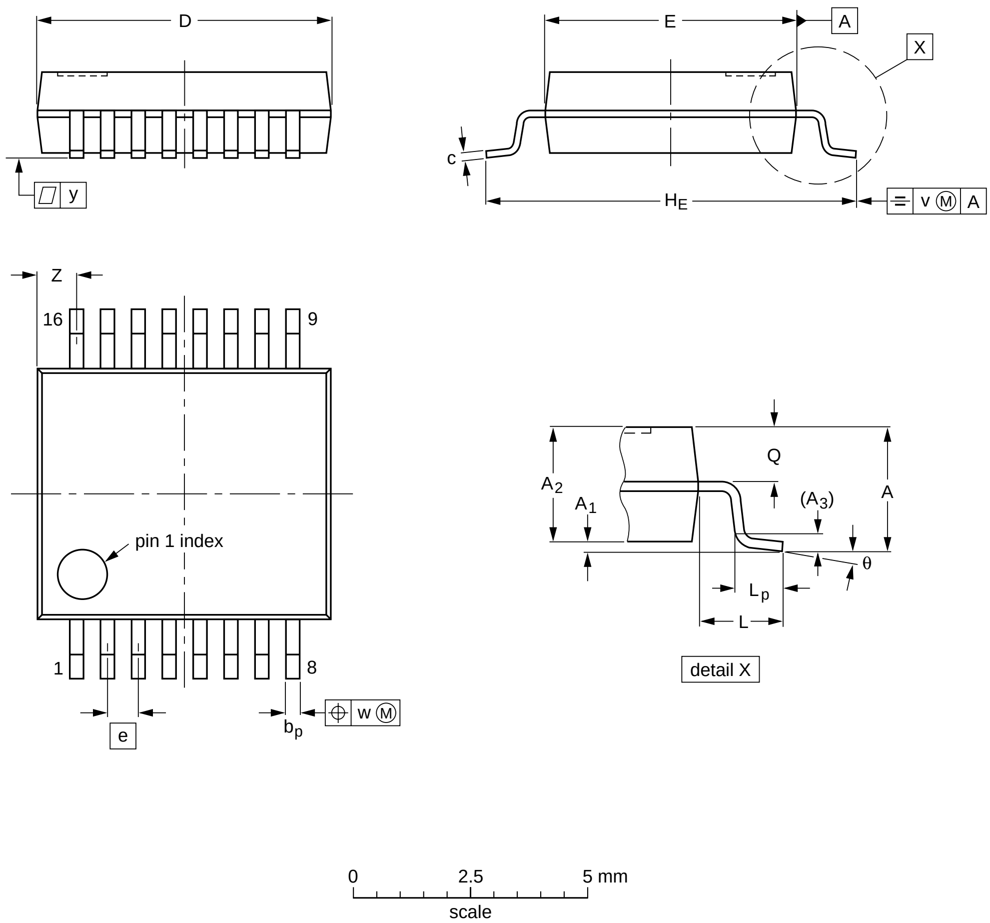
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT162-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

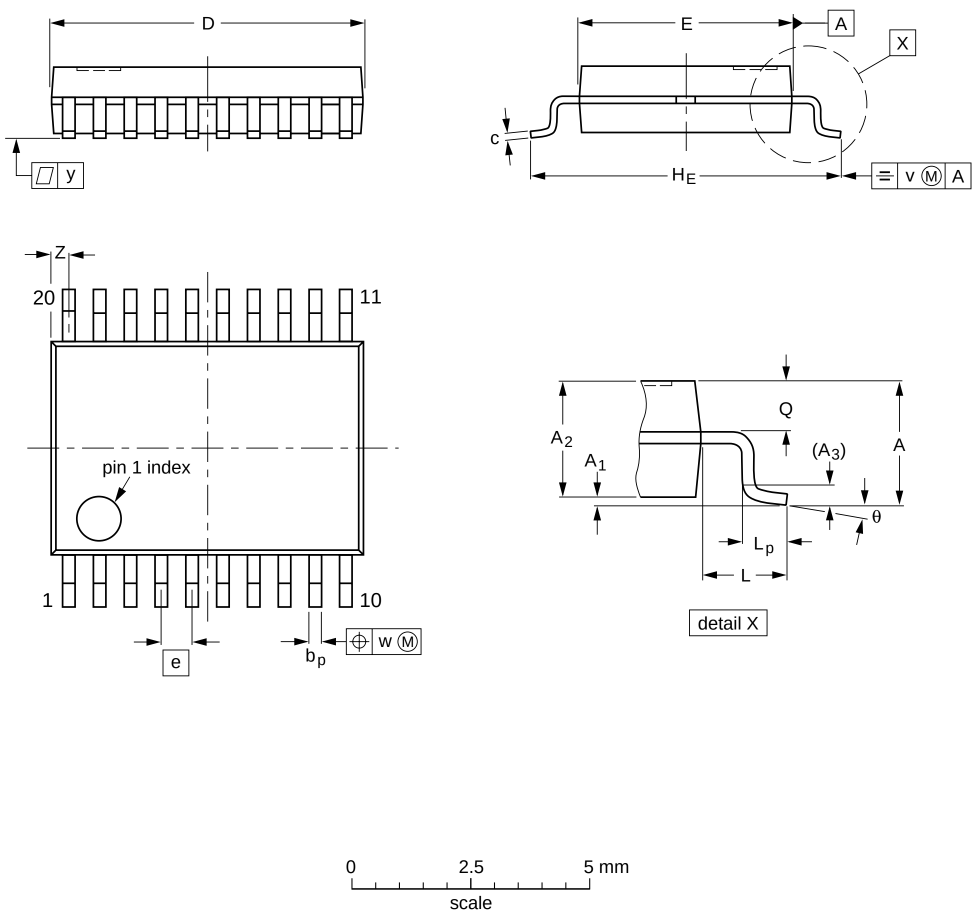
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 20. Package outline SOT338-1 (SSOP16)

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

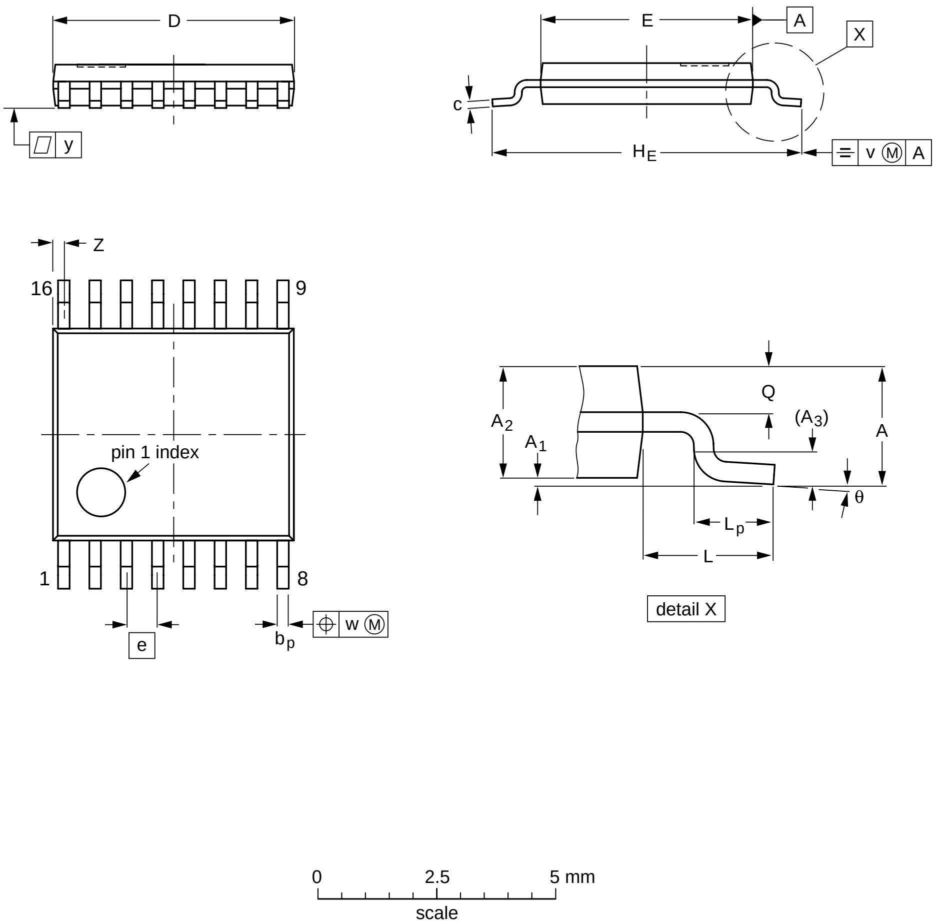
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT266-1		MO-152				~~99-12-27~~ 03-02-19

Fig 21. Package outline SOT266-1 (SSOP20)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

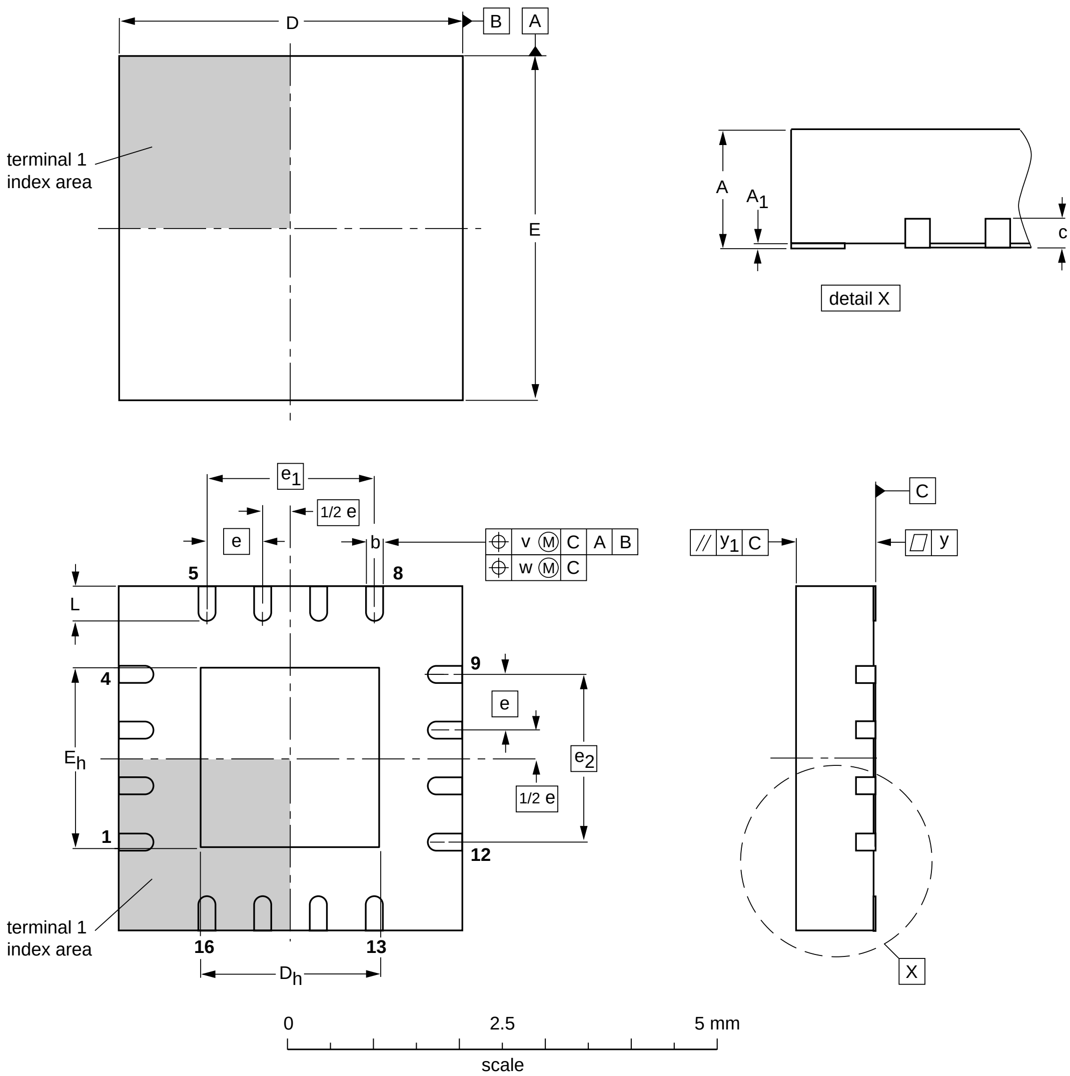
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 22. Package outline SOT403-1 (TSSOP16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.1	0.05	0.05	0.1

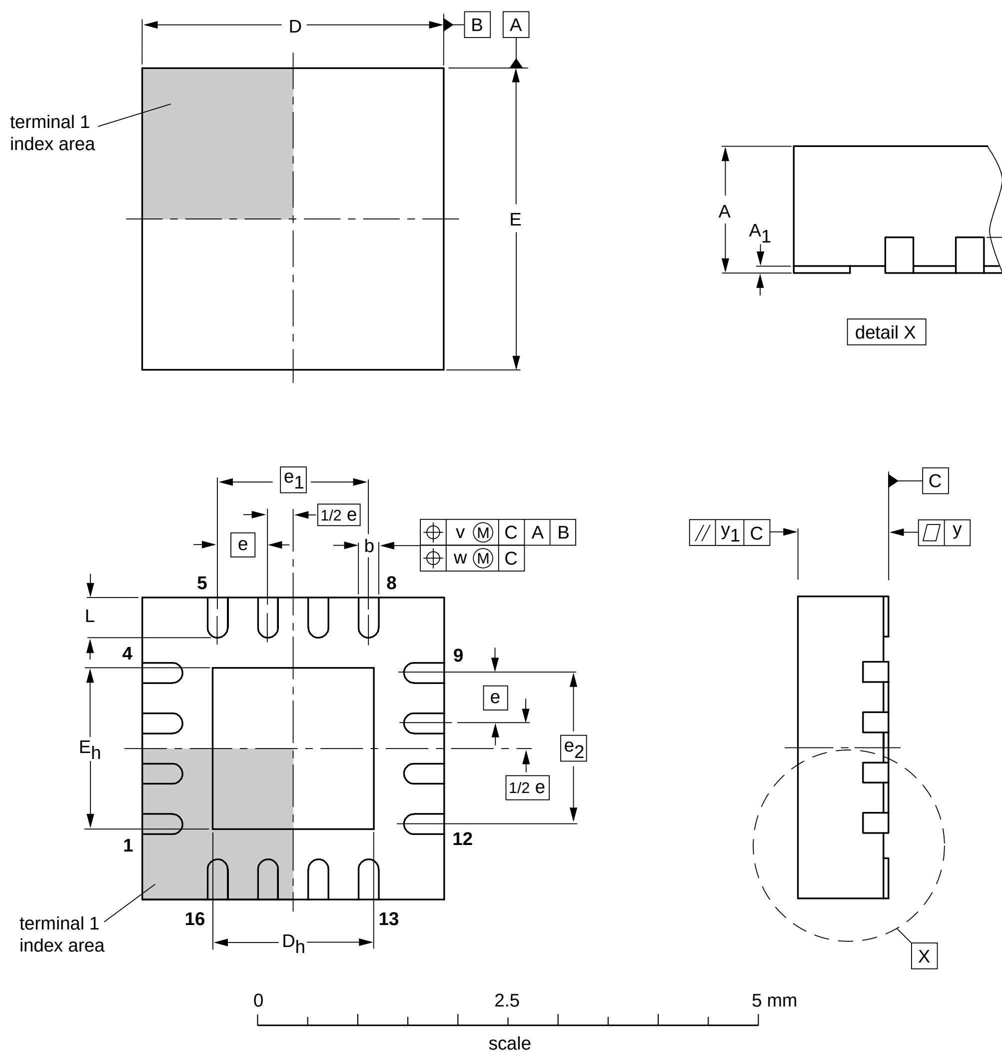
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 23. Package outline SOT629-1 (HVQFN16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Fig 24. Package outline SOT758-1 (HVQFN16)

12. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

13. Soldering

13.1 Introduction

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Through-hole mount packages

13.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

13.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

13.3 Surface mount packages

13.3.1 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the

packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020C)

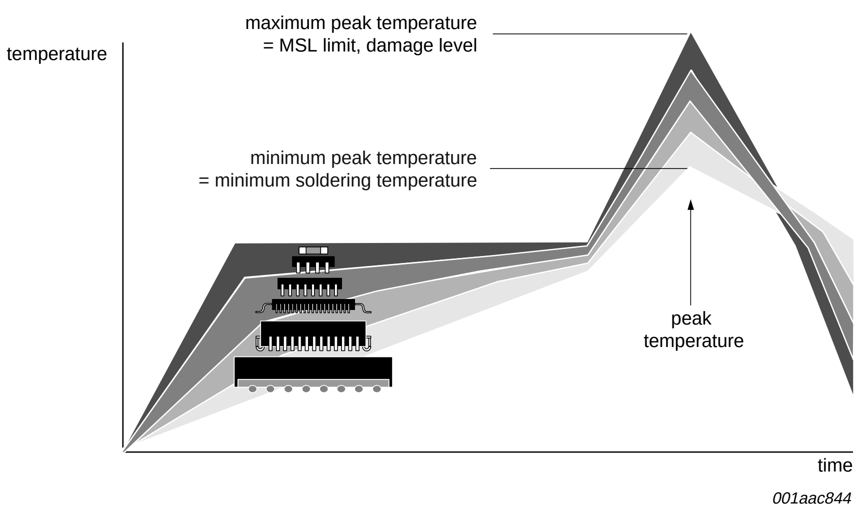
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.



MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

13.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.4 Package related soldering information

Table 13. Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package[1]	Soldering method		
		Wave	Reflow[2]	Dipping
Through-hole mount	CPGA, HCPGA	suitable	–	–
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable[3]	–	suitable
Through-hole-surface mount	PMFP[4]	not suitable	not suitable	–

Table 13. Suitability of IC packages for wave, reflow and dipping soldering methods *...continued*

Mounting	Package[1]	Soldering method		
		Wave	**Reflow[2]**	**Dipping**
Surface mount	BGA, HTSSON..T[5], LBGA, LFBGA, SQFP, SSOP..T[5], TFBGA, VFBGA, XSON	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[6]	suitable	–
	PLCC[7], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[7][8]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended[9]	suitable	–
	CWQCCN..L[10], WQCCN..L[10]	not suitable	not suitable	–

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your NXP Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect).

[3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[4] Hot bar soldering or manual soldering is suitable for PMFP packages.

[5] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[6] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[7] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[8] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[9] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[10] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

14. Abbreviations

Table 14. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
HBM	Human Body Model
I^{2}C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
MM	Machine Model
PCB	Printed-Circuit Board
POR	Power-On Reset
SMBus	System Management Bus

15. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9554_9554A_7	20061113	Product data sheet	-	PCA9554_9554A_6
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added HVQFN16 (SOT758-1) and bare die package offerings • Pin names I/O0 through I/O7 changed to IO0 through IO7 • Table 2 "Pin description": added Table note 1 and its reference at HVQFN pin 6 (V_{SS}) • Symbol (t_{pv} and t_{PV}) changed to $t_{v(Q)}$ • Symbol (t_{ph} and t_{PH}) changed to $t_{h(D)}$ • Symbol (t_{ps} and t_{PS}) changed to $t_{su(D)}$ • Symbol (t_{iv} and t_{IV}) changed to $t_{v(INT\_N)}$ • Symbol (t_{ir} and t_{IR}) changed to $t_{rst(INT\_N)}$ • Figure 16 "Typical application" modified (deleted "PCA9554A") • Table 8 "Limiting values": – Changed parameter description for symbol $V_{I/O}$ from "DC voltage on an I/O" to "voltage on an input/output pin" – Changed symbol "$I_{I/O}$, DC output current on an I/O" to "$I_{O(IOn)}$, output current on pin IOn" – Changed parameter description of I_{SS} from "supply current" to "ground supply current" • Table 9 "Static characteristics": – Symbols "I_{stbl}" and "I_{stbh}" replaced with "I_{stb}" • Added Section 14 "Abbreviations"			
PCA9554_9554A_6 (9397 750 13289)	20040930	Product data	-	PCA9554_9554A_5
PCA9554_9554A_5 (9397 750 10163)	20020726	Product data	853-2243 28672 of 26 July 2002	PCA9554_9554A_4
PCA9554_9554A_4 (9397 750 09817)	20020513	Product specification	-	PCA9554_9554A_3
PCA9554_9554A_3 (9397 750 08342)	20010507	Product specification	-	PCA9554_9554A_2
PCA9554_9554A_2 (9397 750 08209)	20010319	Product specification	-	PCA9554_9554A_1
PCA9554_9554A_1 (9397 750 08159)	20010319	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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