DATA SHEET

PCA9561

Quad 6-bit multiplexed
I²C EEPROM DIP switch

Product data sheet
Supersedes data of 2003 Jun 27

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Philips
Semiconductors

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Quad 6-bit multiplexed I²C EEPROM DIP switch PCA9561

FEATURES

- Selection of non-volatile register_n as source to MUX_OUT pins via I²C-bus
- I²C-bus can override MUX_SELECT pin in selecting output source
- 6-bit 5-to-1 multiplexer DIP switch
- 4 internal non-volatile registers
- Internal non-volatile registers programmable and readable via I²C-bus
- 6 open drain multiplexed outputs
- 400 kHz maximum clock frequency
- Operating supply voltage 3.0 V to 3.6 V
- 5 V and 2.5 V tolerant inputs/outputs
- Useful for Speed Step® configuration of laptop
- 2 address pins, allowing up to 4 devices on the I²C-bus
- MUX_IN values readable via I²C-bus
- ESD protection exceeds 200 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA.

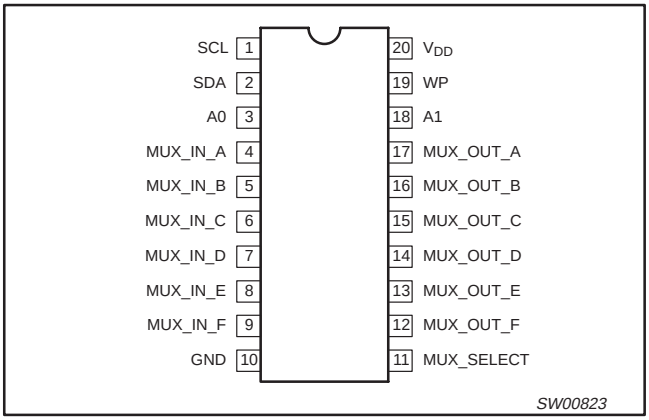
DESCRIPTION

The PCA9561 is a 20-pin CMOS device consisting of four 6-bit non-volatile EEPROM registers, 6 hardware pin inputs and a 6-bit multiplexed output. It is used for DIP switch-free or jumper-less system configuration and supports Mobile and Desktop VID Configuration, where 5 preset values (4 sets of internal non-volatile registers and 1 set of external hardware pins) set processor voltage for operation in various performance or battery conservation sleep modes. The PCA9561 is also useful in server and telecom/networking applications when used to replace DIP switches or jumpers, since the settings can be easily changed via I²C/SMBus without having to power down the equipment to open the cabinet. The non-volatile memory retains the most current setting selected before the power is turned off.

The PCA9561 typically resides between the CPU and Voltage Regulator Module (VRM) when used for CPU VID (Voltage IDentification code) configuration. It is used to bypass the CPU-defined VID values and provide a different set of VID values to the VRM, if an increase in the CPU voltage is desired. An increase in CPU voltage combined with an increase in CPU frequency leads to a performance boost of up to 7.5%. Lower CPU voltage reduces power consumption. The main advantage of the PCA9561 over older devices, such as the PCA9559 or PCA9560, is that it contains four internal non-volatile EEPROM registers instead of just one or two, allowing five independent settings which allows a more accurate CPU voltage tuning depending on specific applications.

The PCA9561 has 2 address pins, allowing up to 4 devices to be placed on the same I²C-bus or SMBus.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
1	I²C SCL	Serial I²C-bus clock
2	I²C SDA	Serial bi-directional I²C-bus data
3	A0	A0 address
4–9	MUX_IN_A–F	External inputs to multiplexer
10	GND	Ground
11	MUX_SELECT	Selects MUX_IN inputs or register contents for MUX_OUT outputs
12–17	MUX_OUT_F–A	Open drain multiplexed outputs
18	A1	A1 address
19	WP	Non-volatile register write-protect
20	V_{DD}	Power supply: +3.0 to +3.6 V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
20-Pin Plastic SO	–40 to +85 °C	PCA9561D	PCA9561D	SOT163-1
20-Pin Plastic TSSOP	–40 to +85 °C	PCA9561PW	PCA9561	SOT360-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

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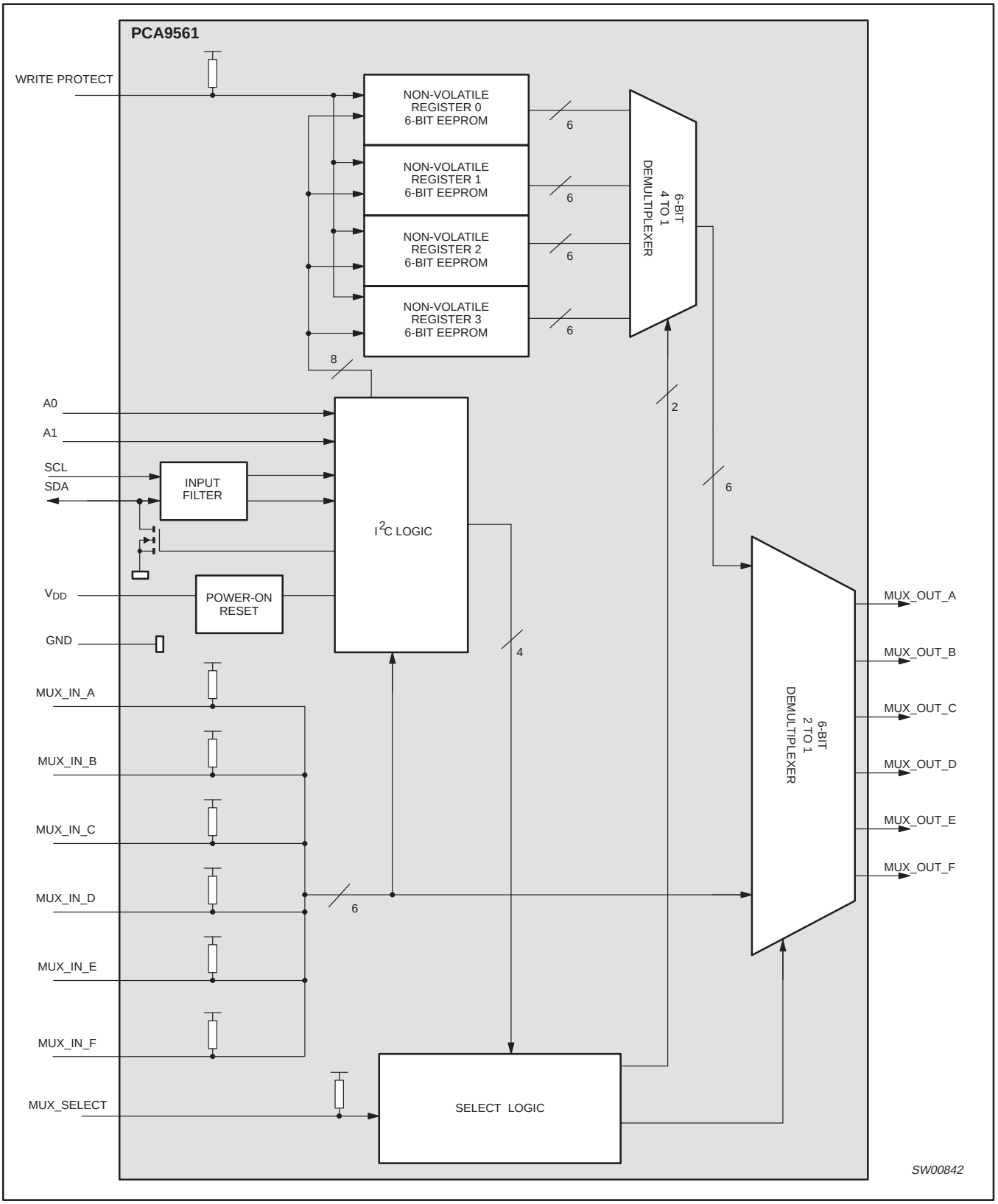
BLOCK DIAGRAM



DEVICE ADDRESS

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9561 is shown in Figure 1. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

The last bit of the slave address byte defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

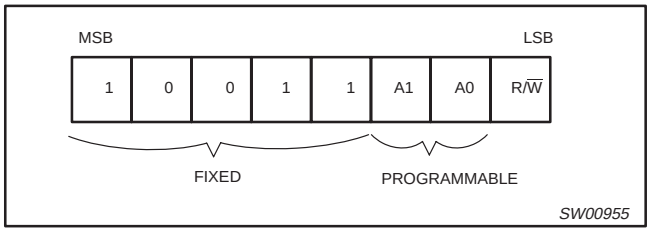


Figure 1. Slave address

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9561, which will be stored in the control register. This register can be written and read via the I²C-bus.

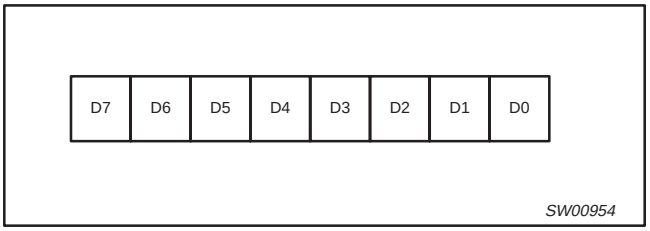


Figure 2. Control Register

CONTROL REGISTER DEFINITION

Following the address and acknowledge bit with logic 0 in the read/write bit, the first byte written is the command byte. If the command byte is reserved and therefore not valid, it will not be acknowledged. Only valid command bytes will be acknowledged.

Table 1. Register Addresses

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NAME	TYPE	REGISTER FUNCTION
0	0	0	0	0	0	0	0	EEPROM 0	Read/Write	EEPROM byte 0 register
0	0	0	0	0	0	0	1	EEPROM 1	Read/Write	EEPROM byte 1 register
0	0	0	0	0	0	1	0	EEPROM 2	Read/Write	EEPROM byte 2 register
0	0	0	0	0	0	1	1	EEPROM 3	Read/Write	EEPROM byte 3 register
1	1	1	1	1	1	1	1	MUX_IN	Read	MUX_IN values register

Table 2. Commands

D7	D6	D5	D4	D3	D2	D1	D0	COMMAND
1	1	1	1	1	0	0	0	MUX_OUT from EEPROM byte 0
1	1	1	1	1	1	0	0	MUX_OUT from EEPROM byte 1
1	1	1	1	1	0	X	1	MUX_OUT from EEPROM byte 2
1	1	1	1	1	1	X	1	MUX_OUT from EEPROM byte 3
1	1	1	1	1	X	1	0	MUX_OUT from MUX_IN
1	1	1	1	1	X	X	1	MUX_OUT from MUX_SELECT[2]

NOTE:
1. All other combinations are reserved.
2. MUX_SELECT pins select between MUX_IN and EEPROM to MUX_OUT.

REGISTER DESCRIPTION

If the command byte is an EEPROM address, the next byte sent will be programmed into that EEPROM address on the following STOP condition, if the WP is logic 0. If more than one byte is sent sequentially, the second byte will be written in the other-volatile register, on the following STOP condition. Up to four bytes can be sent sequentially. If any more data bytes are sent after the second byte, they will not be acknowledged and no bytes will be written to the non-volatile registers. After a byte is read from or written to the EEPROM, the part automatically points to the next non-volatile register. If the command code was FFH, the MUX_IN values are sent with the three MSBs padded with zeroes as shown below. If the command codes was 00H, then the non-volatile register 1 is sent, and if the command code was 01H, then the non-volatile register 1 is sent.

EEPROM Byte 0 Register

	D7	D6	D5	D4	D3	D2	D1	D0
Write	X	X	EEPROM 0 Data F	EEPROM 0 Data E	EEPROM 0 Data D	EEPROM 0 Data C	EEPROM 0 Data B	EEPROM 0 Data A
Read	0	0	EEPROM 0 Data F	EEPROM 0 Data E	EEPROM 0 Data D	EEPROM 0 Data C	EEPROM 0 Data B	EEPROM 0 Data A
Default	0	0	0	0	0	0	0	0

EEPROM Byte 1 Register

	D7	D6	D5	D4	D3	D2	D1	D0
Write	X	X	EEPROM 1 Data F	EEPROM 1 Data E	EEPROM 1 Data D	EEPROM 1 Data C	EEPROM 1 Data B	EEPROM 1 Data A
Read	0	0	EEPROM 1 Data F	EEPROM 1 Data E	EEPROM 1 Data D	EEPROM 1 Data C	EEPROM 1 Data B	EEPROM 1 Data A
Default	0	0	0	0	0	0	0	0

EEPROM Byte 2 Register

	D7	D6	D5	D4	D3	D2	D1	D0
Write	X	X	EEPROM 2 Data F	EEPROM 2 Data E	EEPROM 2 Data D	EEPROM 2 Data C	EEPROM 2 Data B	EEPROM 2 Data A
Read	0	0	EEPROM 2 Data F	EEPROM 2 Data E	EEPROM 2 Data D	EEPROM 2 Data C	EEPROM 2 Data B	EEPROM 2 Data A
Default	0	0	0	0	0	0	0	0

EEPROM Byte 3 Register

	D7	D6	D5	D4	D3	D2	D1	D0
Write	X	X	EEPROM 3 Data F	EEPROM 3 Data E	EEPROM 3 Data D	EEPROM 3 Data C	EEPROM 3 Data B	EEPROM 3 Data A
Read	0	0	EEPROM 3 Data F	EEPROM 3 Data E	EEPROM 3 Data D	EEPROM 3 Data C	EEPROM 3 Data B	EEPROM 3 Data A
Default	0	0	0	0	0	0	0	0

MUX_IN Register

	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	MUX_IN Data F	MUX_IN Data E	MUX_IN Data D	MUX_IN Data C	MUX_IN Data B	MUX_IN Data A

If the command byte is a MUX command byte, any additional data bytes sent after the MUX command code will not be acknowledged. If the read/write bit in the address is a logic 1, then a read operation follows and the data sent out depends on the previously stored command code.

The MUX_SELECT_1 pin can function as the over-ride pin as on the PCA9559 if the non-volatile register 1 is left at all 0s.

The NON_MUXED_OUT pin is a latched output. It is latched when MUX_SELECT_0 = 1. It is transparent when the MUX_SELECT_0 = 0. The data sent out on the NON_MUXED_OUT output is the 6th most significant bit of the non-volatile register. Whether this comes from the non-volatile register 0 or non-volatile register 1 depends on the command code or the external mux-select pins.

After a valid I²C write operation to the EEPROM, the part cannot be addressed via the I²C for 3.6 ms. If the part is addressed prior to this time, the part will not acknowledge its address.

NOTE:
1. To ensure data integrity, the non-volatile register must be internally write protected when V_{DD} to the I²C-bus is powered down or V_{DD} to the component is dropped below normal operating levels.

EXTERNAL CONTROL SIGNALS

The Write Protect (WP) input is used to control the ability to write the content of the non-volatile registers. If the WP signal is logic 0, the I²C-bus will be able to write the contents of the non-volatile registers. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile registers. In this case, the slave address and the command code will be acknowledged but the following data bytes will not be acknowledged and the EEPROM is not updated.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I²C-bus (described in the next section).

The WP, MUX_IN*, and MUX_SELECT signals have internal pull-up resistors. See the DC and AC Characteristics for hysteresis and signal spike suppression figures.

Function Table[1]

WP	MUX_SELECT	COMMANDS
0	X	Write to the non-volatile registers through I²C-bus allowed
1	X	Write to the non-volatile registers through I²C-bus not allowed
X	0	MUX_OUT from EEPROM byte 0–3 (EEPROM selected through I²C – see Table 2)
X	1	MUX_OUT from MUX_IN inputs

NOTE:
1. This table is valid when not overridden by I²C control register.

POWER-ON RESET (POR)

When power is applied to V_{DD}, an internal power-on reset holds the PCA9561 in a reset state until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9561 volatile registers and state machine will initialize to their default states.

The MUX_OUT pin values depend on the MUX_SELECT logic level:

- if MUX_SELECT = 0, the MUX_OUT pin output values will equal the previously stored EEPROM byte 0 values regardless of the last non-volative EEPROM byte selected by the command byte prior to power down.
- if MUX_SELECT = 1, the MUX_OUT output values will equal the MUX_IN pin input values as shown in the Function Table.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 3).

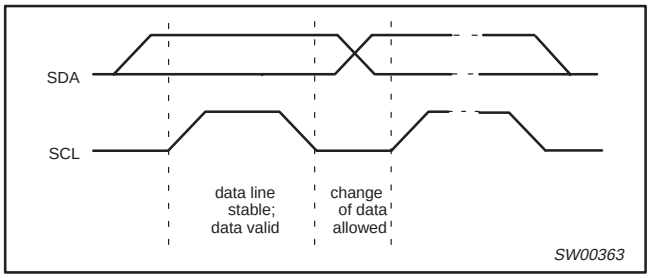


Figure 3. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 4).

System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device initiates a transfer is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 5).

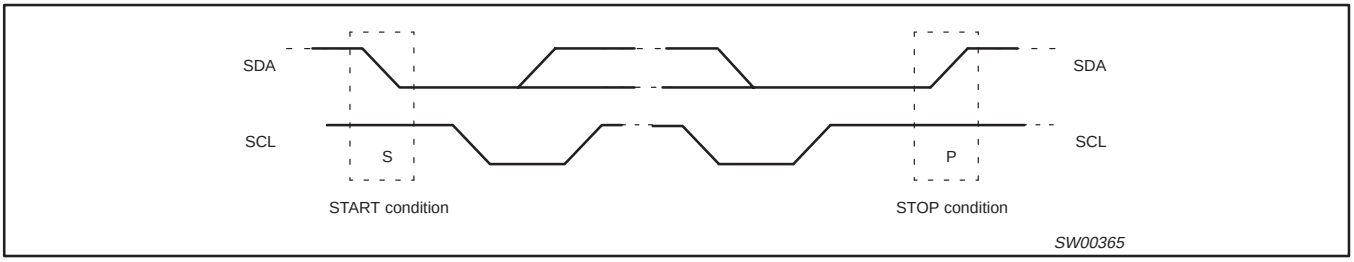


Figure 4. Definition of start and stop conditions

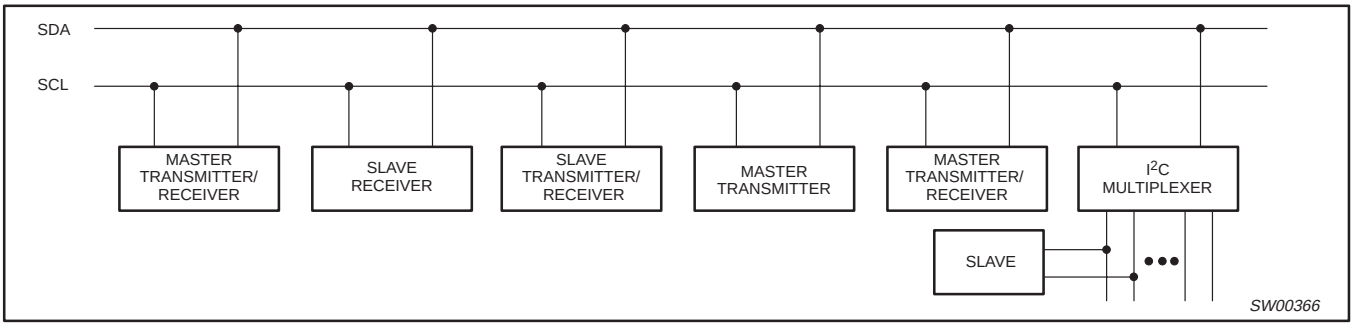


Figure 5. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

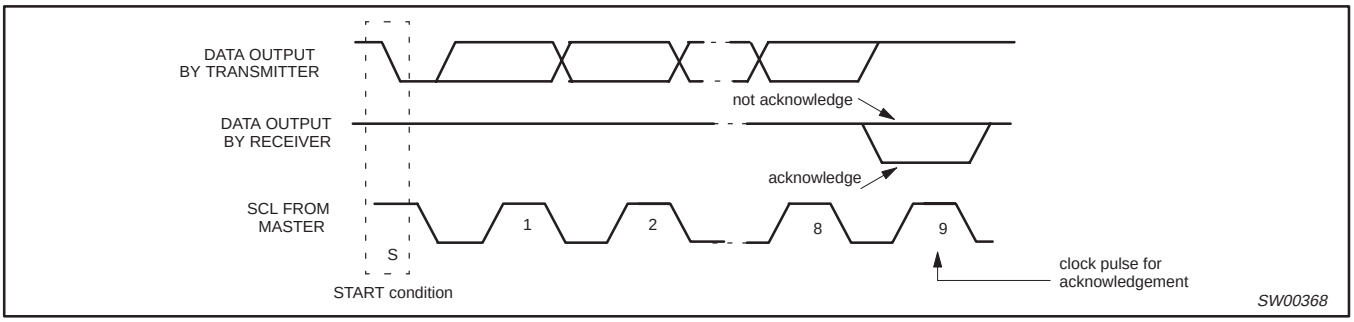


Figure 6. Acknowledgement on the I2C-bus

Bus Transactions

Data is transmitted to the PCA9561 registers using Write Byte transfers (see Figures 7 and 8). Data is read from the PCA9561 registers using Read and Receive Byte transfers (see Figure 9).

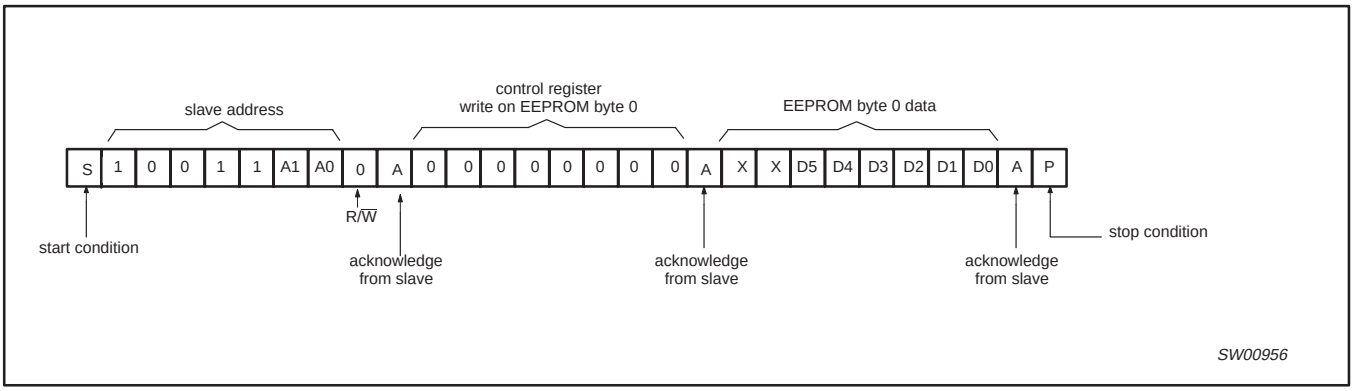


Figure 7. WRITE on 1 EEPROM — assuming WP = 0

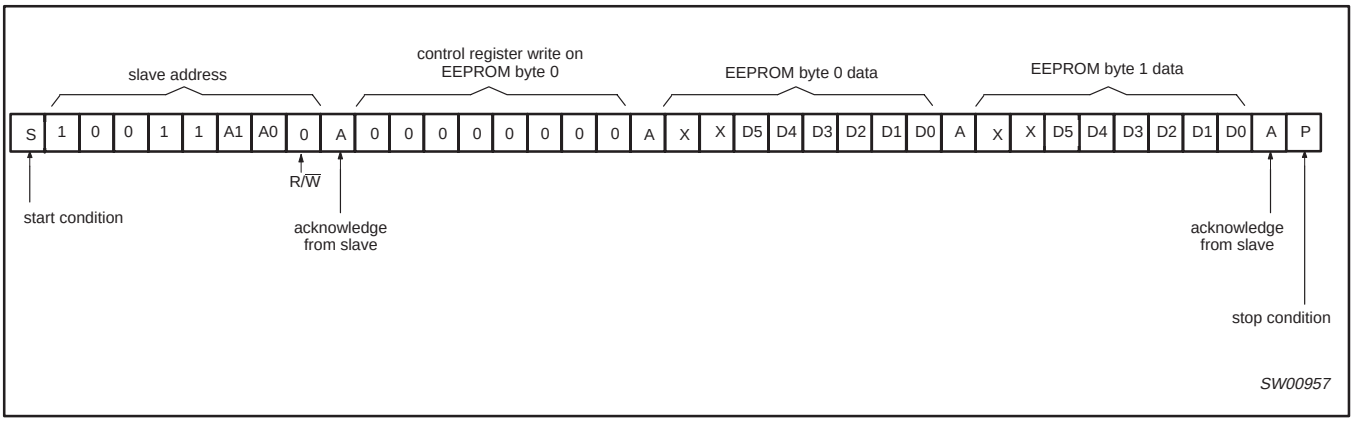


Figure 8. WRITE on 2 EEPROMs — assuming WP = 0

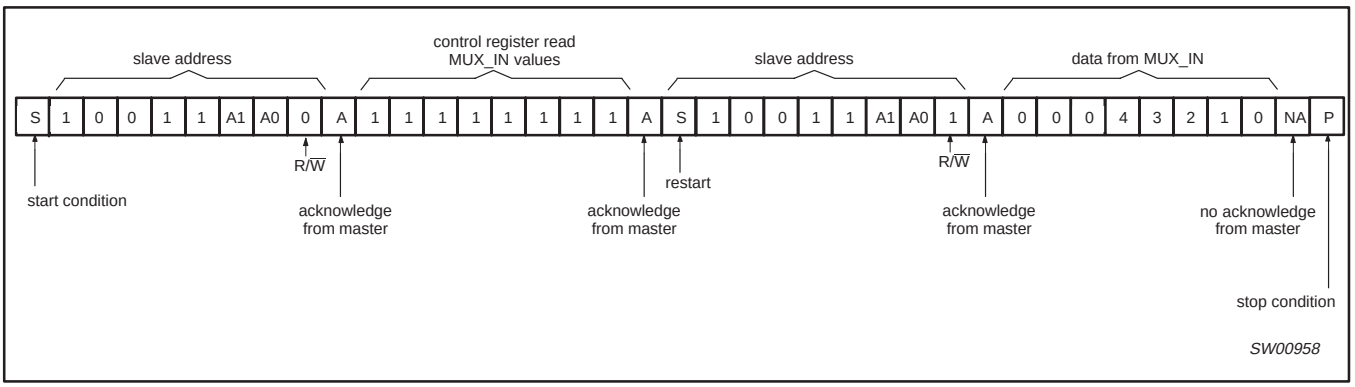


Figure 9. READ MUX_IN register

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{DD}	DC supply voltage		–0.5 to +4.0	V
V_I	DC input voltage	Note 3	–1.5 to +5.5	V
V_{OUT}	DC output voltage	Note 3	–0.5 to +5.5	V
T_{stg}	Storage temperature range		–60 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The maximum input or output voltage is the lesser of 5.5 V or V_{DD} + 4.0 V, except for very short (e.g., system start-up or shut-down) durations.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		CONDITIONS	LIMITS		UNIT
				MIN	MAX	
V_{DD}	DC supply voltage		—	3.0	3.6	V
V_{IL}	LOW-level input voltage	SCL, SDA	I_{OL}= 3 mA	–0.5	0.9	V
V_{IH}	HIGH-level input voltage	SCL, SDA	I_{OL}= 3 mA	2.7	5.5 [1]	V
V_{OL}	LOW-level output voltage	SCL, SDA	I_{OL}= 3 mA	—	0.4	V
			I_{OL}= 6 mA	—	0.6	V
V_{IL}	LOW-level input voltage	MUX_IN, MUX_SELECT_0 MUX_SELECT_1	—	–0.5	0.8	V
V_{IH}	HIGH-level input voltage	MUX_IN, MUX_SELECT_0 MUX_SELECT_1	—	2.0	5.5 [1]	V
I_{OL}	LOW-level output current	MUX_OUT	—	—	8	mA
I_{OH}	HIGH-level output current	MUX_OUT	—	—	100	μA
dt/dv	Input transition rise or fall time		—	0	10	ns/V
T_{amb}	Operating temperature		—	–40	85	°C

NOTES:
1. The maximum input voltage is the lesser of 5.5 V or V_{DD} + 4.0 V, except for very short (e.g., system start-up or shut-down) durations.

DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Supply						
V_{DD}	Supply voltage		3	—	3.6	V
I_{DDL}	Supply current	Operating mode ALL inputs = 0 V	—	0.6	1	mA
I_{DDH}	Supply current	Operating mode ALL inputs = V_{DD}	—	—	600	µA
V_{POR}	Power-on reset voltage	no load; $V_I = V_{DD}$ or GND	—	2.3	2.7	V
Input SCL; Input/Output SDA						
V_{IL}	LOW-level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2	—	5.5 [1]	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
I_{OL}	LOW-level output current	V_{OL} = 0.6 V	6	—	—	mA
I_{IH}	Leakage current HIGH	$V_I = V_{DD}$	–1	—	1	µA
I_{IL}	Leakage current LOW	V_I = GND	–1	—	1	µA
C_I	Input capacitance		—	3	6	pF
WP and MUX_SELECT						
I_{IH}	Leakage current HIGH	$V_I = V_{DD}$	–1	—	1	µA
I_{IL}	Input current LOW	V_{DD} = 3.6 V; V_I = GND	–20	—	–50	µA
C_I	Input capacitance		—	2.5	5	pF
Mux A → F						
I_{IH}	Leakage current HIGH	$V_I = V_{DD}$	–1	—	1	µA
I_{IL}	Input current LOW	V_{DD} = 3.6 V; V_I = GND	–20	—	–50	µA
C_I	Input capacitance		—	2.5	5	pF
A0 and A1 Inputs						
I_{IH}	Leakage current HIGH	$V_I = V_{DD}$	–1	—	1	µA
I_{IL}	Input current LOW	V_{DD} = 3.6 V; V_I = GND	–20	—	–50	µA
C_I	Input capacitance		—	2	4	pF
MUX_OUT						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	—	—	0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	—	—	0.7	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$	—	—	100	µA

NOTE:
1. The maximum input voltage is the lesser of 5.5 V or V_{DD} + 4.0 V, except for very short (e.g., system start-up or shut-down) durations.

NON-VOLATILE STORAGE SPECIFICATIONS

PARAMETER	SPECIFICATION
Memory cell data retention	10 years min
Number of memory cell write cycles	100,000 cycles min

Application Note *AN250 I²C DIP Switch* provides additional information on memory cell data retention and the minimum number of write cycles.

AC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
MUX_IN ⇒ MUX_OUT					
t_{PLH}	LOW-to-HIGH transition time	—	28	40	ns
t_{PHL}	HIGH-to-LOW transition time	—	8	15	ns
Select ⇒ MUX_OUT					
t_{PLH}	LOW-to-HIGH transition time	—	30	43	ns
t_{PHL}	HIGH-to-LOW transition time	—	10	15	ns
t_R	Output rise time	1.0	—	3	ns/V
t_F	Output fall time	1.0	—	3	ns/V
C_L	Test load capacitance on outputs	—	—	—	pF

SYMBOL	PARAMETER	STANDARD-MODE I²C-BUS		FAST-MODE I²C-BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	—	0.6	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
$t_{HD;DAT}$	Data hold time	0[1]	3.45	0[1]	0.9	µs
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	$20 + 0.1C_b$[2]	300	ns
t_f	Fall time of both SDA and SCL signals	—	300	$20 + 0.1C_b$[2]	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	—	0.6	—	µs
C_b	Capacitive load for each bus line	—	400	—	400	pF
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	—	50	—	50	ns

NOTES:
1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
2. C_b = total capacitance of one bus line in pF.

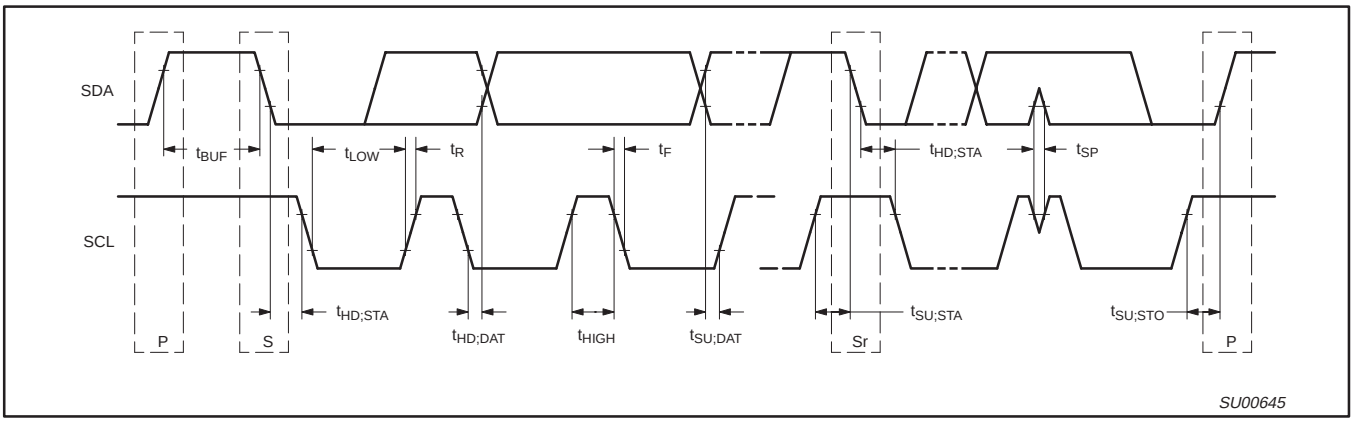


Figure 10. Definition of timing

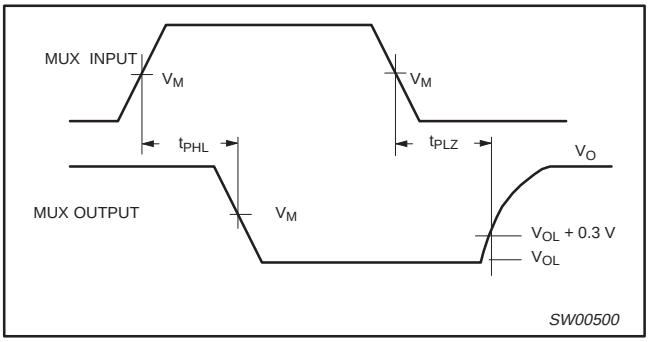


Figure 11. Open drain output enable and disable times

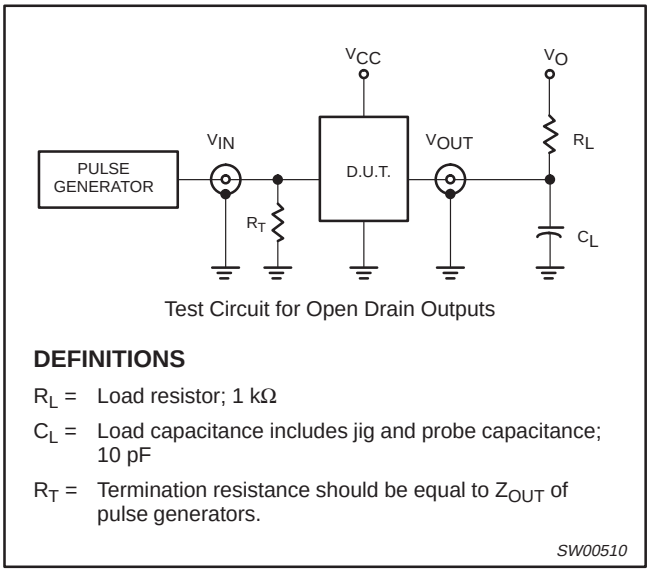
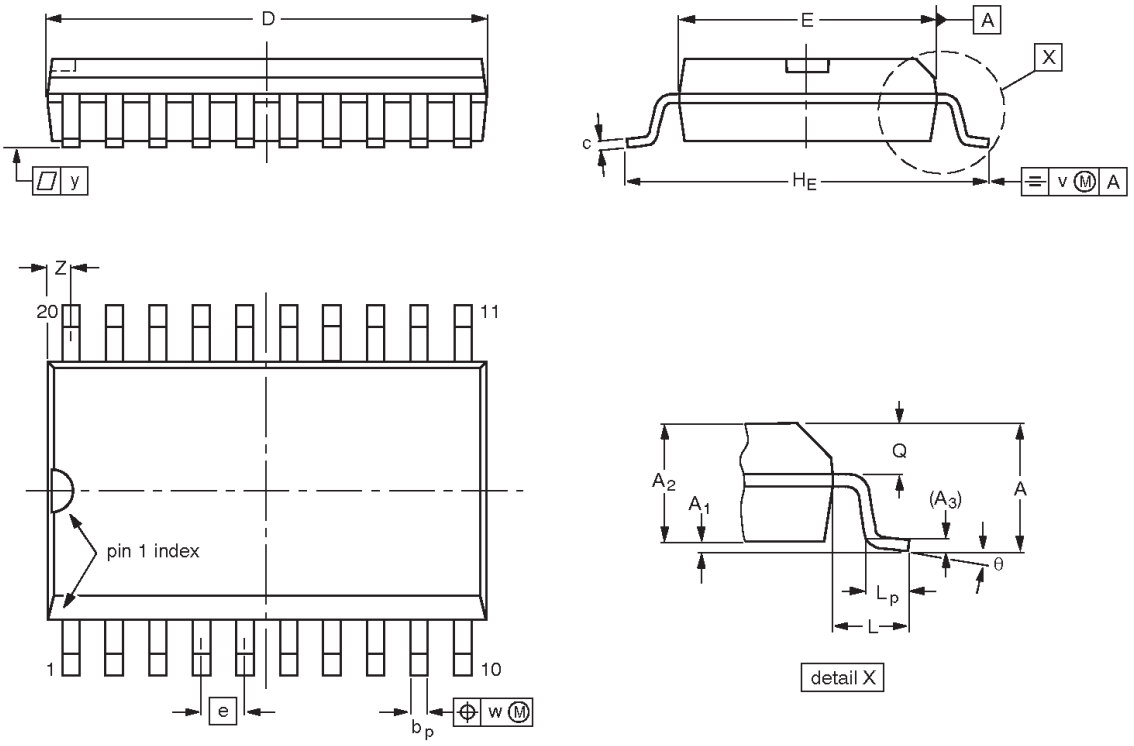
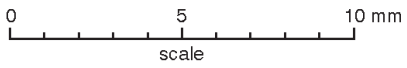


Figure 12. Test circuit

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

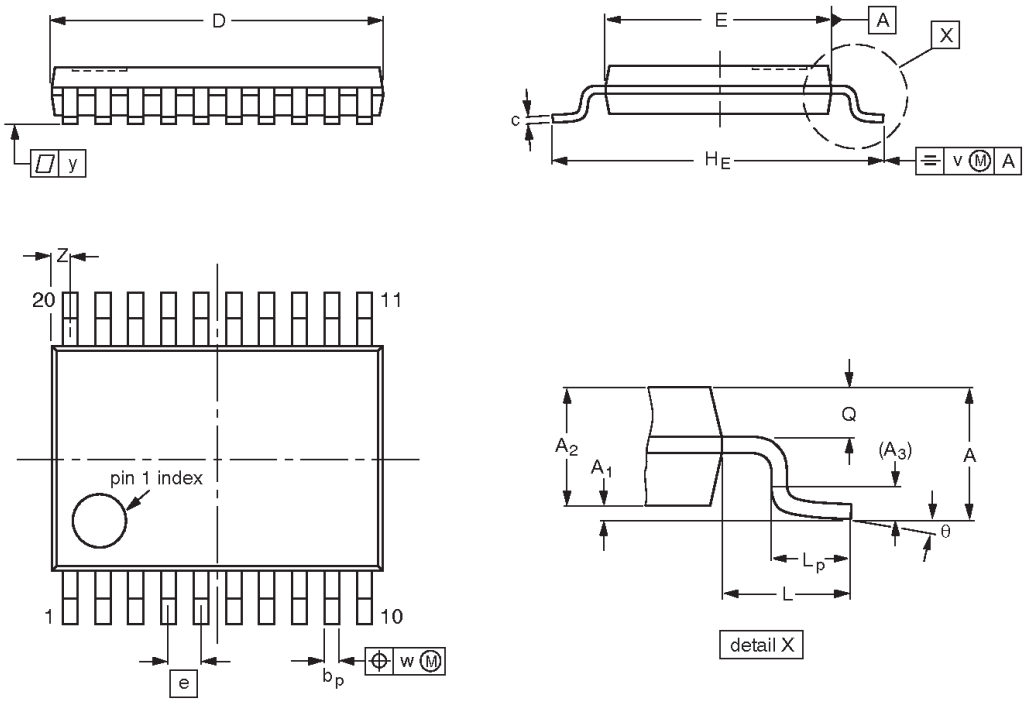
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

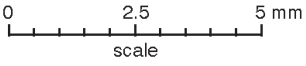
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_3	20040517	**Product data (9397 750 13153). Supersedes data of 2003 Jun 27 (9397 750 11677).** Modifications: ● Features section, 9th bullet: from “inputs” to “inputs/outputs” ● Absolute maximum ratings table: V_{DD}, V_{IN}, and V_{OUT} limits modified. Note 3 re-written. ● Recommended operating conditions – V_{IH} max. (on SCL, SDA) changed from 4.0 V to 5.5 V (with Note 1 added). – V_{IH} max. (on MUX_IN, MUX_SELECT_0, MUX_SELECT_1) changed from 4.0 V to 5.5 V (with Note 1 added). ● DC characteristics table – Input SCL: Input/Output SDA; V_{IH} parameter max. limit modified, and Note 1 added. – Mux A → F: Symbols I_{IH} and I_{IL} : change the Unit from ‘mA’ to ‘μA’.
_2	20030627	**Product data (9397 750 11677); ECN 853-2348 29936 dated 19 May 2003. Supersedes data of 2002 May 24 (9397 750 09888).**
_1	20020524	**Product data (9397 750 09888); ECN 853-2348 28311 of 24 May 2002.**

Quad 6-bit multiplexed I²C EEPROM DIP switch PCA9561

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Date of release: 05-04

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