



PCA9674/74A

Remote 8-bit I/O expander for Fm+ I²C-bus with interrupt

Rev. 05 — 15 June 2009

Product data sheet

1. General description

The PCA9674/74A provide general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C-bus) and is a part of the Fast-mode Plus (Fm+) family.

The PCA9674/74A is a drop-in upgrade for the PCF8574/74A providing higher Fast-mode Plus I²C-bus speeds (1 MHz versus 400 kHz) so that the output can support PWM dimming of LEDs, higher I²C-bus drive (30 mA versus 3 mA) so that many more devices can be on the bus without the need for bus buffers, higher total package sink capacity (200 mA versus 100 mA) that supports having all LEDs on at the same time and more device addresses (64 versus 8) are available to allow many more devices on the bus without address conflicts.

The devices consist of an 8-bit quasi-bidirectional port and an I²C-bus interface. The PCA9674/74A have low current consumption and include latched outputs with 25 mA high current drive capability for directly driving LEDs.

They also possess an interrupt line ($\overline{\text{INT}}$) that can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus.

The internal Power-On Reset (POR) or Software Reset sequence initializes the I/Os as inputs.

2. Features

- 1 MHz I²C-bus interface
- Compliant with the I²C-bus Fast and Standard modes
- SDA with 30 mA sink capability for 4000 pF buses
- 2.3 V to 5.5 V operation with 5.5 V tolerant I/Os
- 8-bit remote I/O pins that default to inputs at power-up
- Latched outputs with 25 mA sink capability for directly driving LEDs
- Total package sink capability of 200 mA
- Active LOW open-drain interrupt output
- 64 programmable slave addresses using 3 address pins
- Readable device ID (manufacturer, device type, and revision)
- Low standby current
- -40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101

- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA
- Packages offered: SO16, SSOP20, TSSOP16, HVQFN16

3. Applications

- LED signs and displays
- Servers
- Industrial control
- Medical equipment
- PLCs
- Cellular telephones
- Gaming machines
- Instrumentation and test measurement

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9674BS	674	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA9674ABS	74A			
PCA9674D	PCA9674D	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA9674AD	PCA9674AD			
PCA9674PW	PCA9674	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9674APW	PA9674A			
PCA9674TS	PCA9674	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1
PCA9674ATS	PA9674A			

5. Block diagram

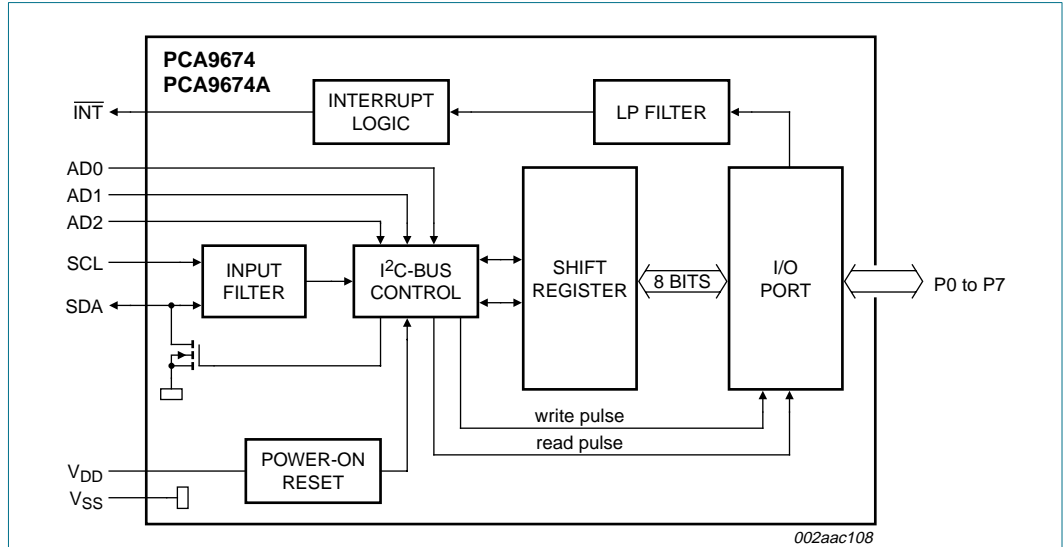


Fig 1. Block diagram of PCA9674/74A

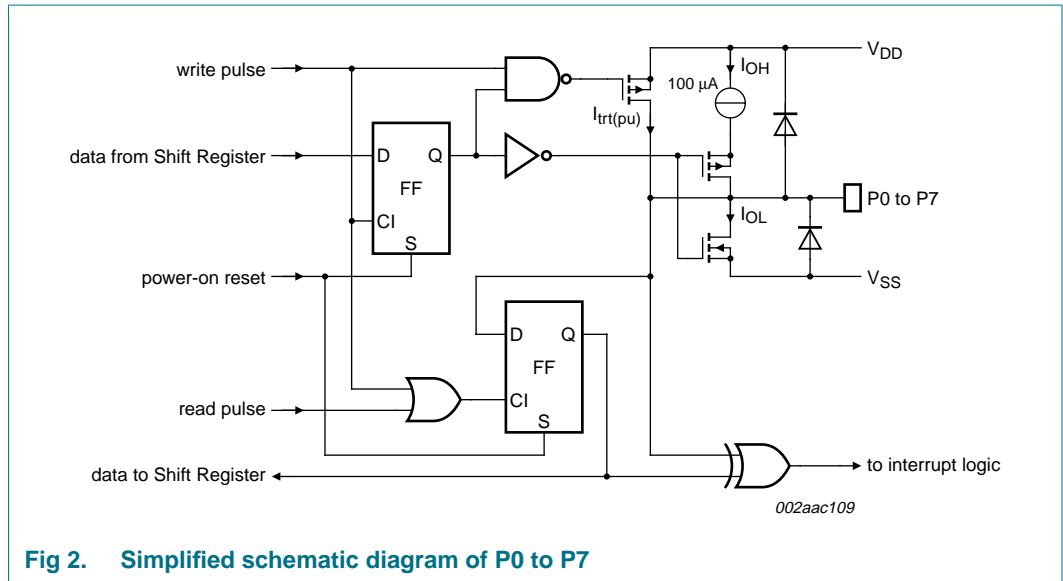
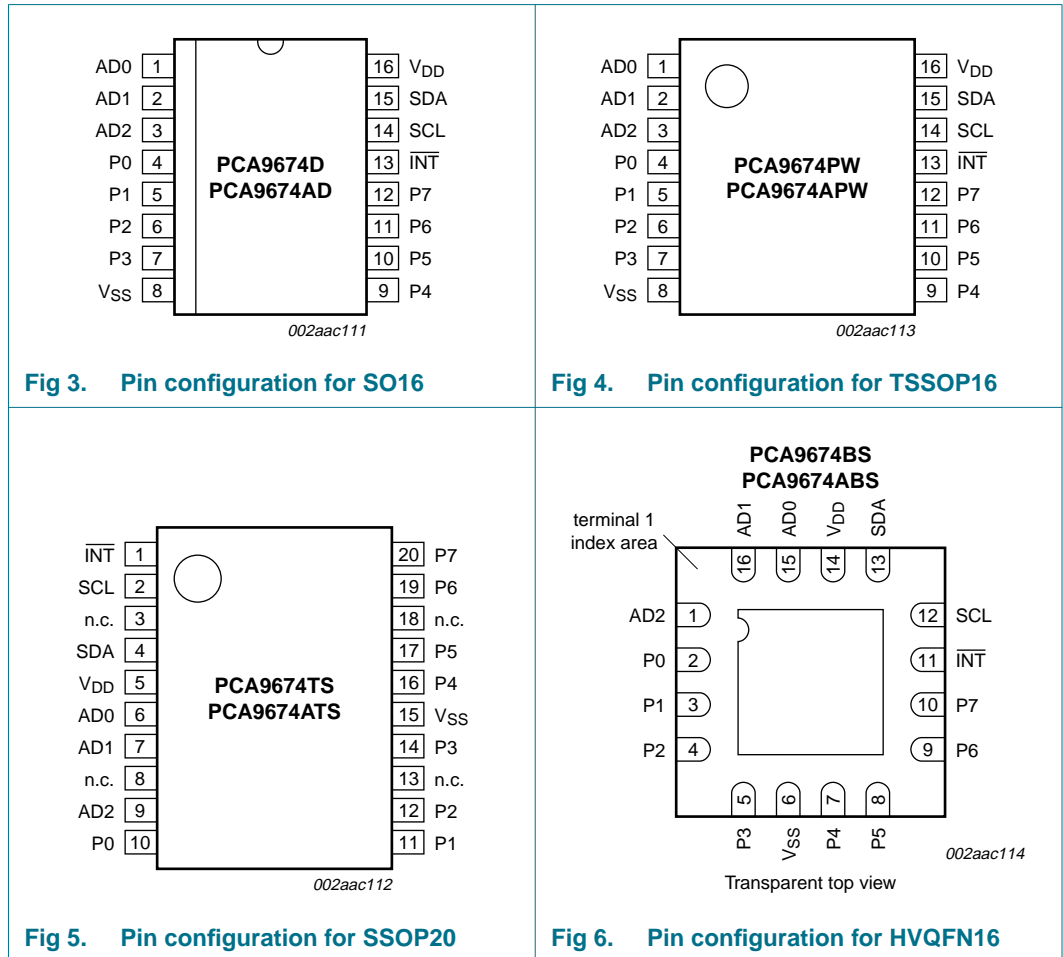


Fig 2. Simplified schematic diagram of P0 to P7

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description for SO16, TSSOP16

Symbol	Pin	Description
AD0	1	address input 0
AD1	2	address input 1
AD2	3	address input 2
P0	4	quasi-bidirectional I/O 0
P1	5	quasi-bidirectional I/O 1
P2	6	quasi-bidirectional I/O 2
P3	7	quasi-bidirectional I/O 3
V _{SS}	8	supply ground
P4	9	quasi-bidirectional I/O 4
P5	10	quasi-bidirectional I/O 5
P6	11	quasi-bidirectional I/O 6
P7	12	quasi-bidirectional I/O 7
$\overline{\text{INT}}$	13	interrupt output (active LOW)
SCL	14	serial clock line
SDA	15	serial data line
V _{DD}	16	supply voltage

Table 3. Pin description for SSOP20

Symbol	Pin	Description
$\overline{\text{INT}}$	1	interrupt output (active LOW)
SCL	2	serial clock line
n.c.	3	not connected
SDA	4	serial data line
V _{DD}	5	supply voltage
AD0	6	address input 0
AD1	7	address input 1
n.c.	8	not connected
AD2	9	address input 2
P0	10	quasi-bidirectional I/O 0
P1	11	quasi-bidirectional I/O 1
P2	12	quasi-bidirectional I/O 2
n.c.	13	not connected
P3	14	quasi-bidirectional I/O 3
V _{SS}	15	supply ground
P4	16	quasi-bidirectional I/O 4
P5	17	quasi-bidirectional I/O 5
n.c.	18	not connected
P6	19	quasi-bidirectional I/O 6
P7	20	quasi-bidirectional I/O 7

Table 4. Pin description for HVQFN16

Symbol	Pin	Description
AD2	1	address input 2
P0	2	quasi-bidirectional I/O 0
P1	3	quasi-bidirectional I/O 1
P2	4	quasi-bidirectional I/O 2
P3	5	quasi-bidirectional I/O 3
V _{SS} ^[1]	6	supply ground
P4	7	quasi-bidirectional I/O 4
P5	8	quasi-bidirectional I/O 5
P6	9	quasi-bidirectional I/O 6
P7	10	quasi-bidirectional I/O 7
INT	11	interrupt output (active LOW)
SCL	12	serial clock line
SDA	13	serial data line
V _{DD}	14	supply voltage
AD0	15	address input 0
AD1	16	address input 1

[1] HVQFN16 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to [Figure 1 “Block diagram of PCA9674/74A”](#).

7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA9674/74A is shown in [Figure 7](#). Slave address pins AD2, AD1, and AD0 choose 1 of 64 slave addresses. To conserve power, no internal pull-up resistors are incorporated on AD2, AD1, and AD0. Address values depending on AD2, AD1, and AD0 can be found in [Table 5 “PCA9674 address map”](#) and [Table 6 “PCA9674A address map”](#).

Remark: When using the PCA9674A, the General Call address (0000 0000b) and the Device ID address (1111 100Xb) are reserved and cannot be used as device address. Failure to follow this requirement will cause the PCA9674A not to acknowledge.

Remark: When using the PCA9674 or the PCA9674A, reserved I²C-bus addresses must be used with caution since they can interfere with:

- “reserved for future use” I²C-bus addresses (0000 011, 1111 101, 1111 110, 1111 111)
- slave devices that use the 10-bit addressing scheme (1111 0xx)
- High speed mode (Hs-mode) master code (0000 1xx)

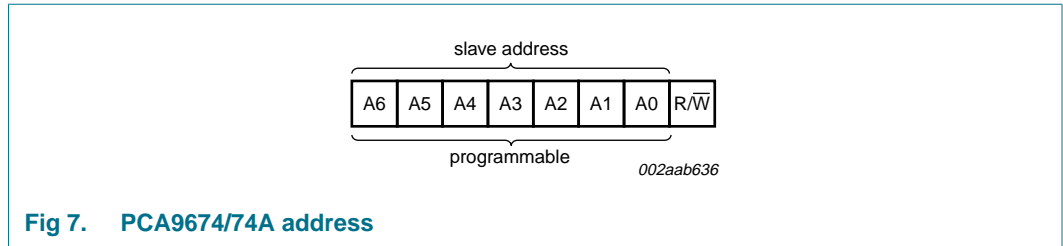


Fig 7. PCA9674/74A address

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

When AD2, AD1 and AD0 are held to V_{DD} or V_{SS}, the same address as the PCF8574 or PCF8574A is applied.

7.1.1 Address maps

Table 5. PCA9674 address map

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address
V _{SS}	SCL	V _{SS}	0	0	1	0	0	0	0	20h
V _{SS}	SCL	V _{DD}	0	0	1	0	0	0	1	22h
V _{SS}	SDA	V _{SS}	0	0	1	0	0	1	0	24h
V _{SS}	SDA	V _{DD}	0	0	1	0	0	1	1	26h
V _{DD}	SCL	V _{SS}	0	0	1	0	1	0	0	28h
V _{DD}	SCL	V _{DD}	0	0	1	0	1	0	1	2Ah
V _{DD}	SDA	V _{SS}	0	0	1	0	1	1	0	2Ch
V _{DD}	SDA	V _{DD}	0	0	1	0	1	1	1	2Eh
V _{SS}	SCL	SCL	0	0	1	1	0	0	0	30h
V _{SS}	SCL	SDA	0	0	1	1	0	0	1	32h
V _{SS}	SDA	SCL	0	0	1	1	0	1	0	34h
V _{SS}	SDA	SDA	0	0	1	1	0	1	1	36h
V _{DD}	SCL	SCL	0	0	1	1	1	0	0	38h
V _{DD}	SCL	SDA	0	0	1	1	1	0	1	3Ah
V _{DD}	SDA	SCL	0	0	1	1	1	1	0	3Ch
V _{DD}	SDA	SDA	0	0	1	1	1	1	1	3Eh
V _{SS}	V _{SS}	V _{SS}	0	1	0	0	0	0	0	40h
V _{SS}	V _{SS}	V _{DD}	0	1	0	0	0	0	1	42h
V _{SS}	V _{DD}	V _{SS}	0	1	0	0	0	1	0	44h
V _{SS}	V _{DD}	V _{DD}	0	1	0	0	0	1	1	46h
V _{DD}	V _{SS}	V _{SS}	0	1	0	0	1	0	0	48h
V _{DD}	V _{SS}	V _{DD}	0	1	0	0	1	0	1	4Ah
V _{DD}	V _{DD}	V _{SS}	0	1	0	0	1	1	0	4Ch
V _{DD}	V _{DD}	V _{DD}	0	1	0	0	1	1	1	4Eh

Table 5. PCA9674 address map ...continued

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address
V _{SS}	V _{SS}	SCL	0	1	0	1	0	0	0	50h
V _{SS}	V _{SS}	SDA	0	1	0	1	0	0	1	52h
V _{SS}	V _{DD}	SCL	0	1	0	1	0	1	0	54h
V _{SS}	V _{DD}	SDA	0	1	0	1	0	1	1	56h
V _{DD}	V _{SS}	SCL	0	1	0	1	1	0	0	58h
V _{DD}	V _{SS}	SDA	0	1	0	1	1	0	1	5Ah
V _{DD}	V _{DD}	SCL	0	1	0	1	1	1	0	5Ch
V _{DD}	V _{DD}	SDA	0	1	0	1	1	1	1	5Eh
SCL	SCL	V _{SS}	1	0	1	0	0	0	0	A0h
SCL	SCL	V _{DD}	1	0	1	0	0	0	1	A2h
SCL	SDA	V _{SS}	1	0	1	0	0	1	0	A4h
SCL	SDA	V _{DD}	1	0	1	0	0	1	1	A6h
SDA	SCL	V _{SS}	1	0	1	0	1	0	0	A8h
SDA	SCL	V _{DD}	1	0	1	0	1	0	1	AAh
SDA	SDA	V _{SS}	1	0	1	0	1	1	0	ACh
SDA	SDA	V _{DD}	1	0	1	0	1	1	1	A Eh
SCL	SCL	SCL	1	0	1	1	0	0	0	B0h
SCL	SCL	SDA	1	0	1	1	0	0	1	B2h
SCL	SDA	SCL	1	0	1	1	0	1	0	B4h
SCL	SDA	SDA	1	0	1	1	0	1	1	B6h
SDA	SCL	SCL	1	0	1	1	1	0	0	B8h
SDA	SCL	SDA	1	0	1	1	1	0	1	BAh
SDA	SDA	SCL	1	0	1	1	1	1	0	BCh
SDA	SDA	SDA	1	0	1	1	1	1	1	BEh
SCL	V _{SS}	V _{SS}	1	1	0	0	0	0	0	C0h
SCL	V _{SS}	V _{DD}	1	1	0	0	0	0	1	C2h
SCL	V _{DD}	V _{SS}	1	1	0	0	0	1	0	C4h
SCL	V _{DD}	V _{DD}	1	1	0	0	0	1	1	C6h
SDA	V _{SS}	V _{SS}	1	1	0	0	1	0	0	C8h
SDA	V _{SS}	V _{DD}	1	1	0	0	1	0	1	CAh
SDA	V _{DD}	V _{SS}	1	1	0	0	1	1	0	CCh
SDA	V _{DD}	V _{DD}	1	1	0	0	1	1	1	CEh
SCL	V _{SS}	SCL	1	1	1	0	0	0	0	E0h
SCL	V _{SS}	SDA	1	1	1	0	0	0	1	E2h
SCL	V _{DD}	SCL	1	1	1	0	0	1	0	E4h
SCL	V _{DD}	SDA	1	1	1	0	0	1	1	E6h
SDA	V _{SS}	SCL	1	1	1	0	1	0	0	E8h
SDA	V _{SS}	SDA	1	1	1	0	1	0	1	E Ah
SDA	V _{DD}	SCL	1	1	1	0	1	1	0	ECh
SDA	V _{DD}	SDA	1	1	1	0	1	1	1	E Eh

Table 6. PCA9674A address map

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address
V _{SS}	SCL	V _{SS}	0	0	0	1	0	0	0	10h
V _{SS}	SCL	V _{DD}	0	0	0	1	0	0	1	12h
V _{SS}	SDA	V _{SS}	0	0	0	1	0	1	0	14h
V _{SS}	SDA	V _{DD}	0	0	0	1	0	1	1	16h
V _{DD}	SCL	V _{SS}	0	0	0	1	1	0	0	18h
V _{DD}	SCL	V _{DD}	0	0	0	1	1	0	1	1Ah
V _{DD}	SDA	V _{SS}	0	0	0	1	1	1	0	1Ch
V _{DD}	SDA	V _{DD}	0	0	0	1	1	1	1	1Eh
V _{SS}	SCL	SCL	0	1	1	0	0	0	0	60h
V _{SS}	SCL	SDA	0	1	1	0	0	0	1	62h
V _{SS}	SDA	SCL	0	1	1	0	0	1	0	64h
V _{SS}	SDA	SDA	0	1	1	0	0	1	1	66h
V _{DD}	SCL	SCL	0	1	1	0	1	0	0	68h
V _{DD}	SCL	SDA	0	1	1	0	1	0	1	6Ah
V _{DD}	SDA	SCL	0	1	1	0	1	1	0	6Ch
V _{DD}	SDA	SDA	0	1	1	0	1	1	1	6Eh
V _{SS}	V _{SS}	V _{SS}	0	1	1	1	0	0	0	70h
V _{SS}	V _{SS}	V _{DD}	0	1	1	1	0	0	1	72h
V _{SS}	V _{DD}	V _{SS}	0	1	1	1	0	1	0	74h
V _{SS}	V _{DD}	V _{DD}	0	1	1	1	0	1	1	76h
V _{DD}	V _{SS}	V _{SS}	0	1	1	1	1	0	0	78h
V _{DD}	V _{SS}	V _{DD}	0	1	1	1	1	0	1	7Ah
V _{DD}	V _{DD}	V _{SS}	0	1	1	1	1	1	0	7Ch
V _{DD}	V _{DD}	V _{DD}	0	1	1	1	1	1	1	7Eh
V _{SS}	V _{SS}	SCL	1	0	0	0	0	0	0	80h
V _{SS}	V _{SS}	SDA	1	0	0	0	0	0	1	82h
V _{SS}	V _{DD}	SCL	1	0	0	0	0	1	0	84h
V _{SS}	V _{DD}	SDA	1	0	0	0	0	1	1	86h
V _{DD}	V _{SS}	SCL	1	0	0	0	1	0	0	88h
V _{DD}	V _{SS}	SDA	1	0	0	0	1	0	1	8Ah
V _{DD}	V _{DD}	SCL	1	0	0	0	1	1	0	8Ch
V _{DD}	V _{DD}	SDA	1	0	0	0	1	1	1	8Eh
SCL	SCL	V _{SS}	1	0	0	1	0	0	0	90h
SCL	SCL	V _{DD}	1	0	0	1	0	0	1	92h
SCL	SDA	V _{SS}	1	0	0	1	0	1	0	94h
SCL	SDA	V _{DD}	1	0	0	1	0	1	1	96h
SDA	SCL	V _{SS}	1	0	0	1	1	0	0	98h
SDA	SCL	V _{DD}	1	0	0	1	1	0	1	9Ah
SDA	SDA	V _{SS}	1	0	0	1	1	1	0	9Ch
SDA	SDA	V _{DD}	1	0	0	1	1	1	1	9Eh

Table 6. PCA9674A address map ...continued

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address
SCL	SCL	SCL	1	1	1	0	0	0	0	D0h
SCL	SCL	SDA	1	1	1	0	0	0	1	D2h
SCL	SDA	SCL	1	1	1	0	0	1	0	D4h
SCL	SDA	SDA	1	1	1	0	0	1	1	D6h
SDA	SCL	SCL	1	1	1	0	1	0	0	D8h
SDA	SCL	SDA	1	1	1	0	1	0	1	DAh
SDA	SDA	SCL	1	1	1	0	1	1	0	DCh
SDA	SDA	SDA	1	1	1	0	1	1	1	DEh
SCL	V _{SS}	V _{SS}	1	1	1	1	0	0	0	F0h
SCL	V _{SS}	V _{DD}	1	1	1	1	0	0	1	F2h
SCL	V _{DD}	V _{SS}	1	1	1	1	0	1	0	F4h
SCL	V _{DD}	V _{DD}	1	1	1	1	0	1	1	F6h
SDA	V _{SS}	V _{SS}	1	1	1	1	1	0	0	[1]
SDA	V _{SS}	V _{DD}	1	1	1	1	1	0	1	FAh
SDA	V _{DD}	V _{SS}	1	1	1	1	1	1	0	FCh
SDA	V _{DD}	V _{DD}	1	1	1	1	1	1	1	FEh
SCL	V _{SS}	SCL	0	0	0	0	0	0	0	[1]
SCL	V _{SS}	SDA	0	0	0	0	0	0	1	02h
SCL	V _{DD}	SCL	0	0	0	0	0	1	0	04h
SCL	V _{DD}	SDA	0	0	0	0	0	1	1	06h
SDA	V _{SS}	SCL	0	0	0	0	1	0	0	08h
SDA	V _{SS}	SDA	0	0	0	0	1	0	1	0Ah
SDA	V _{DD}	SCL	0	0	0	0	1	1	0	0Ch
SDA	V _{DD}	SDA	0	0	0	0	1	1	1	0Eh

[1] The PCA9674A does not acknowledge when AD2, AD1, AD0 follows this configuration.

7.2 Software Reset Call, and device ID addresses

Two other different addresses can be sent to the PCA9674/74A.

- General Call address: allows to reset the PCA9674/74A through the I²C-bus upon reception of the right I²C-bus sequence. See [Section 7.2.1 “Software Reset”](#) for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See [Section 7.2.2 “Device ID \(PCA9674/74A ID field\)”](#) for more information.

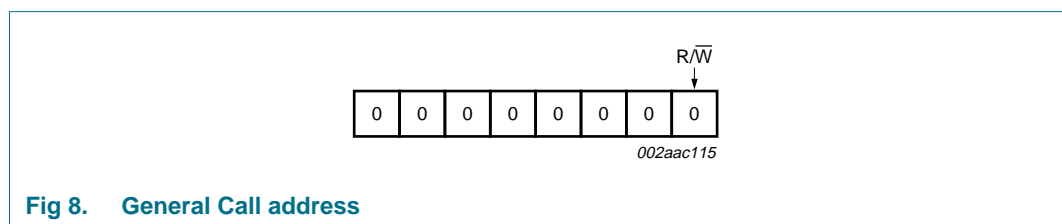
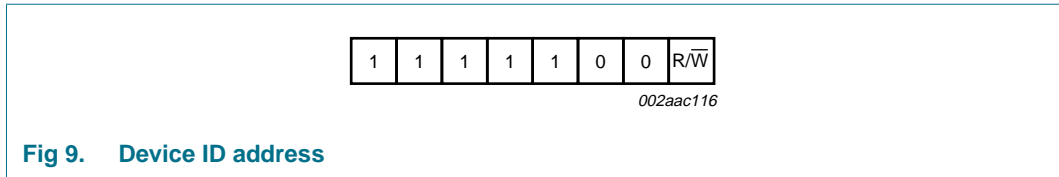


Fig 8. General Call address



7.2.1 Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

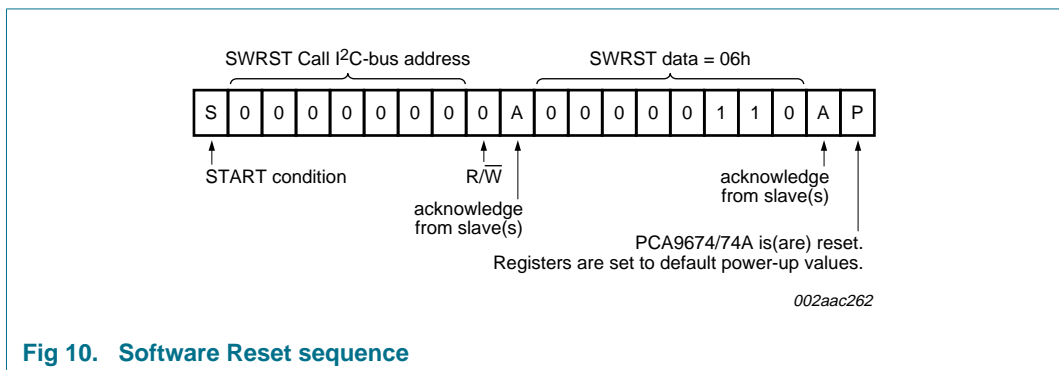
1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address '0000 000' with the R/W bit set to 0 (write) is sent by the I²C-bus master.
3. The PCA9674/74A device(s) acknowledge(s) after seeing the General Call address '0000 0000' (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
 - a. The PCA9674/74A acknowledges this value only. If the byte is not equal to 06h, the PCA9674/74A does not acknowledge it.

If more than 1 byte of data is sent, the PCA9674/74A does not acknowledge any more.

5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the PCA9674/74A then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the PCA9674/74A (at any time) as a 'Software Reset Abort'. The PCA9674/74A does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in [Figure 10](#).



7.2.2 Device ID (PCA9674/74A ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 8 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 13 bits with the part identification, assigned by manufacturer, the 7 MSBs with the category ID and the 6 LSBs with the feature ID (for example, for example PCA9674/74A 16-bit quasi-output I/O expander).
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I²C-bus address '1111 100' with the R/W bit set to 0 (write).
3. The master sends the I²C-bus slave address of the slave device it needs to identify. The LSB is a 'Don't care' value. Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
4. The master sends a Re-START command.

Remark: A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed.

Remark: A STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID read cannot be performed.

5. The master sends the Reserved Device ID I²C-bus address '1111 100' with the R/W bit set to 1 (read).
6. The device ID read can be done, starting with the 8 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 13 part identification bits and then the 3 die revision bits (3 LSB of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

Remark: The reading of the Device ID can be stopped anytime by sending a NACK command.

Remark: If the master continues to ACK the bytes after the third byte, the PCA9674/74A rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCA9674/74A, the Device ID is as shown in [Figure 11](#).

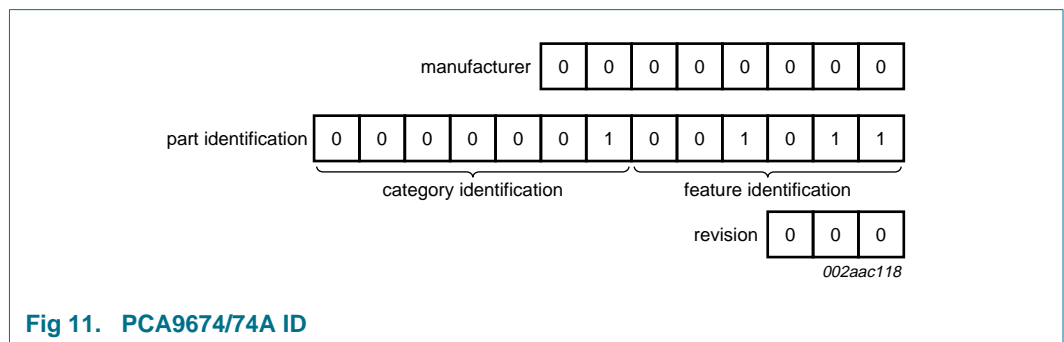
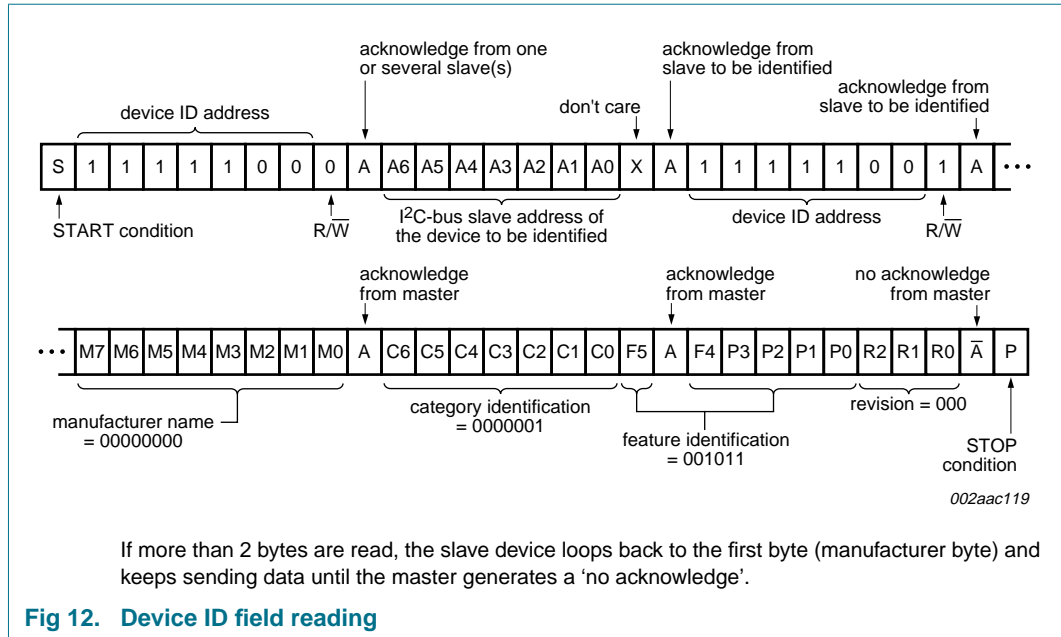


Fig 11. PCA9674/74A ID



8. I/O programming

8.1 Quasi-bidirectional I/O architecture

The PCA9674/74A's 8 ports (see [Figure 2](#)) are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the Read mode (see [Figure 14](#)). Output data is transmitted to the ports in the Write mode (see [Figure 13](#)).

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data directions. At power-on the I/Os are HIGH. In this mode only a current source (I_{OH}) to V_{DD} is active. An additional strong pull-up to V_{DD} ($I_{trt(pu)}$) allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. After power-on, as all the I/Os are set HIGH, all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode.

Remark: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current (I_{OL}) will flow to V_{SS} .

8.2 Writing to the port (Output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the write mode is entered. The PCA9674/74A acknowledges and the master sends the data byte for P7 to P0 and is acknowledged by the PCA9674/74A. The 8-bit data is presented on the port lines after it has been acknowledged by the PCA9674/74A.

The number of data bytes that can be sent successively is not limited. The previous data is overwritten every time a data byte has been sent.

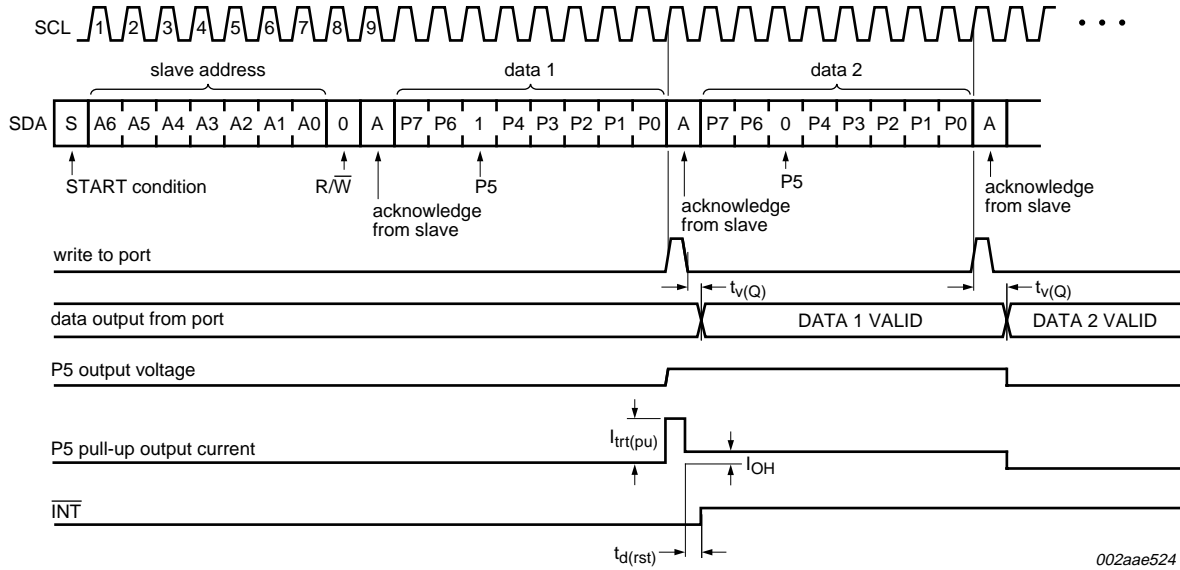
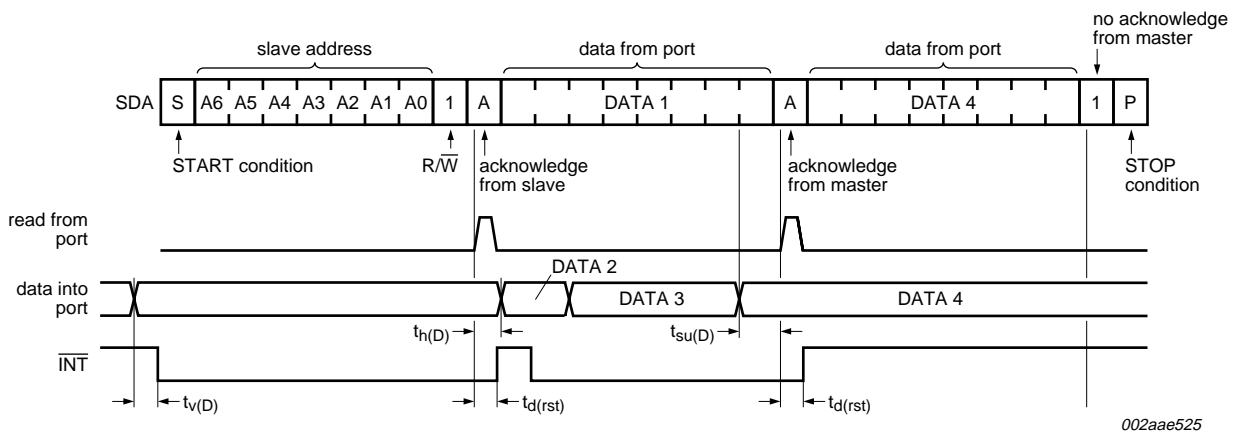


Fig 13. Write mode (output)

8.3 Reading from a port (Input mode)

All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the Read mode is entered. The data bytes that follow on the SDA are the values on the ports.

If the data on the input port changes faster than the master can read, this data may be lost.



A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the last acknowledge phase is valid (Output mode). Input data is lost.

Fig 14. Read input port register

8.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9674/74A in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9674/74A registers and I²C-bus/SMBus state machine will initialize to their default states. Thereafter V_{DD} must be lowered below 0.2 V to reset the device.

8.5 Interrupt output ($\overline{\text{INT}}$)

The PCA9674/74A provides an open-drain interrupt ($\overline{\text{INT}}$) which can be fed to a corresponding input of the microcontroller (see [Figure 13](#), [Figure 14](#), and [Figure 15](#)). This gives these chips a kind of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs. After time t_{v(D)} the signal $\overline{\text{INT}}$ is valid.

The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.

In the write mode, the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).

The interrupt is reset in the read mode on the rising edge of the read from port pulse.

During the resetting of the interrupt itself, any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an $\overline{\text{INT}}$.

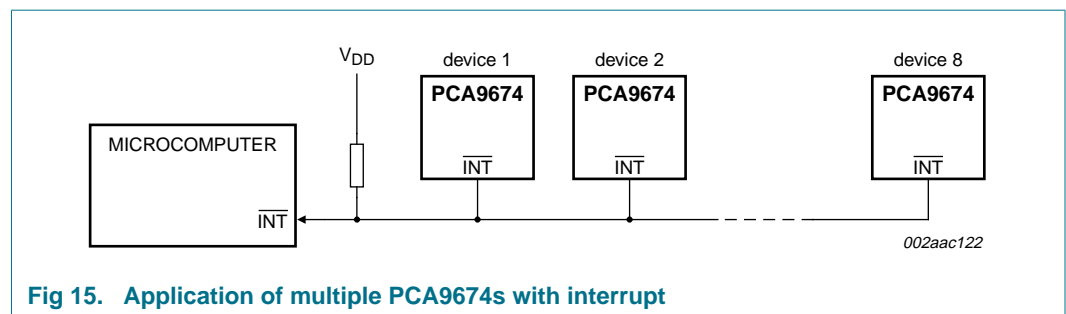


Fig 15. Application of multiple PCA9674s with interrupt

9. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 16](#)).

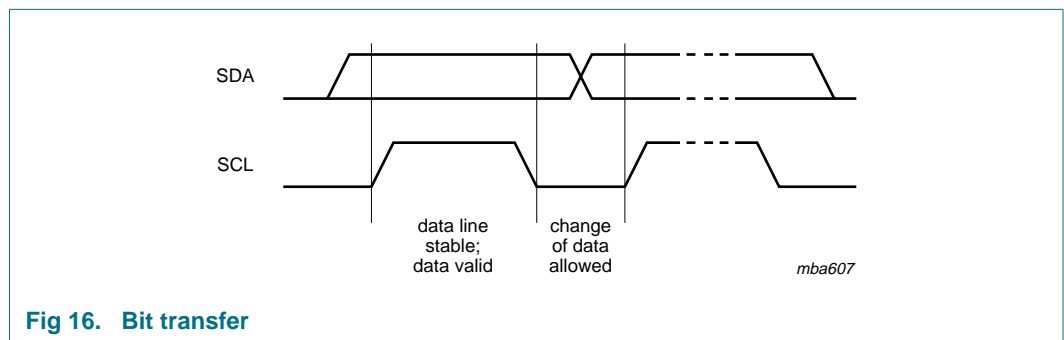


Fig 16. Bit transfer

9.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 17](#)).

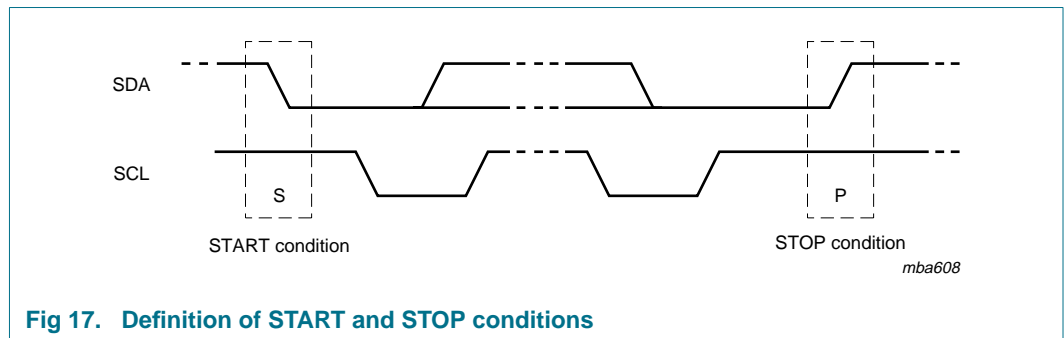


Fig 17. Definition of START and STOP conditions

9.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 18](#)).

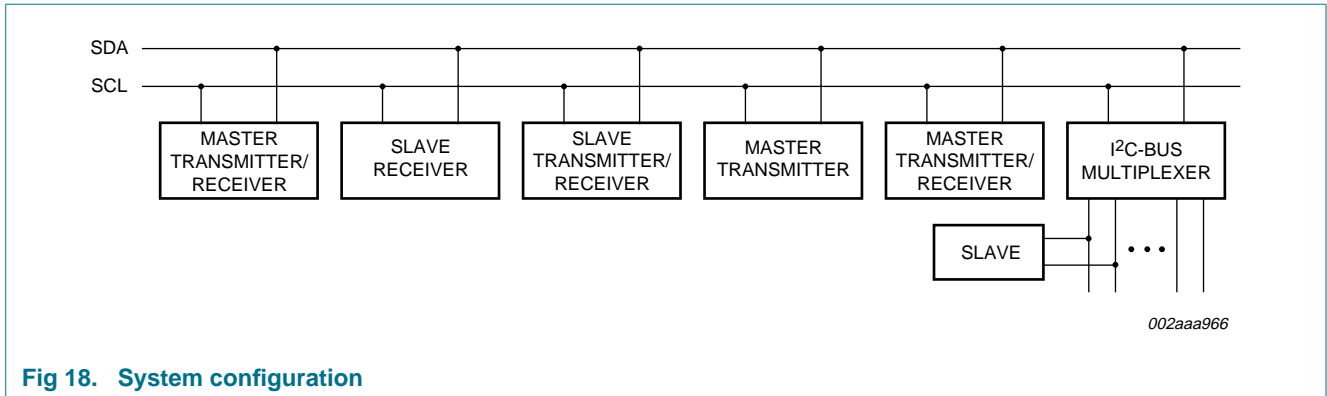


Fig 18. System configuration

9.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

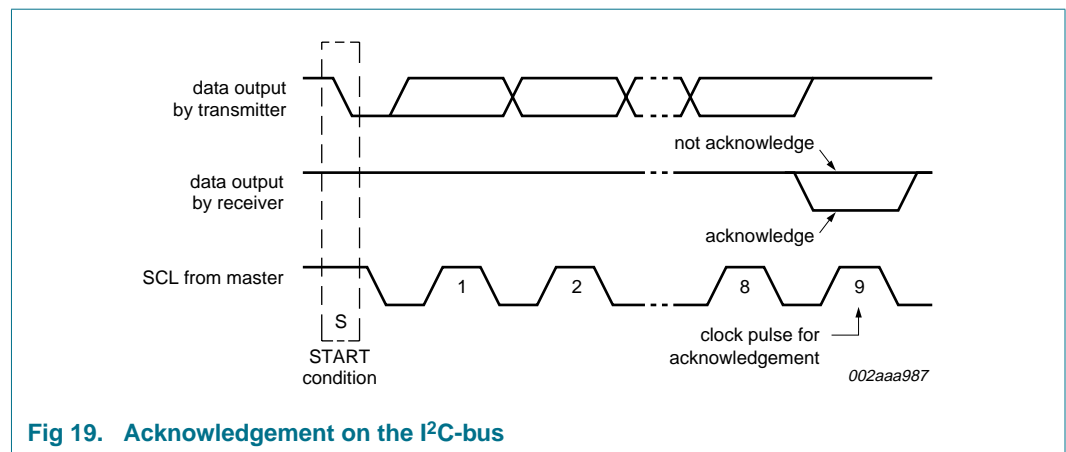


Fig 19. Acknowledgement on the I²C-bus

10. Application design-in information

10.1 Bidirectional I/O expander applications

In the 8-bit I/O expander application shown in [Figure 20](#), P0 and P1 are inputs, and P2 to P7 are outputs. When used in this configuration, during a write, the input (P0 and P1) must be written as HIGH so the external devices fully control the input ports. The desired HIGH or LOW logic levels may be written to the I/Os used as outputs (P2 to P7). During a read, the logic levels of the external devices driving the input ports (P0 and P1) and the previous written logic level to the output ports (P2 to P7) will be read.

The GPIO also has an interrupt line (\overline{INT}) that can be connected to the interrupt logic of the microprocessor. By sending an interrupt signal on this line, the remote I/O informs the microprocessor that there is incoming data or a change of data on its ports without having to communicate via the I²C-bus.

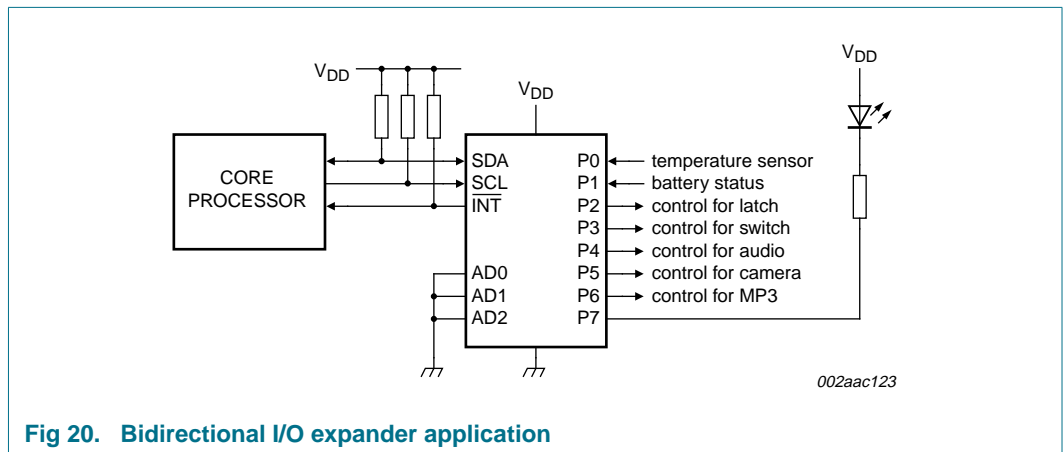


Fig 20. Bidirectional I/O expander application

10.2 High current-drive load applications

The GPIO has a maximum sinking current of 25 mA per bit. In applications requiring additional drive, two port pins in the same octal may be connected together to sink up to 50 mA current. Both bits must then always be turned on or off together. Up to 8 pins (one octal) can be connected together to drive 200 mA.

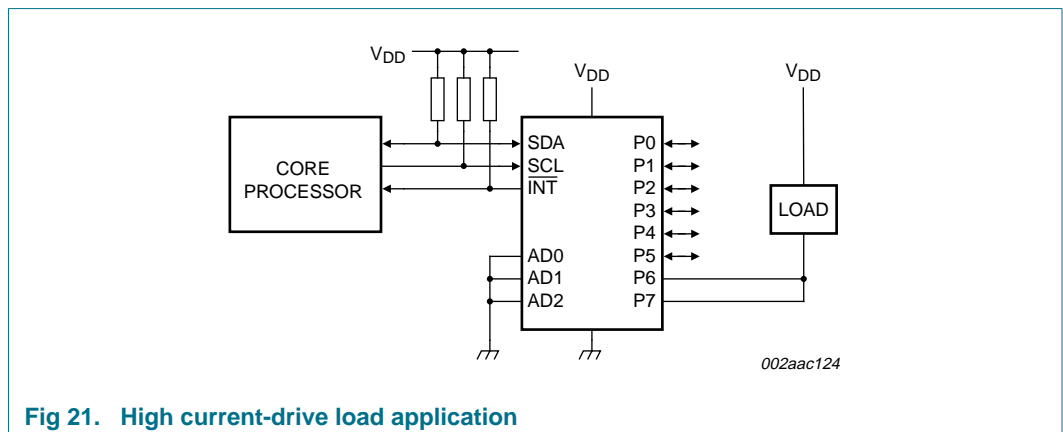


Fig 21. High current-drive load application

11. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+6	V
I _{DD}	supply current		-	±100	mA
I _{SS}	ground supply current		-	±400	mA
V _I	input voltage		V _{SS} - 0.5	5.5	V
I _I	input current		-	±20	mA
I _O	output current	[1]	-	±50	mA
P _{tot}	total power dissipation		-	400	mW
P/out	power dissipation per output		-	100	mW
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature	operating	-40	+85	°C

[1] Total package (maximum) output current is 400 mA.

12. Static characteristics

Table 8. Static characteristics

$V_{DD} = 2.3\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		2.3	-	5.5	V
I_{DD}	supply current	Operating mode; no load; $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 1\text{ MHz}$; AD0, AD1, AD2 = static H or L	-	200	500	μA
I_{stb}	standby current	Standby mode; no load; $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 0\text{ kHz}$	-	4.5	10	μA
V_{POR}	power-on reset voltage		[1] -	1.8	2.0	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		-0.5	-	+0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$; $V_{DD} = 2.3\text{ V}$	20	35	-	mA
		$V_{OL} = 0.4\text{ V}$; $V_{DD} = 3.0\text{ V}$	25	44	-	mA
		$V_{OL} = 0.4\text{ V}$; $V_{DD} = 4.5\text{ V}$	30	57	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	-1	-	+1	μA
C_i	input capacitance	$V_I = V_{SS}$	-	5	10	pF
I/Os; P0 to P7						
I_{OL}	LOW-level output current	$V_{OL} = 0.5\text{ V}$; $V_{DD} = 2.3\text{ V}$	[2] 12	26	-	mA
		$V_{OL} = 0.5\text{ V}$; $V_{DD} = 3.0\text{ V}$	[2] 17	33	-	mA
		$V_{OL} = 0.5\text{ V}$; $V_{DD} = 4.5\text{ V}$	[2] 25	40	-	mA
$I_{OL(tot)}$	total LOW-level output current	$V_{OL} = 0.5\text{ V}$; $V_{DD} = 4.5\text{ V}$	[2] -	-	200	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{SS}$	-30	-138	-300	μA
$I_{trt(pu)}$	transient boosted pull-up current	$V_{OH} = V_{SS}$; see Figure 13	-0.5	-1.0	-	mA
C_i	input capacitance		[3] -	2.1	10	pF
C_o	output capacitance		[3] -	2.1	10	pF
Interrupt INT (see Figure 14 and Figure 13)						
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3.0	-	-	mA
C_o	output capacitance		-	3	5	pF
Inputs AD0, AD1, AD2						
V_{IL}	LOW-level input voltage		-0.5	-	+0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	5.5	V
I_{LI}	input leakage current		-1	-	+1	μA
C_i	input capacitance		-	3.5	5	pF

[1] V_{DD} must be lowered to 0.2 V or less in order to reset part.

[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 200 mA due to internal busing limits.

[3] The value is verified by characterization.

13. Dynamic characteristics

Table 9. Dynamic characteristics
 $V_{DD} = 2.3\text{ V to }5.5\text{ V}; V_{SS} = 0\text{ V}; T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C};$ unless otherwise specified.

Symbol	Parameter	Conditions	Standard mode I ² C-bus		Fast mode I ² C-bus		Fast-mode Plus I ² C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f _{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t _{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	μs
t _{HD;STA}	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	μs
t _{SU;STA}	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	μs
t _{SU;STO}	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	μs
t _{HD;DAT}	data hold time		0	-	0	-	0	-	ns
t _{VD;ACK}	data valid acknowledge time ^[1]		0.3	3.45	0.1	0.9	0.05	0.45	μs
t _{VD;DAT}	data valid time ^[2]		300	-	50	-	50	450	ns
t _{SU;DAT}	data set-up time		250	-	100	-	50	-	ns
t _{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	μs
t _{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	μs
t _f	fall time of both SDA and SCL signals	^[4] ^[5]	-	300	20 + 0.1C _b ^[3]	300	-	120	ns
t _r	rise time of both SDA and SCL signals		-	1000	20 + 0.1C _b ^[3]	300	-	120	ns
t _{SP}	pulse width of spikes that must be suppressed by the input filter ^[6]		-	50	-	50	-	50	ns
Port timing; C_L ≤ 100 pF (see Figure 13 and Figure 14)									
t _{v(Q)}	data output valid time		-	4	-	4	-	4	μs
t _{su(D)}	data input set-up time		0	-	0	-	0	-	μs
t _{h(D)}	data input hold time		4	-	4	-	4	-	μs
Interrupt timing; C_L ≤ 100 pF (see Figure 13 and Figure 14)									
t _{v(D)}	data input valid time		-	4	-	4	-	4	μs
t _{d(rst)}	reset delay time		-	4	-	4	-	4	μs

[1] t_{VD;ACK} = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

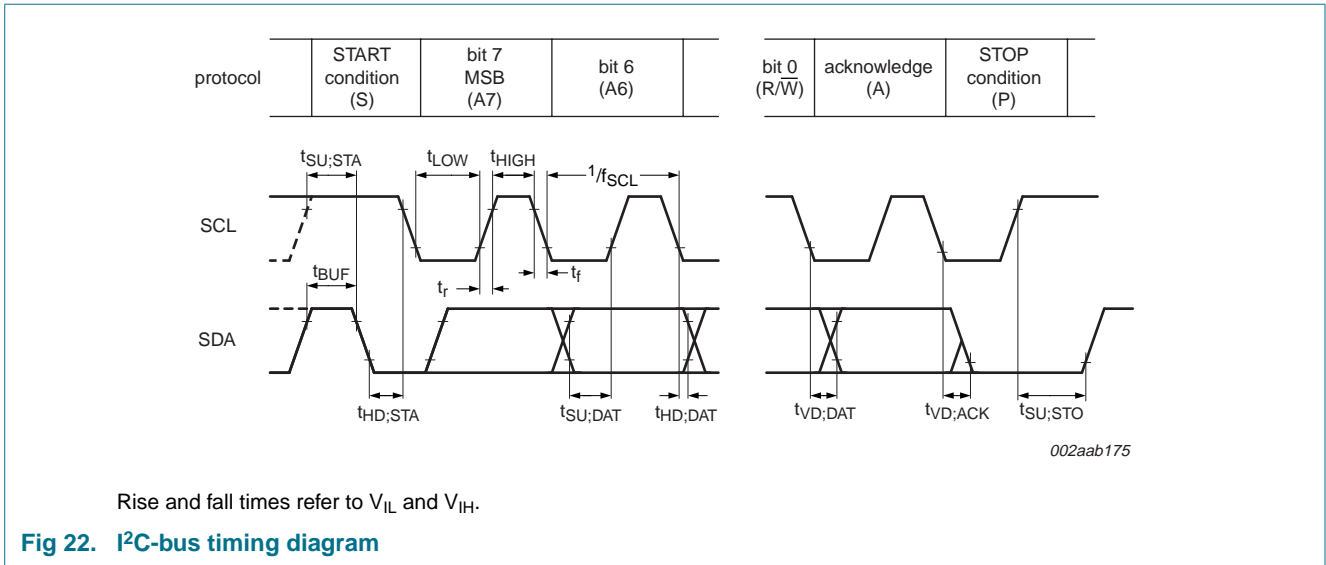
[2] t_{VD;DAT} = minimum time for SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

[4] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.

[5] The maximum t_r for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_r.

[6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.



14. Package outline

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm

SOT758-1

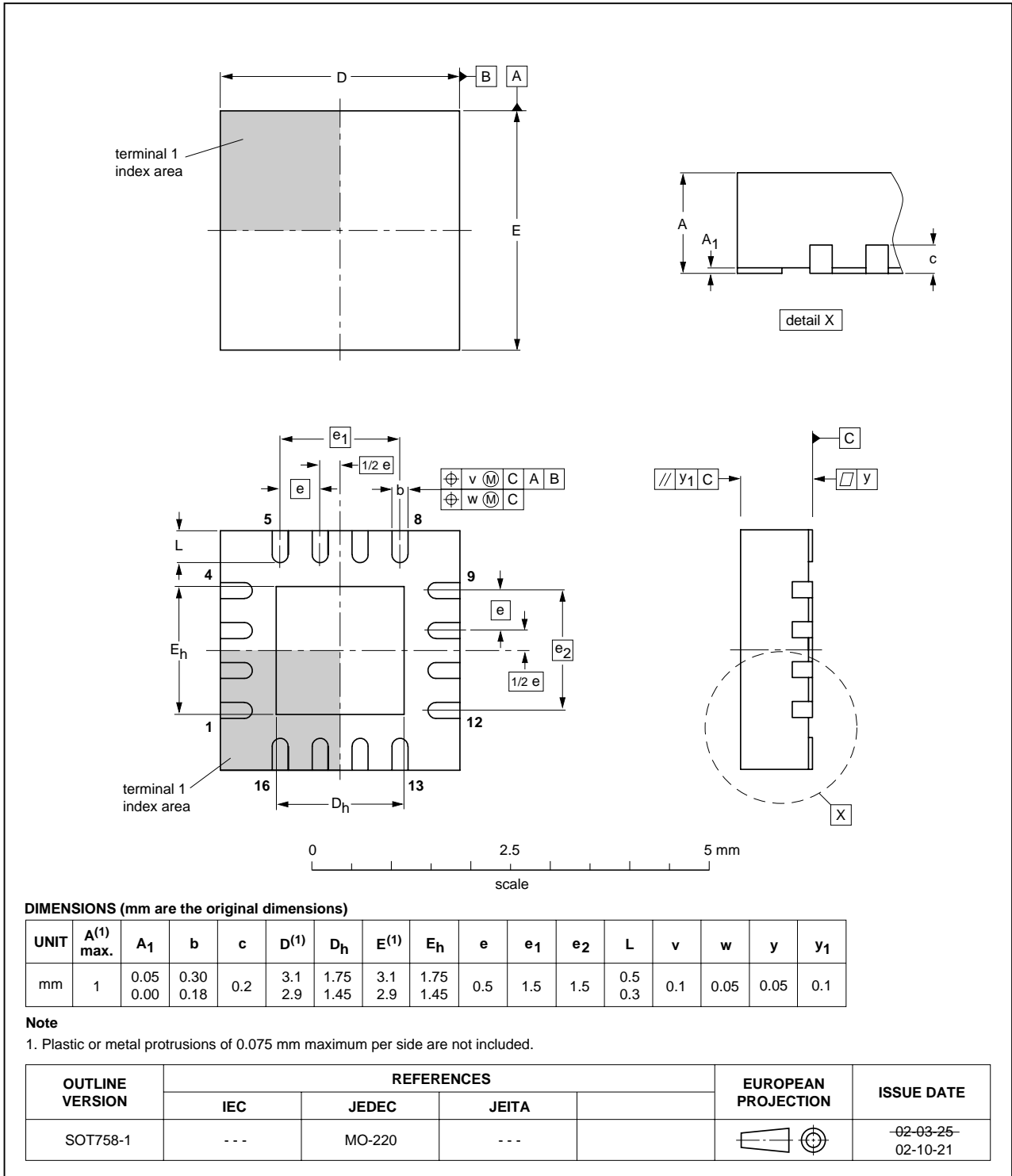


Fig 23. Package outline SOT758-1 (HVQFN16)

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1

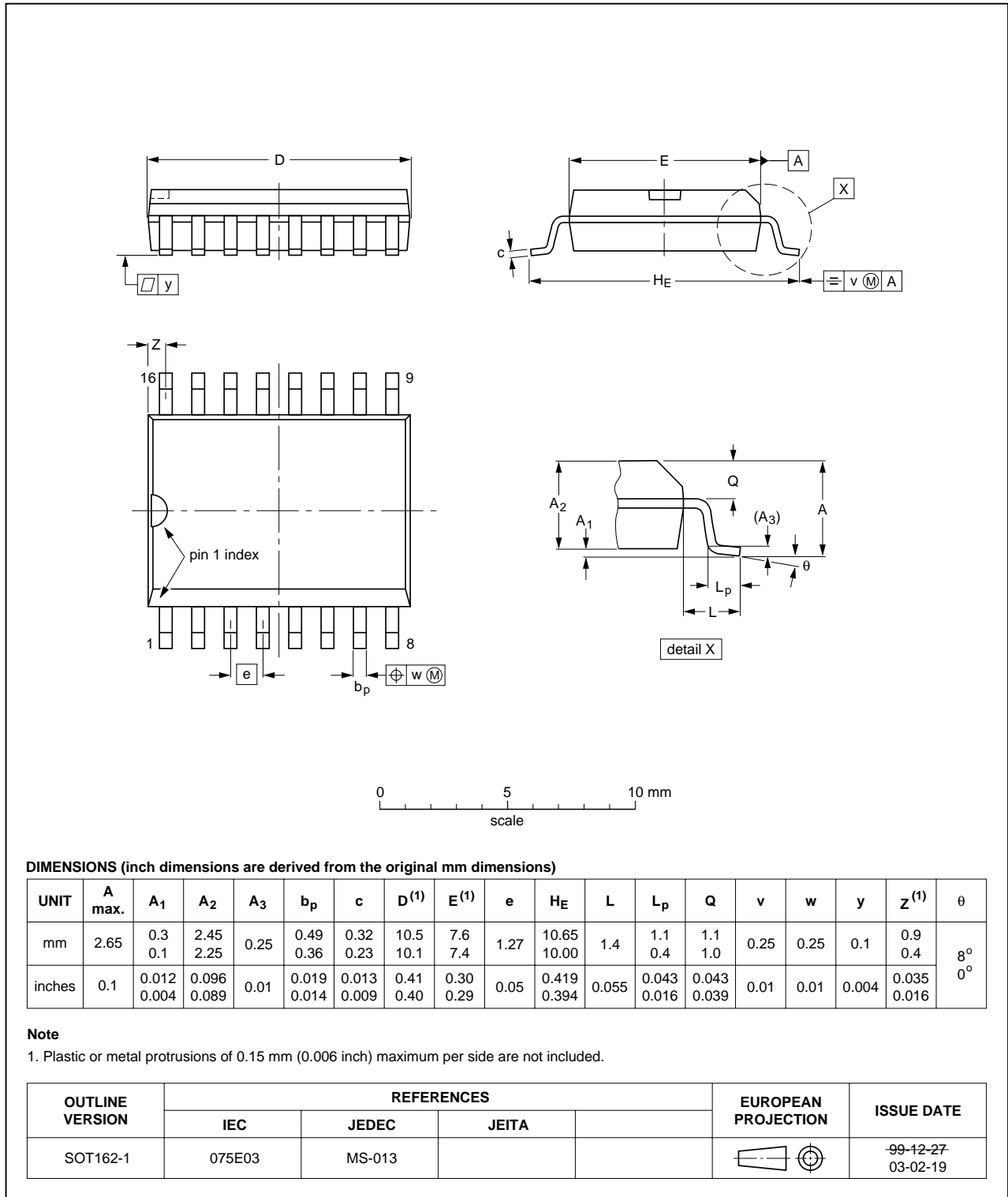


Fig 24. Package outline SOT162-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

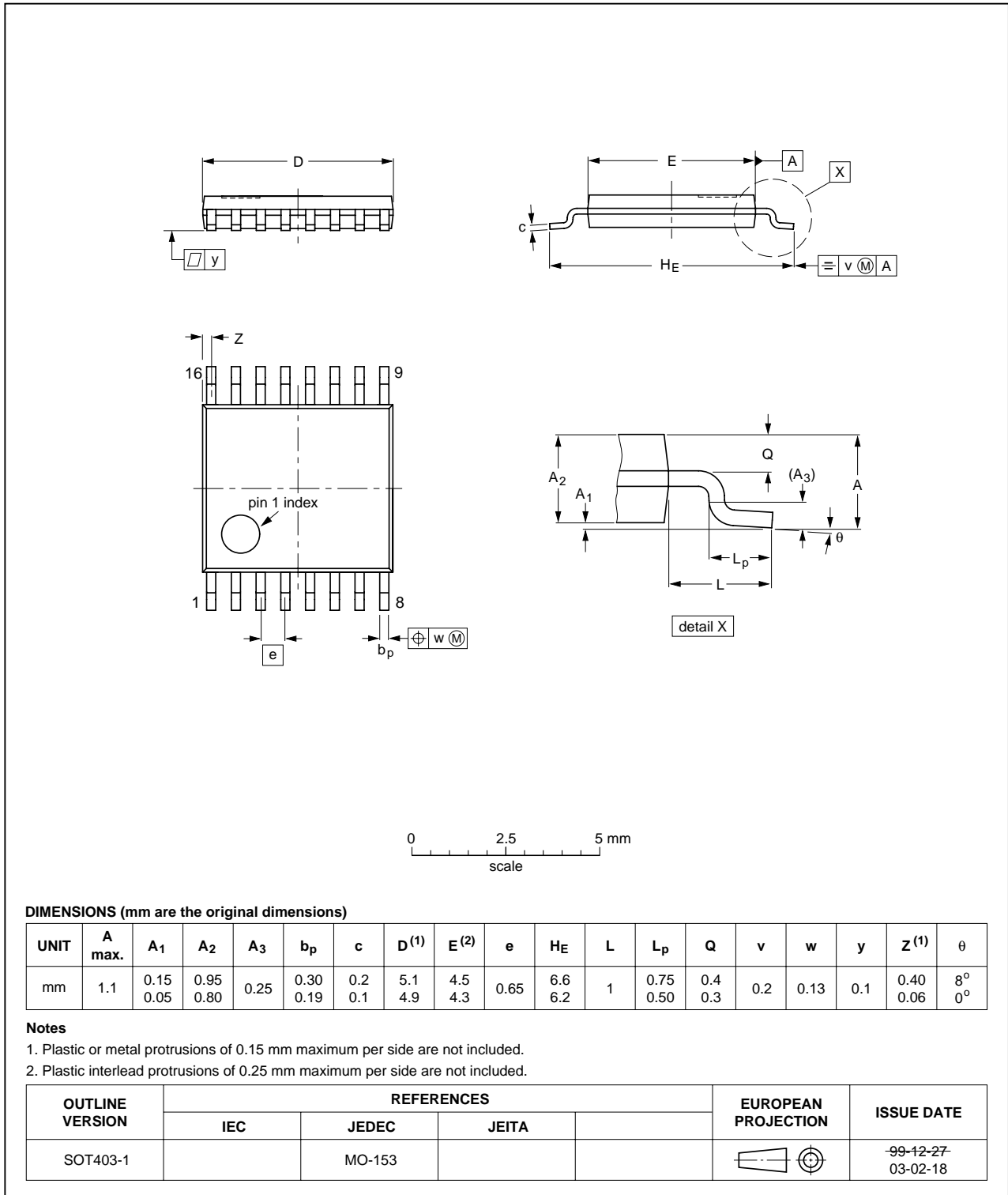


Fig 25. Package outline SOT403-1 (TSSOP16)

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1

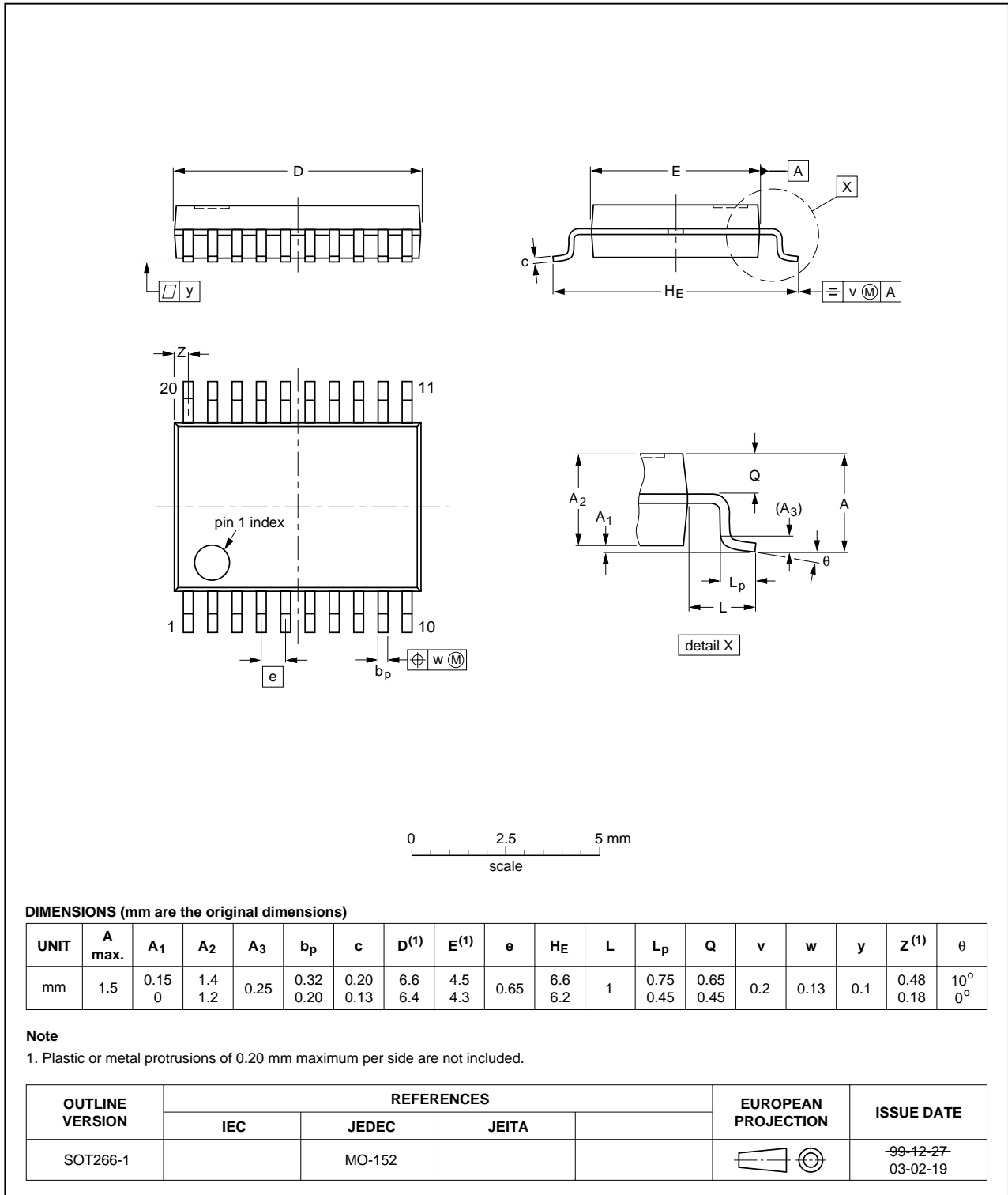


Fig 26. Package outline SOT266-1 (SSOP20)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 27](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [11](#)

Table 10. SnPb eutectic process (from J-STD-020C)

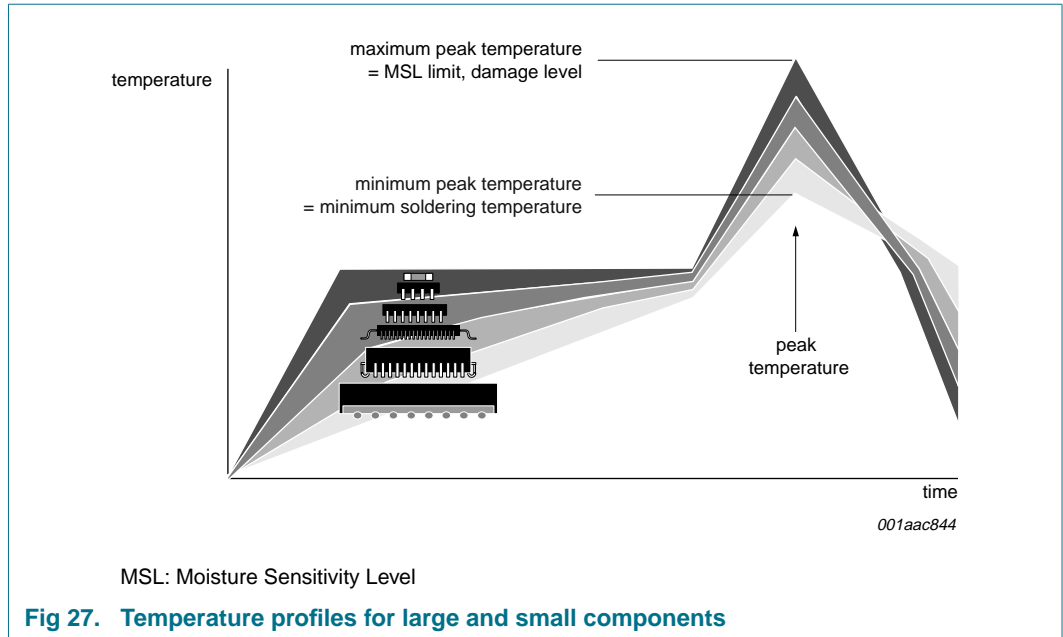
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 27](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

17. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
LED	Light Emitting Diode
IC	Integrated Circuit
I ² C-bus	Inter-Integrated Circuit bus
ID	Identification
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PLC	Programmable Logic Controller
PWM	Pulse Width Modulation
SMBus	System Management Bus

18. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9674_PCA9674A_5	20090615	Product data sheet	-	PCA9674_PCA9674A_4
Modifications:	<ul style="list-style-type: none">• Table 8 “Static characteristics”:<ul style="list-style-type: none">– Table note [1] re-written.– Table note [3] re-written.			
PCA9674_PCA9674A_4	20090303	Product data sheet	-	PCA9674_PCA9674A_3
PCA9674_PCA9674A_3	20070907	Product data sheet	-	PCA9674_PCA9674A_2
PCA9674_PCA9674A_2	20061012	Product data sheet	-	PCA9674_PCA9674A_1
PCA9674_PCA9674A_1	20060905	Objective data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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