DATA SHEET

PCK2001

14.318–150 MHz I^2C 1:18 clock buffer

Product data
Supersedes data of 1999 Jul 06

2002 Jun 03

Philips
Semiconductors

PHILIPS

14.318–150 MHz I²C 1:18 clock buffer PCK2001

FEATURES

- HIGH speed, LOW noise non-inverting 1–18 buffer
- Typically used to support four SDRAM DIMMs
- Multiple V_{DD}, V_{SS} pins for noise reduction
- 3.3 V operation
- Separate 3-State pin for testing
- ESD protection exceeds 2000 V per Standard 801.2
- Optimized for 66 MHz, 100 MHz and 133 MHz operation
- 175 ps skew outputs
- Available in 48-pin SSOP package
- See PCK2001M for mobile (reduced pincount) 28-pin 1-10 buffer version
- Individual clock output enable/disable via I²C

DESCRIPTION

The PCK2001 is a 1–18 fanout buffer used for 133/100 MHz CPU, 66/33 MHz PCI, 14.318 MHz REF, or 133/100/66 MHz SDRAM clock distribution. 18 outputs are typically used to support up to four SDRAM DIMMS commonly found in desktop, workstation or server applications.

All clock outputs meet Intel's drive, rise/fall time, accuracy, and skew requirements. An I²C interface is included to allow each output to be enabled/disabled individually. An output disabled via the I²C interface will be held in the LOW state. In addition, there is an OE input which 3-States all outputs.

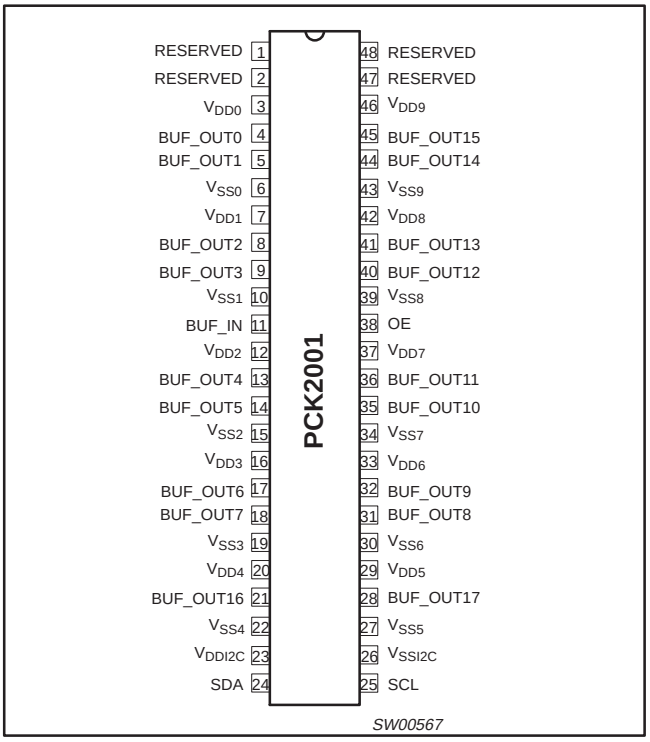
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay BUF_IN to BUF_OUT$_n$	V_{CC} = 3.3 V; C_L = 30 pF	2.5 2.5	ns
t_r	Rise time	V_{CC} = 3.3 V, C_L = 30 pF	1.0	ns
t_f	Fall time	V_{CC} = 3.3 V, C_L = 20 pF	700	ps
I_{CC}	Total supply current	V_{CC} = 3.465 V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic SSOP	0 °C to +70 °C	PCK2001DL	SOT370-1

PIN CONFIGURATION



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PIN DESCRIPTION

PIN NUMBER	I/O TYPE	SYMBOL	FUNCTION
4, 5, 8, 9	Output	BUF_OUT (0–3)	Buffered clock outputs
13, 14, 17, 18	Output	BUF_OUT (4–7)	Buffered clock outputs
31, 32, 35, 36	Output	BUF_OUT (8–11)	Buffered clock outputs
40, 41, 44, 45	Output	BUF_OUT (12–15)	Buffered clock outputs
21, 28	Output	BUF_OUT (16–17)	Buffered clock outputs
11	Input	BUF_IN	Buffered clock input
38	Input	OE	Active-HIGH output enable
24	I/O	SDA	I²C serial data
25	Input	SCL	I²C serial clock
3, 7, 12, 16, 20, 29, 33, 37, 42, 46	Input	$V_{DD\ (0–9)}$	3.3 V power supply
6, 10, 15, 19, 22, 27, 30, 34, 39, 43	Input	$V_{SS\ (0–9)}$	Ground
23	Input	V_{DDI2C}	3.3 V I²C power supply
26	Input	V_{SSI2C}	I²C ground
1, 2, 47, 48	n/a	RESERVED	Undefined

FUNCTION TABLE

OE	BUF_IN	I²CEN	BUF_OUTn
L	X	X	Z
H	L	X	L
H	H	H	H
H	H	L	L

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to V_{SS} (V_{SS} = 0 V).

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC 3.3 V supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	V_I < 0 V		–50	mA
V_I	DC input voltage	Note 2	–0.5	5.5	V
I_{OK}	DC output diode current	V_O > V_{DD} or V_O < 0 V		±50	mA
V_O	DC output voltage	Note 2	–0.5	V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O >= 0 V to V_{DD}		±50	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{TOT}	Power dissipation per package plastic medium-shrink SO (SSOP)	For temperature range: 0 to +70 °C above +55 °C derate linearly with 11.3 mW/K		850	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC 3.3 V supply voltage		3.135	3.465	V
C_L	Capacitive load		20	30	pF
V_I	DC input voltage range		0	V_{DD}	V
V_O	DC output voltage range		0	V_{DD}	V
T_{amb}	Operating ambient temperature range in free air		0	+70	°C

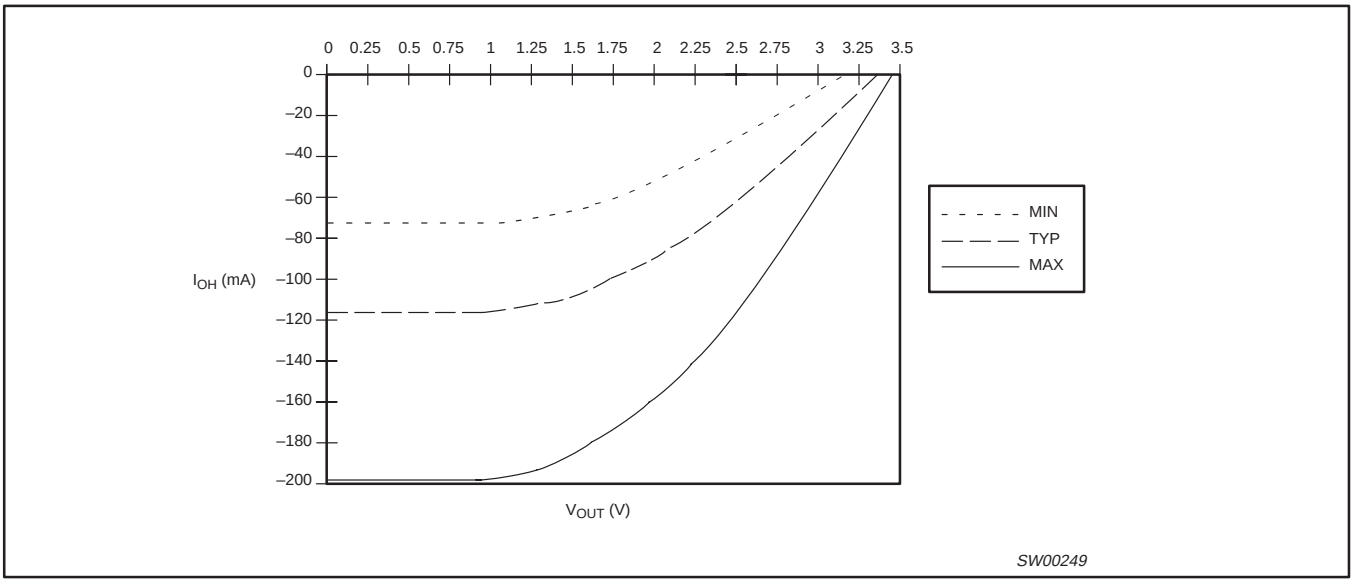
DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS		UNIT
					T_{amb} = 0 °C to +70 °C		
		V_{DD} (V)	OTHER		MIN	MAX	
V_{IH}	HIGH level input voltage	3.135 to 3.465			2.0	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage	3.135 to 3.465			V_{SS} – 0.3	0.8	V
V_{OH}	3.3 V output HIGH voltage	3.135 to 3.465	I_{OH} = –1 mA		2.4	–	V
V_{OL}	3.3 V output LOW voltage	3.135 to 3.465	I_{OL}= 1 mA		–	0.4	V
I_{OH}	Output HIGH current	3.135 to 3.465	V_{OUT} = 2.0 V		–54	–	mA
		3.135 to 3.465	V_{OUT} = 3.135 V		–	–46	mA
I_{OL}	Output LOW current	3.135 to 3.465	V_{OUT} = 1.0 V		54	–	mA
		3.135 to 3.465	V_{OUT} = 0.4 V		–	53	mA
$\pm I_I$	Input leakage current	3.465			–	5	µA
$\pm I_{OZ}$	3-State output OFF-State current	3.465	V_{OUT} = V_{DD} or GND	I_O = 0	–	10	µA
I_{CC}	Quiescent supply current	3.465	V_I = V_{DD} or GND	I_O = 0	–	100	µA
ΔI_{CC}	Additional quiescent supply current given per control pin	3.135 to 3.465	V_I = V_{DD} – 0.6 V	I_O = 0	–	500	µA

SDRAM CLOCK OUTPUT BUFFER PULL-UP CHARACTERISTICS

PULL-UP			
VOLTAGE (V)	I (mA)		
	MIN	TYP	MAX
0	–72	–116	–198
1	–72	–116	–198
1.40	–68	–110	–188
1.50	–67	–107	–184
1.65	–64	–103	–177
1.80	–60	–98	–170
2.00	–54	–90	–157
2.40	–39	–69	–126
2.60	–30	–56	–107
3.135	0	–15	–46
3.30		0	–23
3.465			0

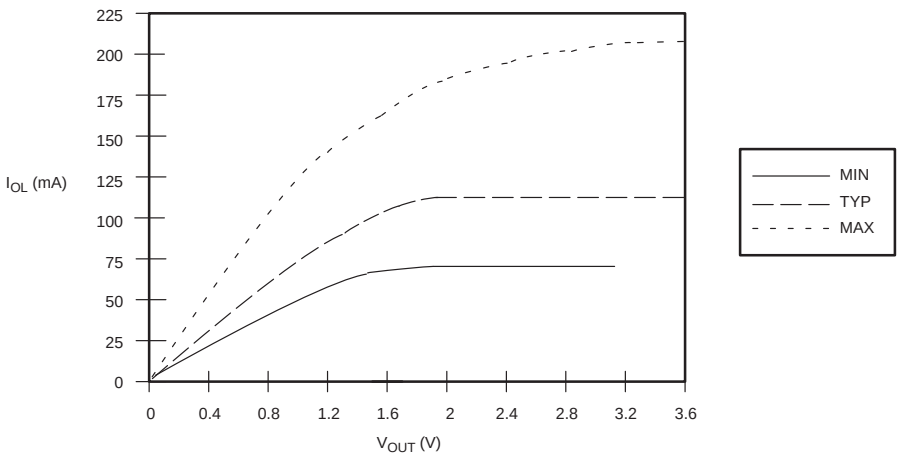
SDRAM PULL-UP



SDRAM CLOCK OUTPUT BUFFER PULL-DOWN CHARACTERISTICS

PULL-UP			
VOLTAGE (V)	I (mA)		
	MIN	TYP	MAX
0	0	0	0
0.4	23	34	53
0.65	35	52	83
0.85	43	65	104
1.00	49	74	118
1.4	61	93	152
1.5	64	98	159
1.65	67	103	168
1.8	70	108	177
1.95	72	112	184
3.135	72	112	204
3.6		112	204

SDRAM PULL-DOWN



AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0 °C to +70 °C			UNIT
			NOTES	MIN	TYP[9]	MAX	
T_{SDKP}	SDRAM CLK period	66 MHz	1, 6	15.0	15.2	15.5	ns
T_{SDKH}	SDRAM CLK HIGH time		2, 6, 8	5.6	7.8	8.4	
T_{SDKL}	SDRAM CLK LOW time		3, 6, 8	5.3	7.4	8.0	
T_{SDKP}	SDRAM CLK period	100 MHz	1, 6	10.0	10.01	10.5	ns
T_{SDKH}	SDRAM CLK HIGH time		2, 6, 8	3.3	5.1	5.7	
T_{SDKL}	SDRAM CLK LOW time		3, 6, 8	3.1	4.9	5.5	
T_{SDKP}	SDRAM clock period	133 MHz	1, 6	7.4	7.5	7.7	ns
T_{SDKH}	SDRAM CLK HIGH time		2, 6, 8	2.6	3.2	3.8	
T_{SDKL}	SDRAM CLK LOW time		3, 6, 8	2.1	2.8	3.5	
T_{SDRISE}	SDRAM rise time		4, 6, 10	1.5	2.0	4.0	V/ns
T_{SDFALL}	SDRAM fall time		4, 6, 11	1.5	2.9	4.0	V/ns
T_{PLH}	SDRAM buffer LH propagation delay		6, 7	1.0	2.5	3.5	ns
T_{PHL}	SDRAM buffer HL propagation delay		6, 7	1.0	2.5	3.5	ns
T_{PZL}, T_{PZH}	SDRAM buffer enable time		6, 7	1.0	2.6	5.0	ns
T_{PLZ}, T_{PHZ}	SDRAM buffer disable time		6, 7	1.0	2.7	5.0	ns
DUTY CYCLE	Output Duty Cycle	Measured at 1.5 V	5, 6, 7	45	52	55	%
T_{SDSKW}	SDRAM Bus CLK skew		1, 6		150	250	ps
T_{DDSKW}	Device to device skew					250	ps

NOTES:
1. Clock period and skew are measured on the rising edge at 1.5 V.
2. T_{SDKH} is measured at 2.4 V as shown in Figure 4.
3. T_{SDKL} is measured at 0.4 V as shown in Figure 4.
4. T_{SDRISE} and T_{SDFALL} are measured as a transition through the threshold region V_{OL} = 0.4 V and V_{OH} = 2.4 V (1 mA) JEDEC specification.
5. Duty cycle should be tested with a 50/50% input.
6. Over MIN (20 pF) to MAX (30 pF) discrete load, process, voltage, and temperature.
7. Input edge rate for these tests must be faster than 1 V/ns.
8. Calculated at minimum edge rate (1.5 ns) to guarantee 45/55% duty cycle at 1.5 V. Pulse width is required to be wider at the faster edge to ensure duty cycle specification is met.
9. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
10. Typical is measured with MAX (30 pF) discrete load.
11. Typical is measured with MIN (20 pF) discrete load.

I²C CONSIDERATIONS

I²C has been chosen as the serial bus interface to control the PCK2001. I²C was chosen to support the JEDEC proposal JC-42.5 168 Pin Unbuffered SDRAM DIMM. All vendors are required to determine the legal issues associated with the manufacture of I²C devices.

1. **Address assignment:** The clock driver in this specification uses the single, 7-bit address shown below. All devices can use the address if only one master clock driver is used in a design. The address can be re-used for the CKBF device if no other conflicting I²C clock driver is used in the system.

   The following address was confirmed by Philips on 09/04/96.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	0	1	0

   NOTE: The R/W# bit is used by the I²C controller as a data direction bit. A ‘zero’ indicates a transmission (WRITE) to the clock device. A ‘one’ indicates a request for data (READ) from the clock driver. Since the definition of the clock buffer only allows the controller to WRITE data; the R/W# bit of the address will always be seen as ‘zero’. Optimal address decoding of this bit is left to the vendor.

2. **Options:** It is our understanding that metal mask options and other pinouts of this type of clock driver will be allowed to use the same address as the original CKBF device. I²C addresses are defined in terms of function (master clock driver) rather than form (pinout, and option).

3. **Slave/Receiver:** The clock driver is assumed to require only slave/receiver functionality. Slave/transmitter functionality is optional.

4. **Data Transfer Rate:** 100 kbits/s (standard mode) is the base functionality required. Fast mode (400 kbits/s) functionality is optional.

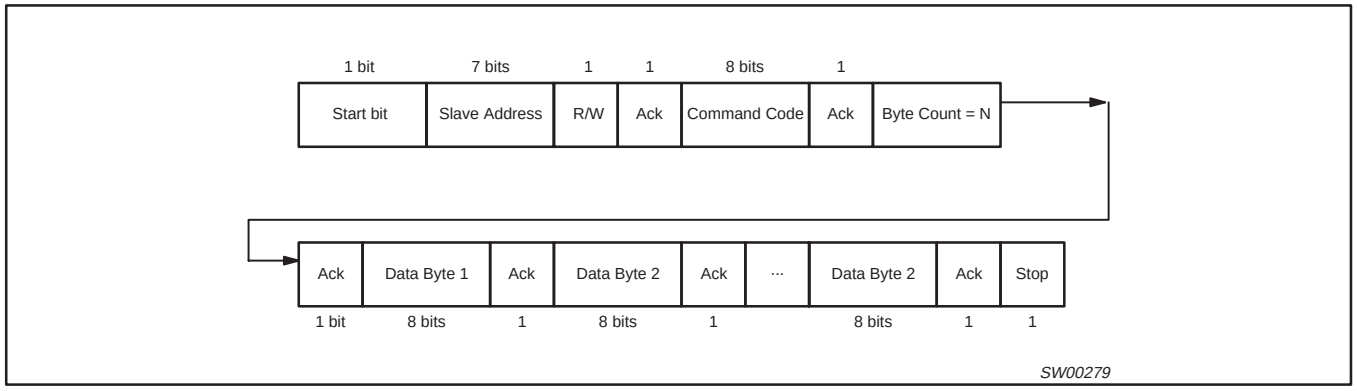
5. **Logic Levels:** I²C logic levels are based on a percentage of V_{DD} for the controller and other devices on the bus. Assume all devices are based on a 3.3 Volt supply.

6. **Data Byte Format:** Byte format is 8 Bits as described in the following appendices.

7. **Data Protocol:** To simplify the clock I²C interface, the clock driver serial protocol was specified to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed. However, the SMBus controller has a more specific format than the generic I²C protocol.

   The clock driver must meet this protocol which is more rigorous than previously stated I²C protocol. Treat the description from the viewpoint of controller. The controller “writes” to the clock driver and if possible would “read” from the clock driver (the clock driver is a slave/receiver only and is incapable of this transaction.)

   “The block write begins with a slave address and a write condition. After the command code the host (controller) issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to transfer a maximum of 32 data bytes.”



NOTE: The acknowledgement bit is returned by the slave/receiver (the clock driver).

Consider the command code and the byte count bytes required as the first two bytes of any transfer. The command code is software programmable via the controller, but will be specified as 0000 0000 in the clock specification. The byte count byte is the number of additional bytes required to transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement.

For example:

Byte count byte		Notes:
MSB	LSB	
0000	0000	Not allowed. Must have at least one byte.
0000	0001	Data for functional and frequency select register (currently byte 0 in spec)
0000	0010	Reads first two bytes of data. (byte 0 then byte 1)
0000	0011	Reads first three bytes (byte 0, 1, 2 in order)
0000	0100	Reads first four bytes (byte 0, 1, 2, 3 in order)
0000	0101	Reads first five bytes (byte 0, 1, 2, 3, 4 in order)
0000	0110	Reads first six bytes (byte 0, 1, 2, 3, 4, 5 in order)
0000	0111	Reads first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order)
0010	0000	Max byte count supported = 32

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The serial controller interface can be simplified by discarding the information in both the command code and the byte count bytes and simply reading all the bytes that are sent to the clock driver after being addressed by the controller. It is expected that the controller will not provide more bytes than the clock driver can handle. A clock vendor may choose to discard any number of bytes that exceed the defined byte count.

8. **Clock stretching:** The clock device must not hold/stretch the SCLOCK or SDATA lines low for more than 10 mS. Clock stretching is discouraged and should only be used as a last resort. Stretching the clock/data lines for longer than this time puts the device in an error/time-out mode and may not be supported in all platforms. It is assumed that all data transfers can be completed as specified without the use of clock/data stretching.
9. **General Call:** It is assumed that the clock driver will not have to respond to the “general call.”
10. **Electrical Characteristics:** All electrical characteristics must meet the standard mode specifications found in section 15 of the I²C specification.

a. **Pull-Up Resistors:** Any internal resistors pull-ups on the SDATA and SCLOCK inputs must be stated in the individual data sheet. The use of internal pull-ups on these pins of below 100 kΩ is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5 to 6 kΩ range. Assume one I²C device per DIMM (serial presence detect), one I²C controller, one clock driver plus one/two more I²C devices on the platform for capacitive loading purposes.

b. **Input Glitch Filters:** Only fast mode I²C devices require input glitch filters to suppress bus noise. The clock driver is specified as a standard mode device and is not required to support this feature.

11. **PWR DWN#:** If a clock driver is placed in PWR DWN# mode, the SDATA and SCLK inputs must be 3-Stated and the device must retain all programming information. I_{DD} current due to the I²C circuitry must be characterized and in the data sheet.

For specific I²C information consult the *Philips I²C Peripherals Data Handbook IC12 (1997).*

SERIAL CONFIGURATION MAP

The serial bits will be read by the clock buffer in the following order:

Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 2 – Bits 7, 6, 5, 4, 3, 2, 1, 0

All unused register bits (Reserved and N/A) should be defined as “Don’t Care”. It is expected that the controller will force all of these bits to a “0” level.

All register bits labeled “Initialize to 0” must be written to zero during initialization. Failure to do so may result in a higher than normal operating current. The controller will read back the last written value.

Byte 0: Output active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	DESCRIPTION
7	18	BUF_OUT7	Active/Inactive
6	17	BUF_OUT6	Active/Inactive
5	14	BUF_OUT5	Active/Inactive
4	13	BUF_OUT4	Active/Inactive
3	9	BUF_OUT3	Active/Inactive
2	8	BUF_OUT2	Active/Inactive
1	5	BUF_OUT1	Active/Inactive
0	4	BUF_OUT0	Active/Inactive

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 1: Output active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	DESCRIPTION
7	45	BUF_OUT15	Active/Inactive
6	44	BUF_OUT14	Active/Inactive
5	41	BUF_OUT13	Active/Inactive
4	40	BUF_OUT12	Active/Inactive
3	36	BUF_OUT11	Active/Inactive
2	35	BUF_OUT10	Active/Inactive
1	32	BUF_OUT9	Active/Inactive
0	31	BUF_OUT8	Active/Inactive

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 2: Optional register for possible future requirements

BIT	PIN#	NAME	DESCRIPTION
7	28	BUF_OUT17	Active/Inactive
6	21	BUF_OUT16	Active/Inactive
5	—	(reserved)	(reserved)
4	—	(reserved)	(reserved)
3	—	(reserved)	(reserved)
2	—	(reserved)	(reserved)
1	—	(reserved)	(reserved)
0	—	(reserved)	(reserved)

NOTE:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

AC WAVEFORMS

V_M = 1.5 V
$V_X = V_{OL}$ + 0.3 V
$V_Y = V_{OH}$ – 0.3 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

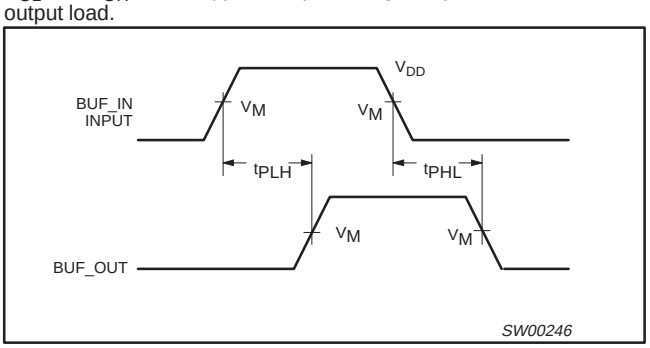


Figure 1. Load circuitry for switching times.

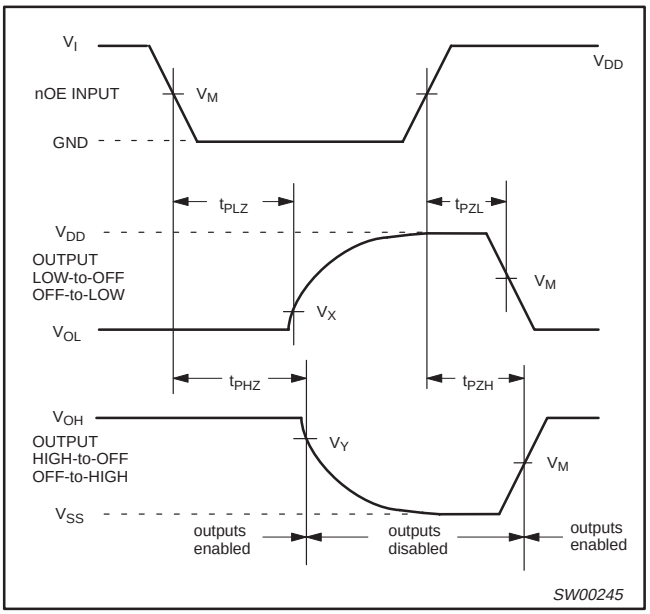


Figure 2. 3-State enable and disable times

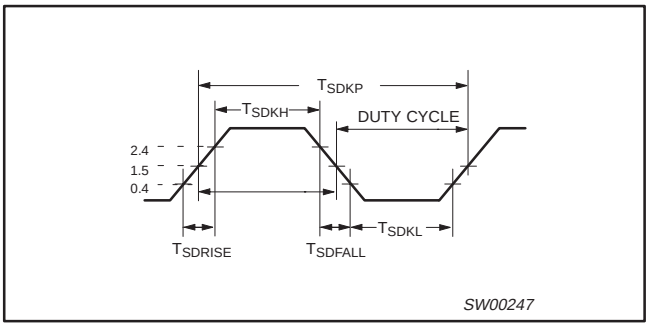


Figure 3. Buffer Output clock

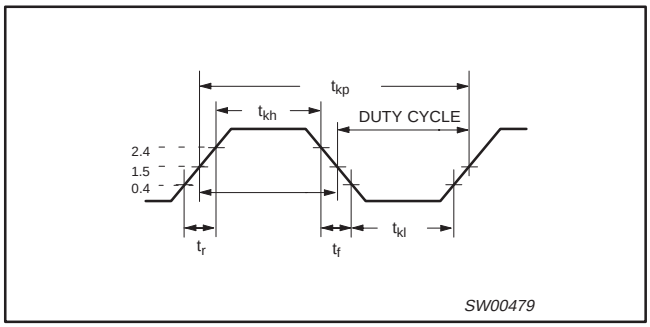


Figure 4. SDRAM Output clock

TEST CIRCUIT

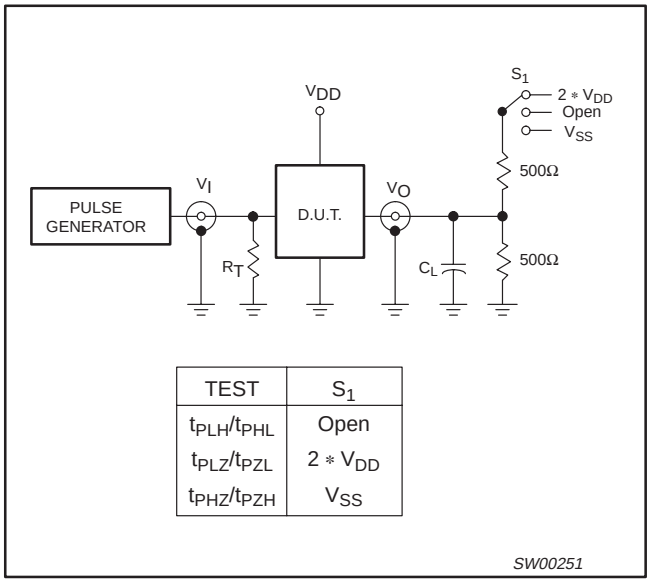
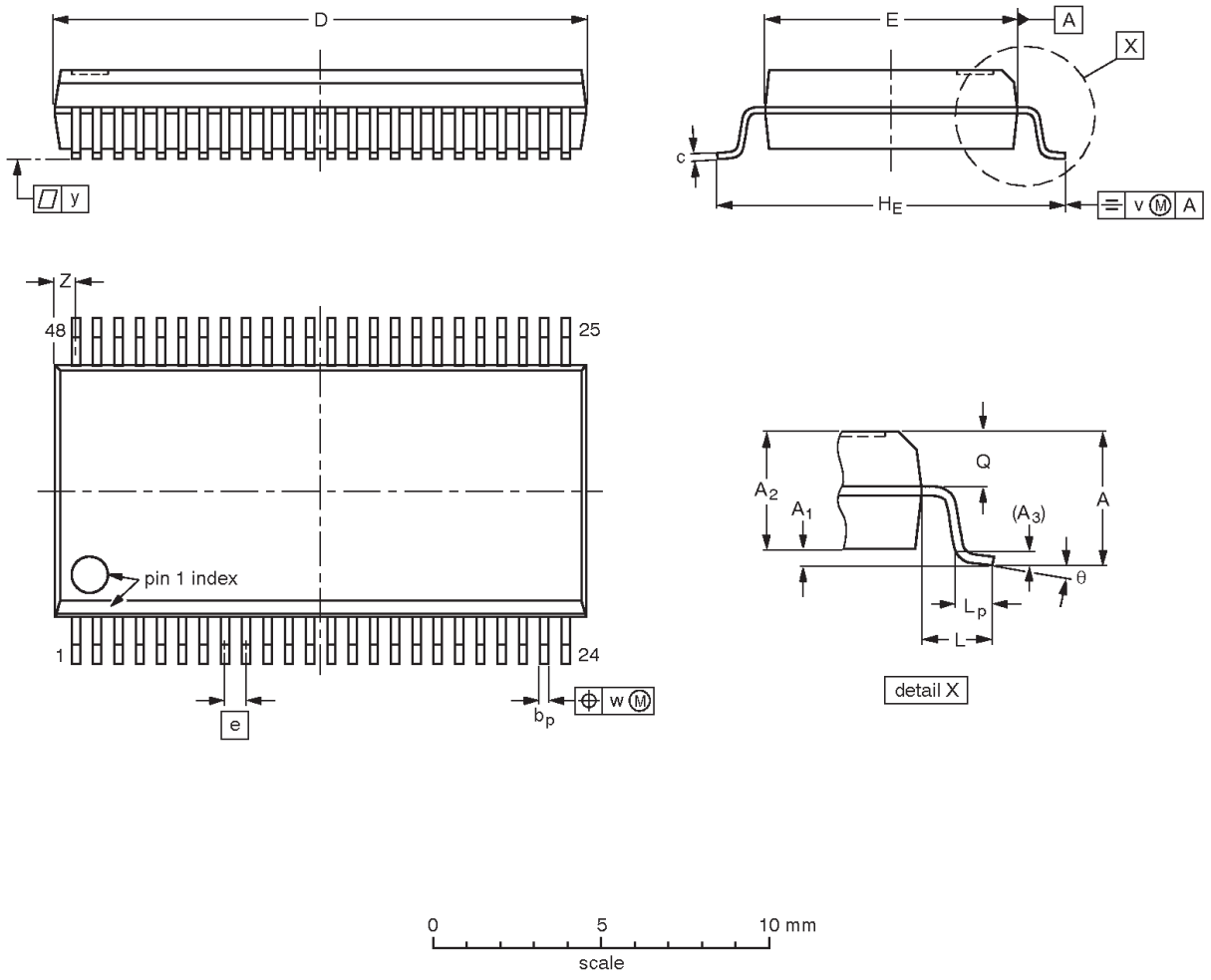


Figure 5. Load circuitry for switching times

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118				~~95-02-04~~ 99-12-27

NOTES

14.318–150 MHz I²C 1:18 clock buffer PCK2001

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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