# PHD101NQ03LT

## N-channel TrenchMOS logic level FET

Rev. 04 — 9 June 2009 Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC convertors

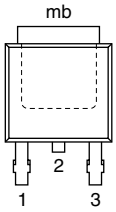
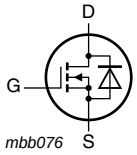
### 1.4 Quick reference data

**Table 1. Quick reference**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | - | - | 30 | V |
| $I_D$ | drain current | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see Figure 1; see Figure 3 | - | - | 75 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; see Figure 2 | - | - | 166 | W |
| **Dynamic characteristics** | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS}$ = 5 V; $I_D$ = 50 A; $V_{DS}$ = 15 V; $T_j$ = 25 °C; see Figure 11 | - | 8 | - | nC |
| **Static characteristics** | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 9; see Figure 10 | - | 4.5 | 5.5 | mΩ |

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | | Simplified outline | Graphic symbol |
|---|---|---|---|---|---|
| 1 | G | gate | |   **SOT428 (SC-63; DPAK)** |   |
| 2 | D | drain | [1] | | |
| 3 | S | source | | | |
| mb | D | mounting base; connected to drain | | | |

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

**Table 3. Ordering information**

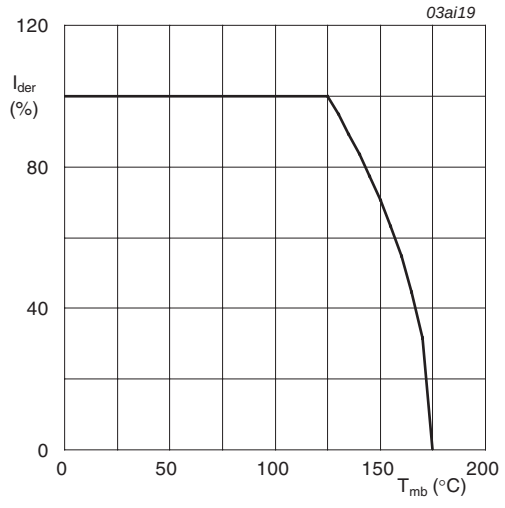
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PHD101NQ03LT | SC-63; DPAK | plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) | SOT428 |

# 4. Limiting values

**Table 4. Limiting values**

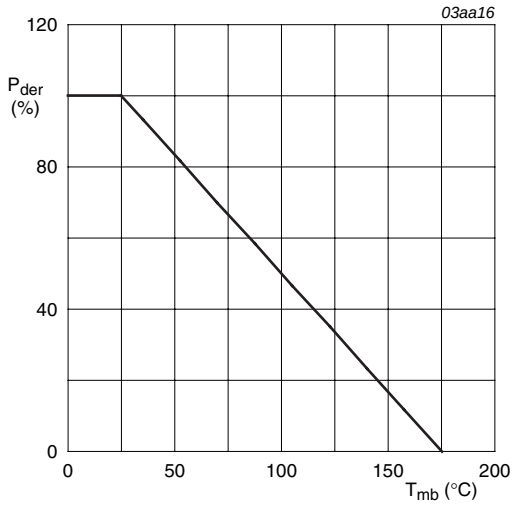
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | - | 30 | V |
| $V_{DGR}$ | drain-gate voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C; $R_{GS}$ = 20 kΩ | - | 30 | V |
| $V_{GS}$ | gate-source voltage | | -20 | 20 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; see Figure 1 | - | 75 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; see Figure 1; see Figure 3 | - | 75 | A |
| $I_{DM}$ | peak drain current | $t_p \leq 10$ µs; pulsed; $T_{mb}$ = 25 °C; see Figure 3 | - | 240 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; see Figure 2 | - | 166 | W |
| $T_{stg}$ | storage temperature | | -55 | 175 | °C |
| $T_j$ | junction temperature | | -55 | 175 | °C |
| $V_{GSM}$ | peak gate-source voltage | pulsed; δ = 25 %; $t_p \leq 50$ µs | -25 | 25 | V |
| **Source-drain diode** | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | - | 75 | A |
| $I_{SM}$ | peak source current | $t_p \leq 10$ µs; pulsed; $T_{mb}$ = 25 °C | - | 240 | A |
| **Avalanche ruggedness** | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 43 A; $V_{sup} \leq 15$ V; unclamped; $t_p$ = 0.19 ms; $R_{GS}$ = 50 Ω | - | 185 | mJ |



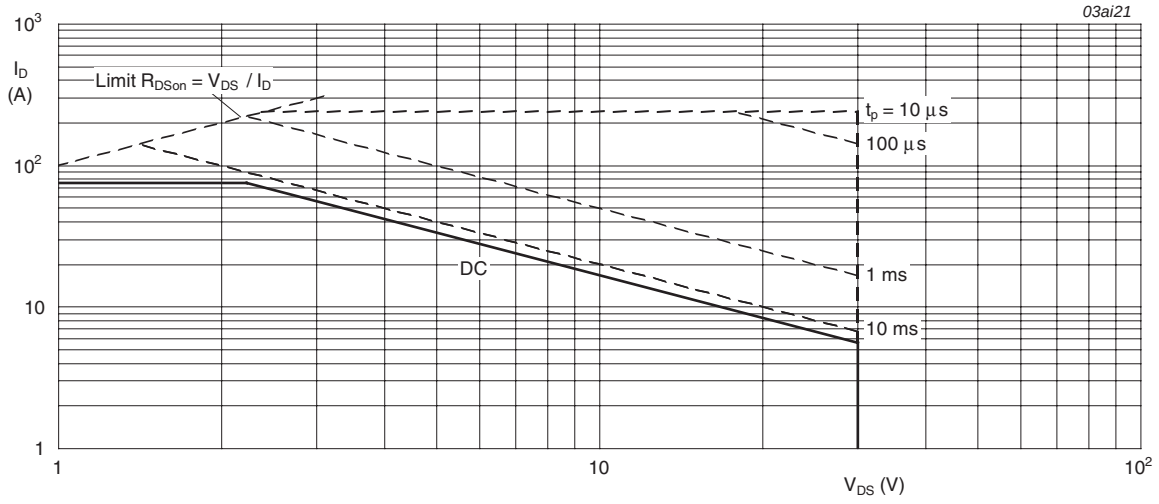

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**




$T_{mb} = 25°C; I_{DM}$ is single pulse; $V_{GS} = 10V$

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | | - | - | 0.9 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | minimum footprint | [1] | - | 75 | - | K/W |
| | | SOT404 minimum footprint | [1] | - | 50 | - | K/W |

[1] Mounted on a printed-cirquit board; vertical in still air.

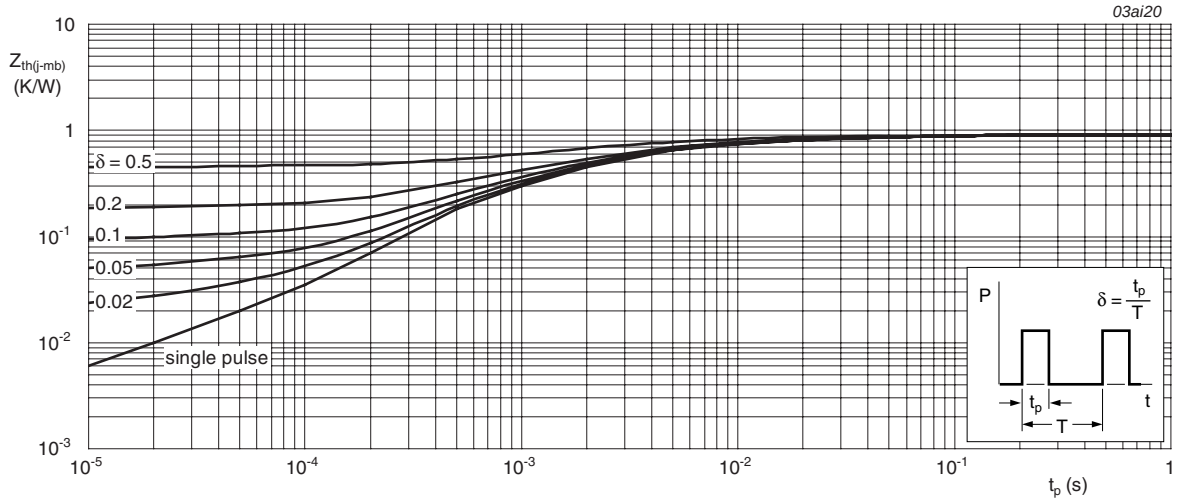
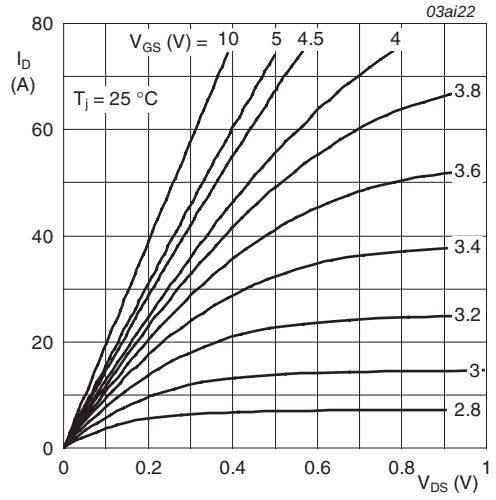



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

# 6. Characteristics

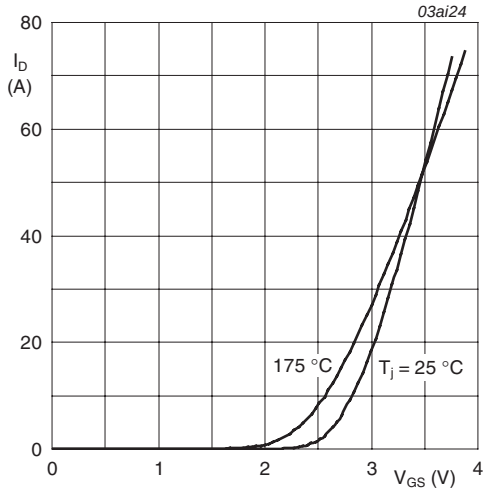
**Table 6. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | 27 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | 30 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 175 °C; see Figure 7; see Figure 8 | 0.6 | - | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; see Figure 7; see Figure 8 | - | - | 2.9 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 7; see Figure 8 | 1 | 1.9 | 2.5 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | 0.05 | 1 | µA |
| | | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | - | - | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 10 | 100 | nA |
| | | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 10 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 9; see Figure 10 | - | 4.5 | 5.5 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 175 °C; see Figure 9; see Figure 10 | - | 10.5 | 13.5 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 9; see Figure 10 | - | 5.8 | 7.5 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 50 A; $V_{DS}$ = 15 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; see Figure 11 | - | 23 | - | nC |
| $Q_{GS}$ | gate-source charge | | - | 10.5 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 8 | - | nC |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; see Figure 12 | - | 2180 | - | pF |
| $C_{oss}$ | output capacitance | | - | 600 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 225 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 15 V; $R_L$ = 0.6 Ω; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 5.6 Ω; $T_j$ = 25 °C; $I_D$ = 25 A | - | 23 | - | ns |
| $t_r$ | rise time | | - | 90 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 37 | - | ns |
| $t_f$ | fall time | | - | 33 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; see Figure 13 | - | 0.85 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 10 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; $T_j$ = 25 °C | - | 37 | - | ns |
| $Q_r$ | recovered charge | | - | 33 | - | nC |



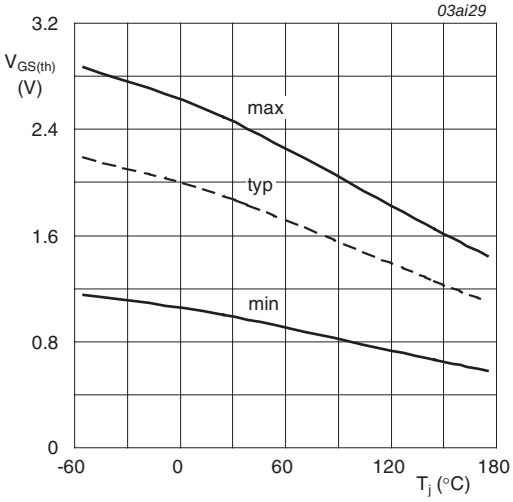

$T_j = 25°C$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



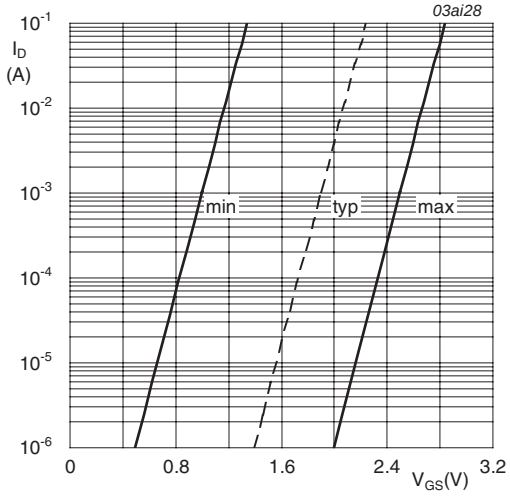

$T_j = 25°C \text{ and } 175°C; V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



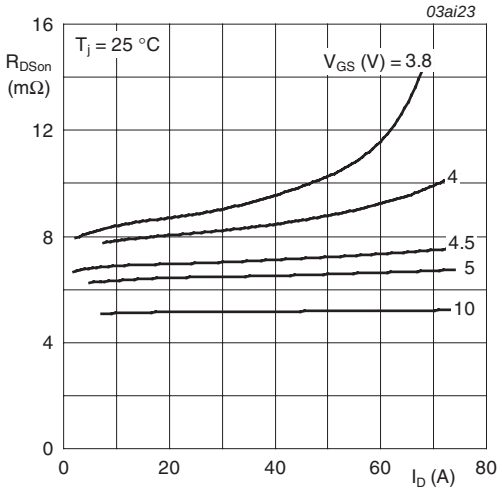

$I_D = 1mA; V_{DS} = V_{GS}$

**Fig 7. Gate-source threshold voltage as a function of junction temperature**



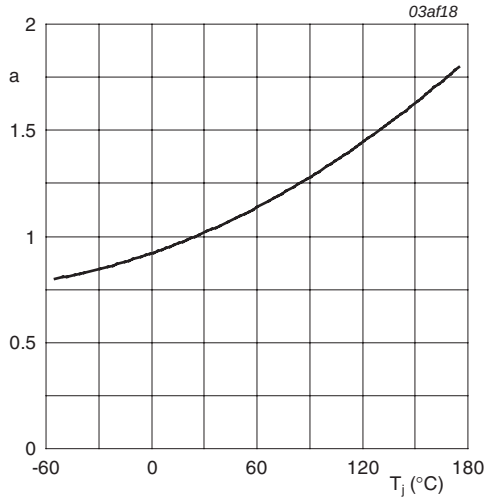

$T_j = 25°C; V_{DS} = 5V$

**Fig 8. Sub-threshold drain current as a function of gate-source voltage**



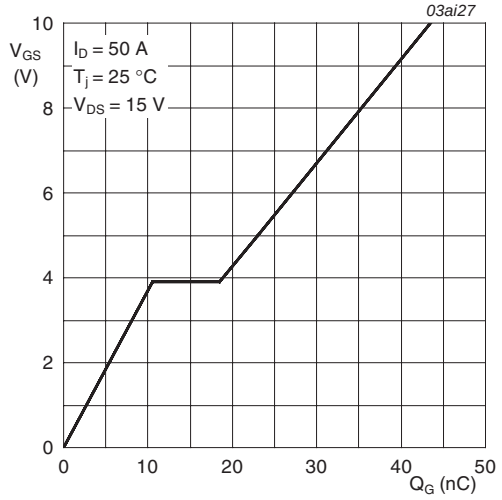

$T_j = 25°C$

**Fig 9. Drain-source on-state resistance as a function of drain current; typical values**



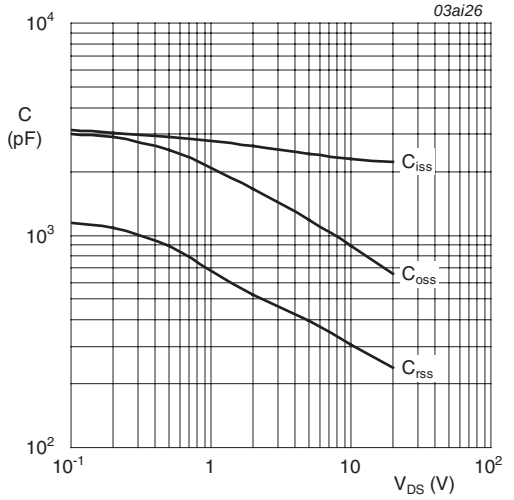

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature**



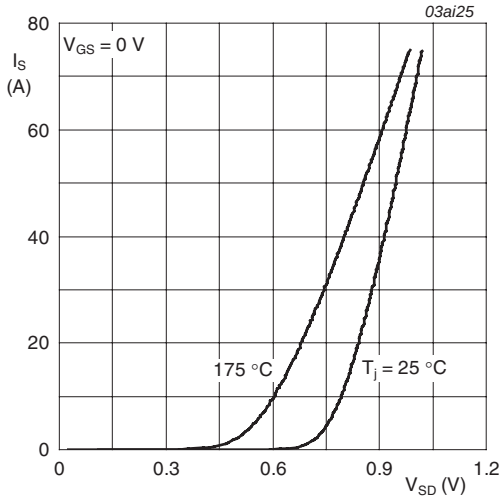

$I_D = 50A; V_{DS} = 15V$

**Fig 11. Gate-source voltage as a function of gate charge; typical values**




$V_{GS} = 0V; f = 1MHz$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

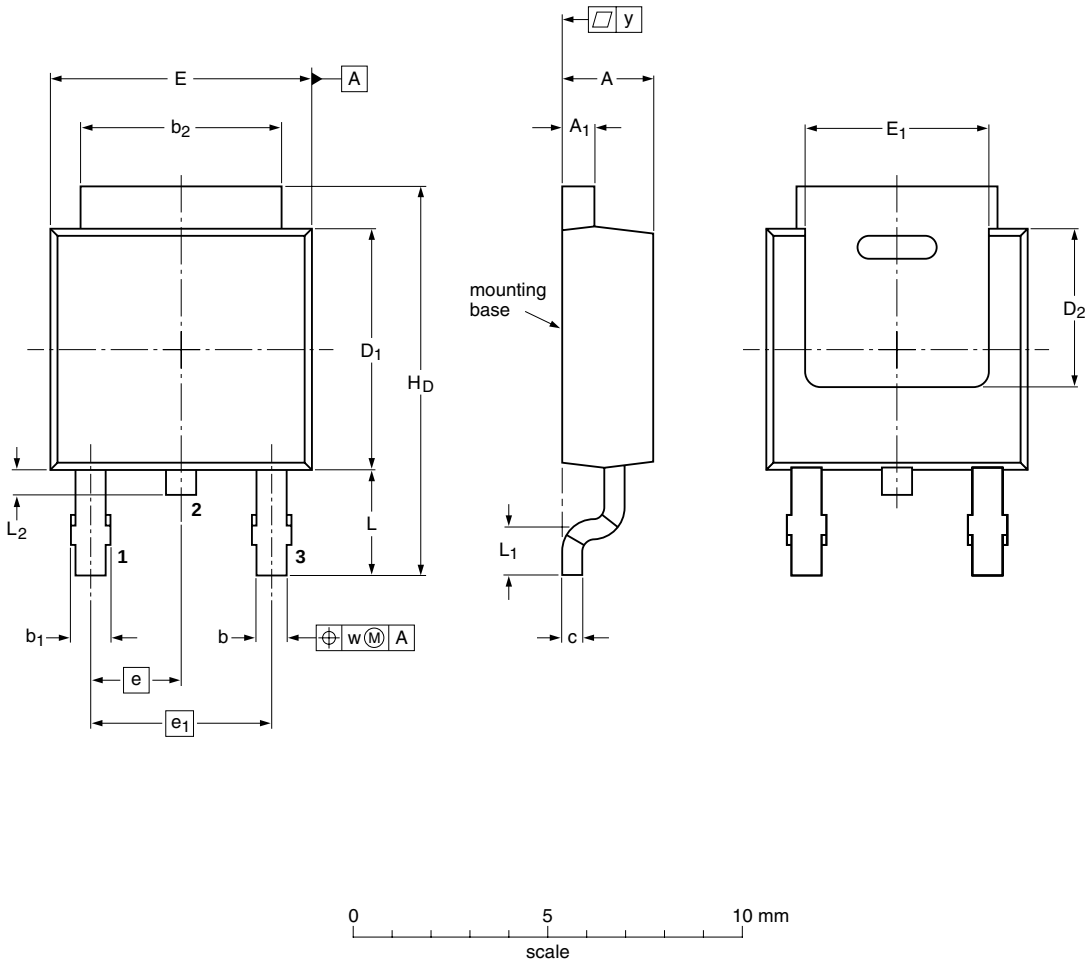



$T_j = 25°C \text{ and } 175°C; V_{GS} = 0V$

**Fig 13. Source current as a function of source-drain voltage; typical values**

## 7. Package outline

**Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)** **SOT428**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | $b_2$ | c | $D_1$ | $D_2$ min | E | $E_1$ min | e | $e_1$ | $H_D$ | L | $L_1$ min | $L_2$ | w | y max |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.38<br>2.22 | 0.93<br>0.46 | 0.89<br>0.71 | 1.1<br>0.9 | 5.46<br>5.00 | 0.56<br>0.20 | 6.22<br>5.98 | 4.0 | 6.73<br>6.47 | 4.45 | 2.285 | 4.57 | 10.4<br>9.6 | 2.95<br>2.55 | 0.5 | 0.9<br>0.5 | 0.2 | 0.2 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT428 | | TO-252 | SC-63 | | | ~~06-02-14~~<br>06-03-16 |

**Fig 14. Package outline SOT428 (DPAK)**

## 8. Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PHD101NQ03LT_4 | 20090609 | Product data sheet | - | PHD101NQ03LT_3 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| PHD101NQ03LT_3 | 20051206 | Product data sheet | CPCN # 200309016 | PHB_PHD101NQ03LT-02 |
| PHB_PHD101NQ03LT-02 (9397 750 10929) | 20030225 | Product data | - | PHB_PHD_PHP101NQ03LT-01 |
| PHB_PHD_PHP101NQ03LT-01 (9397 750 09307) | 20020220 | Product data | - | - |

# 9. Legal information

## 9.1 Data sheet status

| Document status [1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 9.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

## 9.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

## 9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**TrenchMOS** — is a trademark of NXP B.V.

# 10. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

## 11. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 9 June 2009**
**Document identifier: PHD101NQ03LT_4**