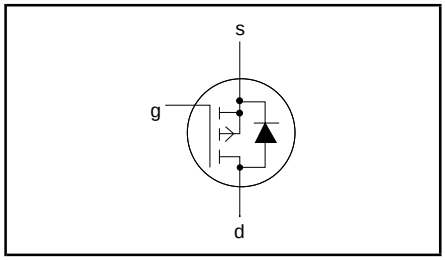
P-channel enhancement mode MOS transistor

PHK04P02T

FEATURES

- Very low threshold voltage
- Fast switching
- Logic level compatible
- Surface mount package

SYMBOL



QUICK REFERENCE DATA

V_{DS} = -16 V

I_D = -4.66 A

$R_{DS(ON)} \leq 0.15\ \Omega$ (V_{GS} = -2.5 V)

$V_{GS(TO)} \geq 0.4$ V

GENERAL DESCRIPTION

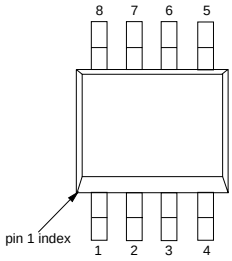
P-channel, enhancement mode, logic level, field-effect power transistor. This device has low threshold voltage and extremely fast switching making it ideal for battery powered applications and high speed digital interfacing.

The PHK04P02T is supplied in the SOT96-1 (SO8) surface mounting package.

PINNING

PIN	DESCRIPTION
1,2,3	source
4	gate
5,6,7,8	drain

SOT96-1



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	-16	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	-16	V
V_{GS}	Gate-source voltage		-	± 8	V
I_D	Drain current (DC)	T_{sp} = 25 ˚C	-	-4.66	A
		T_{sp} = 100 ˚C	-	-1.87	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 ˚C	-	-26.4	A
P_{tot}	Total power dissipation	T_{sp} = 25 ˚C	-	5.0	W
		T_{sp} = 100 ˚C	-	2.0	W
T_{stg}, T_j	Storage & operating temperature		- 55	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point	mounted on metal clad substrate.	25	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = -10 µA	-16	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = -1 mA	-0.4	-0.6	-	V
		T_j = 150˚C	-0.1	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -1 A	-	80	120	mΩ
		V_{GS} = -2.5 V; I_D = -1 A	-	117	150	mΩ
		V_{GS} = -1.8 V; I_D = -0.5 A	-	140	180	mΩ
		V_{GS} = -2.5 V; I_D = -1 A; T_j = 150˚C	-	175	230	mΩ
g_{fs}	Forward transconductance	V_{DS} = -12.8 V; I_D = -1 A	1.5	4.5	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±8 V; V_{DS} = 0 V	-	±10	±100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = -12.8 V; V_{GS} = 0 V;	-	-50	-100	nA
		T_j = 150˚C	-	-13	-100	µA
$Q_{g(tot)}$	Total gate charge	I_D = -1 A; V_{DD} = -10 V; V_{GS} = -4.5 V	-	7.2	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	1.83	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = -10 V; I_D = -1 A;	-	2	-	ns
t_r	Turn-on rise time	V_{GS} = -8 V; R_G = 6 Ω	-	4.5	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	45	-	ns
t_f	Turn-off fall time		-	20	-	ns
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = -12.8 V; f = 1 MHz	-	528	-	pF
C_{oss}	Output capacitance		-	200	-	pF
C_{rss}	Feedback capacitance		-	57	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{sp} = 25 ˚C, t ≤ 5 s	-	-	-4.66	A
I_{DRM}	Pulsed reverse drain current		-	-	-26	A
V_{SD}	Diode forward voltage	I_F = -0.62 A; V_{GS} = 0 V	-	-0.62	-1.3	V
t_{rr}	Reverse recovery time	I_F = -0.5 A; -dI_F/dt = 100 A/µs;	-	75	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = -12.8 V	-	69	-	nC

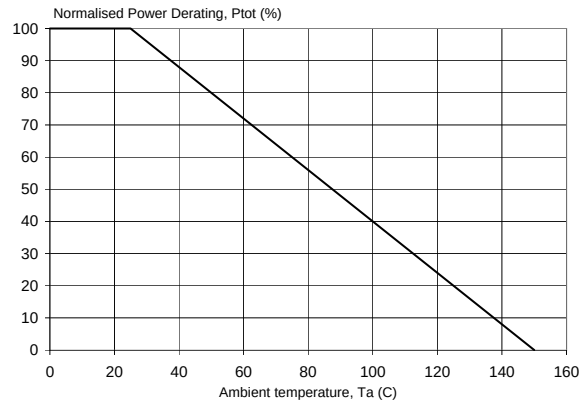


Fig.1. Normalised power dissipation. PD% = 100·P_D/$P_{D\ 25\ ^\circ C}$ = f(T_a)

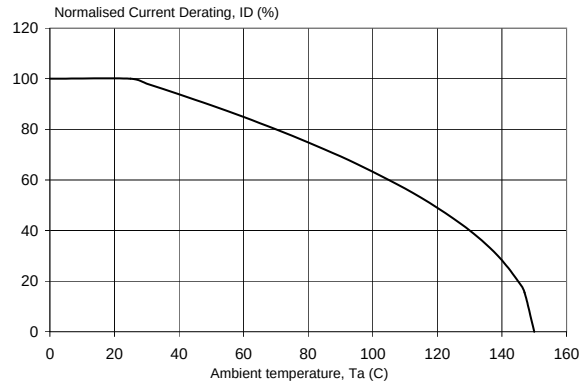


Fig.2. Normalised continuous drain current. ID% = 100·I_D/$I_{D\ 25\ ^\circ C}$ = f(T_a); conditions: V_{GS} ≤ -10 V

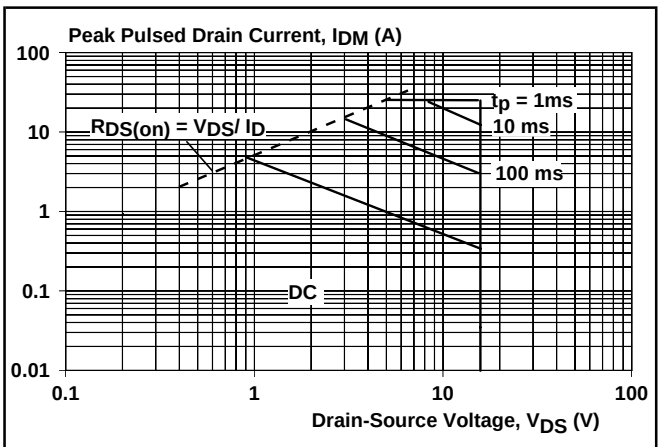


Fig.3. Safe operating area. T_{sp} = 25 ˚C; I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p.

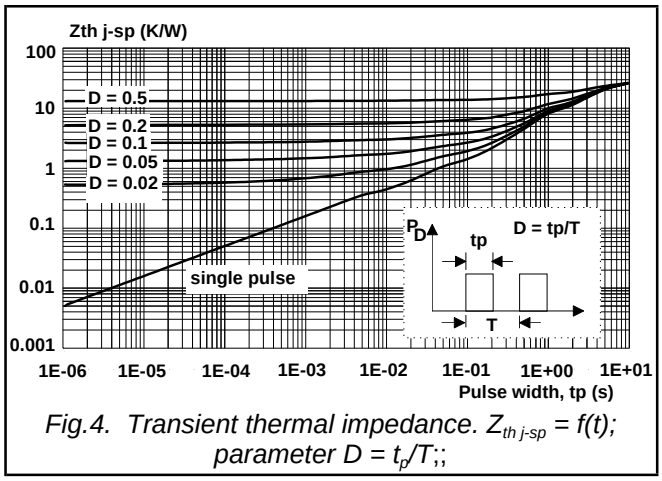


Fig.4. Transient thermal impedance. $Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T;;

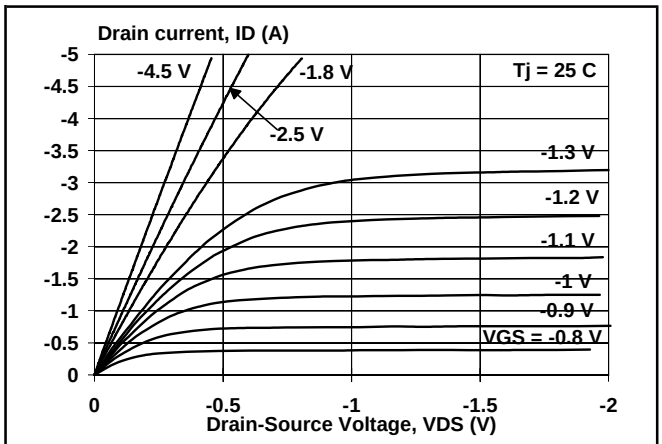


Fig.5. Typical output characteristics, T_j = 25 ˚C. I_D = f(V_{DS}); parameter V_{GS}

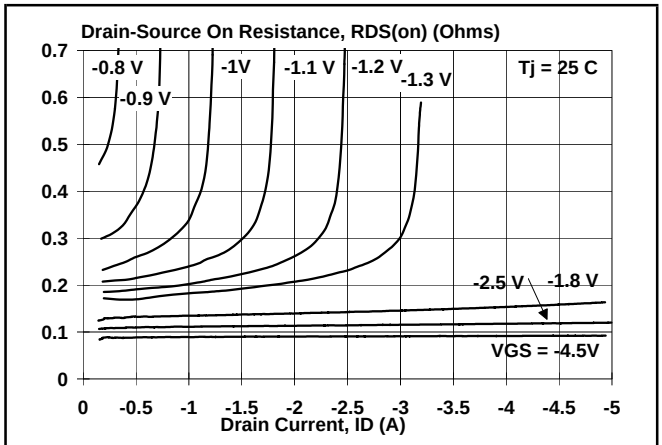


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)}$ = f(I_D); parameter V_{GS}

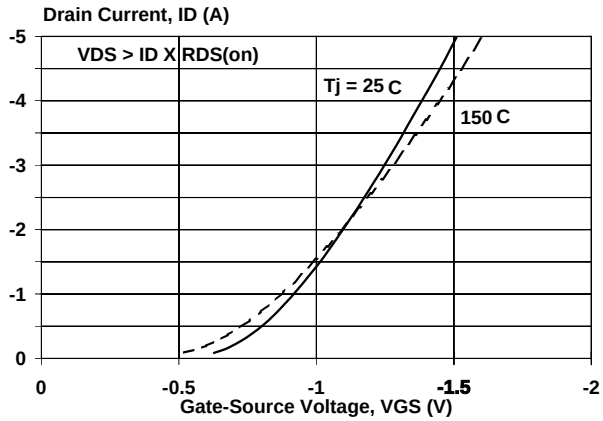


Fig.7. Typical transfer characteristics; $I_D = f(V_{GS})$

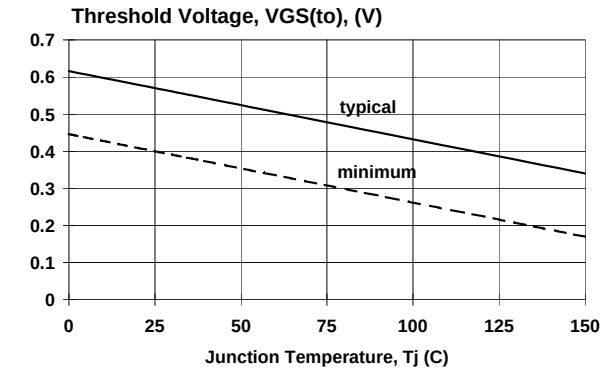


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

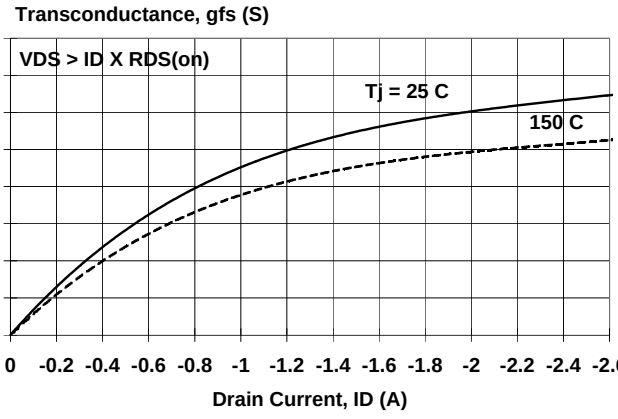


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$

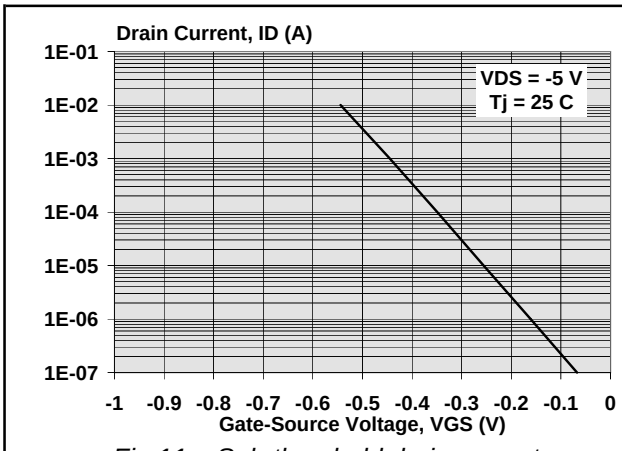


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 ˚C

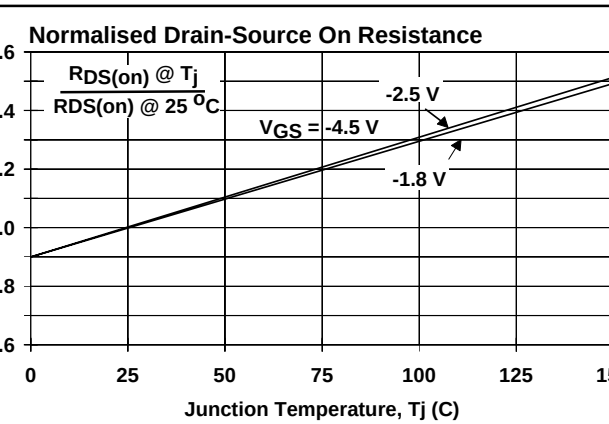


Fig.9. Normalised drain-source on-state resistance. $R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$

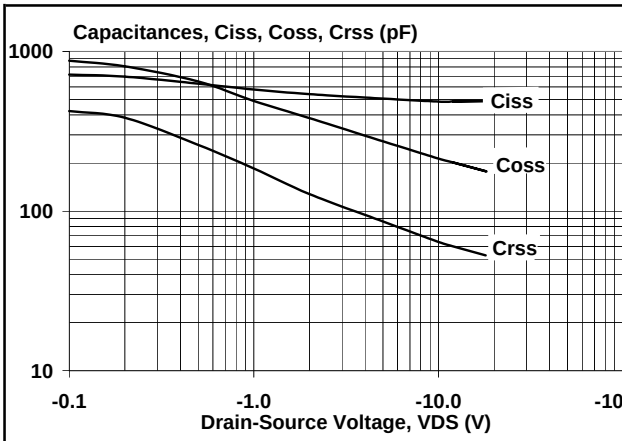


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

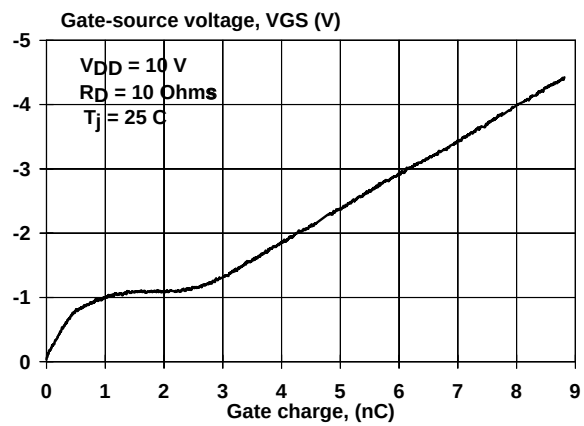


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$

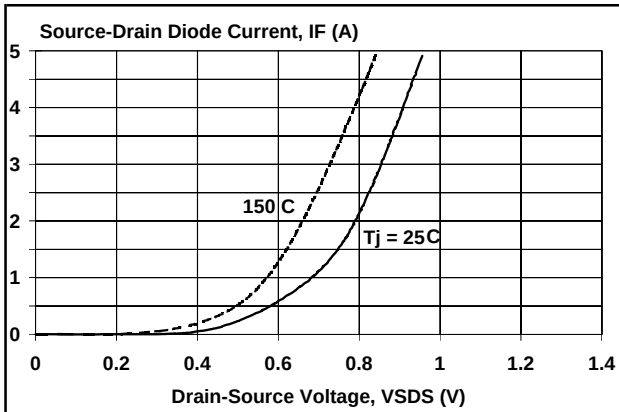
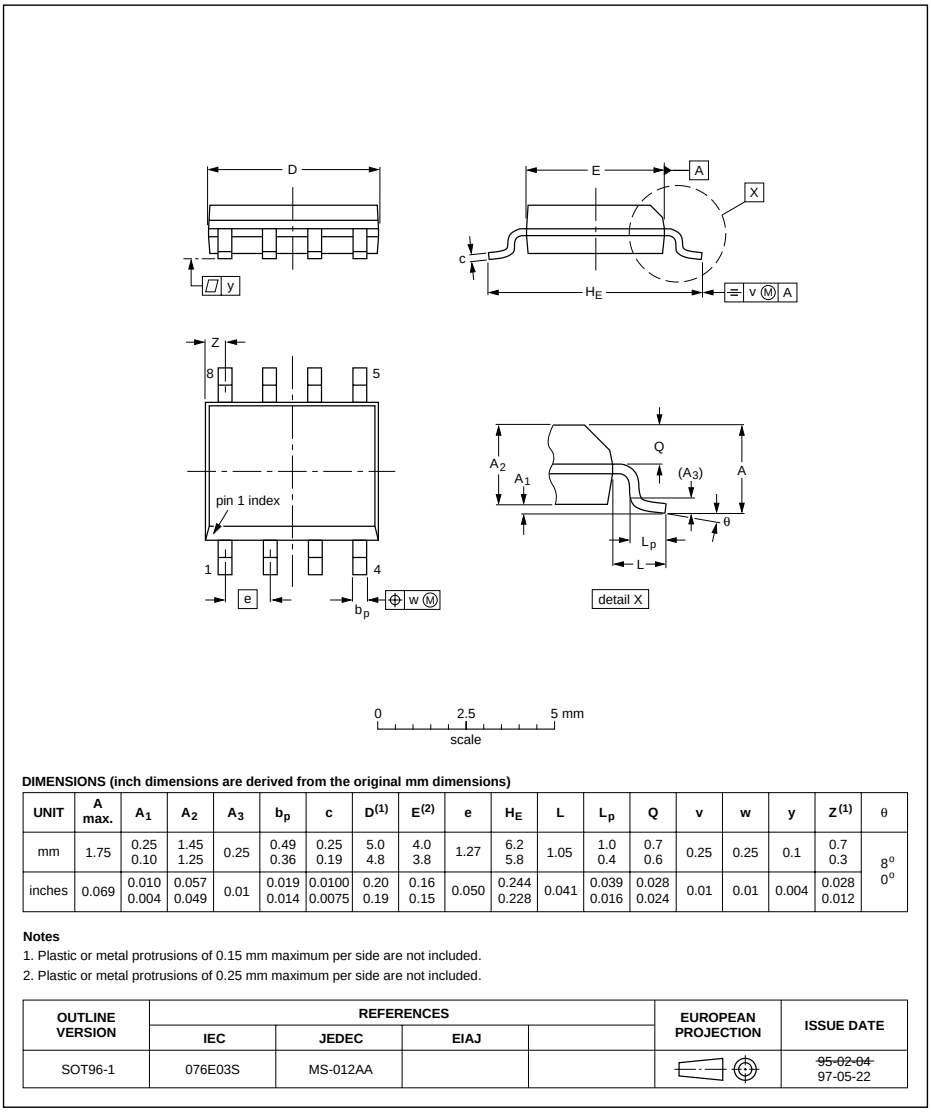


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

MECHANICAL DATA

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Fig.15. SOT96 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS[1]	**PRODUCT STATUS**[2]	**DEFINITIONS**
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A
Limiting values		
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

1 Please consult the most recently issued datasheet before initiating or completing a design.

2 The product status of the device(s) described in this datasheet may have changed since this datasheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.