SAA7102; SAA7103

Digital video encoder

Rev. 04 — 18 January 2006 Product data sheet

1. General description

The SAA7102; SAA7103 is used to encode PC graphics data at maximum 800 × 600 resolution to PAL (50 Hz) or NTSC (60 Hz) video signals. A programmable scaler and interlacer ensures properly sized and flicker-free TV display as CVBS or S-video output.

Alternatively, the three Digital-to-Analog Converters (DACs) can output RGB signals together with a TTL composite sync to feed SCART connectors.

When the scaler/interlacer is bypassed, a second VGA monitor can be connected to the RGB outputs and separate H and V-syncs as well, thereby serving as an auxiliary monitor at maximum 800 × 600 resolution/60 Hz (PIXCLK < 45 MHz).

The device includes a sync/clock generator and on-chip DACs.

2. Features

- Digital PAL/NTSC encoder with integrated high quality scaler and anti-flicker filter for TV output from a PC
- 27 MHz crystal-stable subcarrier generation
- Maximum graphics pixel clock 45 MHz at double edged clocking, synthesized on-chip or from external source
- Up to 800 × 600 graphics data at 60 Hz or 50 Hz with programmable underscan range.
- Three Digital-to-Analog Converters (DACs) at 27 MHz sample rate for CVBS (BLUE, C_B), VBS (GREEN, CVBS) and C (RED, C_R) (signals in parenthesis are optional); all at 10-bit resolution
- Non-Interlaced (NI) C_B-Y-C_R or RGB input at maximum 4 : 4 : 4 sampling
- Downscaling from 1 : 1 to 1 : 2 and up to 20 % upscaling
- Optional interlaced C_B-Y-C_R input of Digital Versatile Disc (DVD) signals
- Optional non-interlaced RGB output to drive second VGA monitor (bypass mode with maximum 45 MHz)
- 3 × 256 bytes RGB Look-Up Table (LUT)
- Support for hardware cursor
- Programmable border color of underscan area
- On-chip 27 MHz crystal oscillator (3rd-harmonic or fundamental 27 MHz crystal)
- Fast I^2C-bus control port (400 kHz)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Color Bar Generator (CBG)
- Optional support of various Vertical Blanking Interval (VBI) data insertion

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- Macrovision Pay-per-View copy protection system rev. 7.01 and rev. 6.1 as option; this applies to the SAA7102 only
- Power-save modes
- Joint Test Action Group (JTAG) Boundary Scan Test (BST)
- Monolithic CMOS 3.3 V device, 5 V tolerant I/Os
- QFP44 and LBGA156 packages
- Same footprint as SAA7108E; SAA7109E

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDA}	analog supply current		1	110	140	mA
I_{DDD}	digital supply current		1	70	90	mA
V_i	input signal voltage levels		TTL compatible			
$V_{o(p-p)}$	analog CVBS output signal voltage for a 100/100 color bar at 75/2 Ω load (peak-to-peak value)		-	1.23	-	V
R_L	load resistance		-	37.5	-	Ω
$ILE_{lf(DAC)}$	low frequency integral linearity error of DACs		-	-	±3	LSB
$DLE_{lf(DAC)}$	low frequency differential linearity error of DACs		-	-	±1	LSB
T_{amb}	ambient temperature		0	-	70	°C

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
SAA7102E	LBGA156	plastic low profile ball grid array package; 156 balls; body 15 × 15 × 1.05 mm	SOT700-1
SAA7103E			
SAA7102H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
SAA7103H			

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5. Block diagram

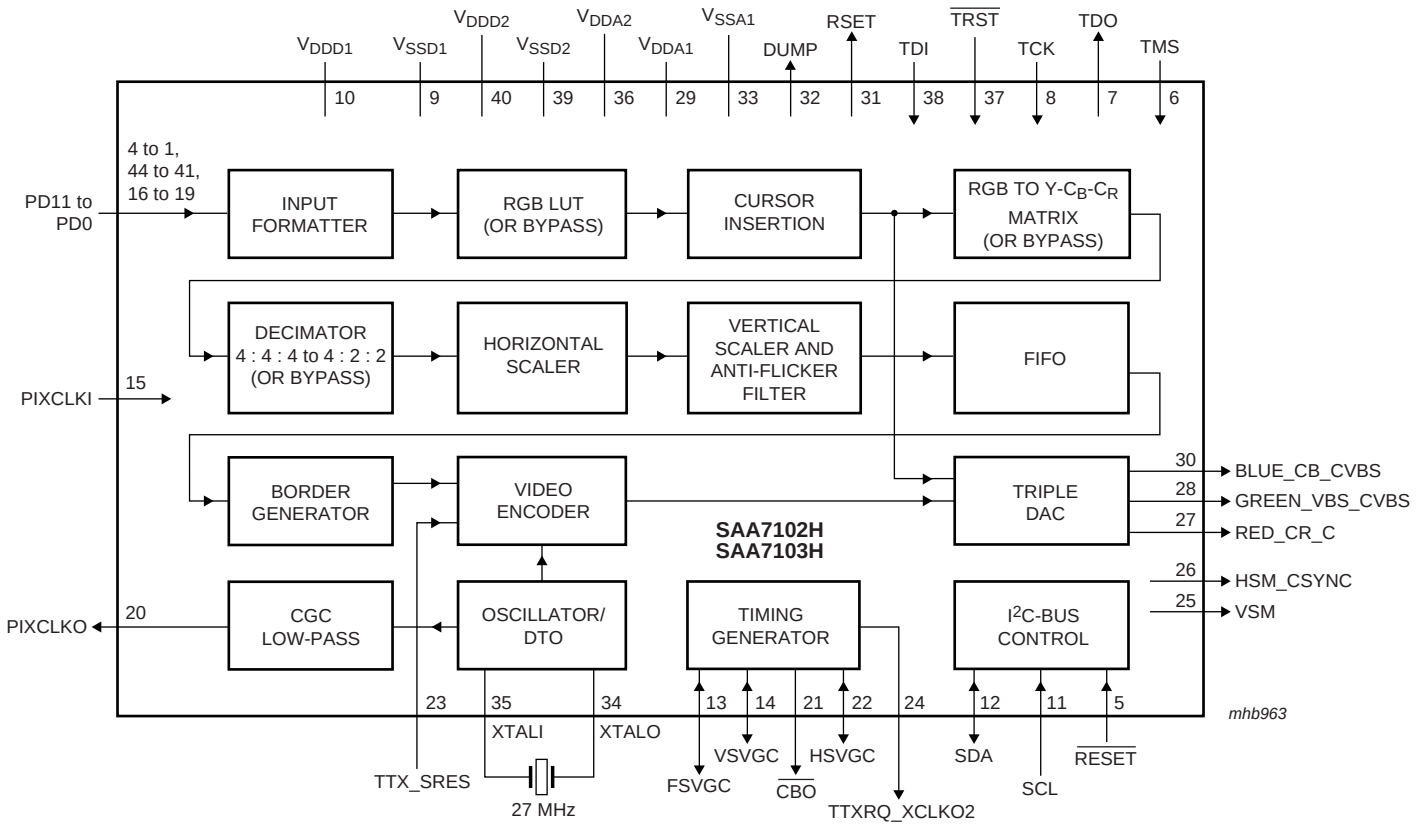

Fig 1. Block diagram (SAA7102H and SAA7103H)

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6. Pinning information

6.1 Pinning

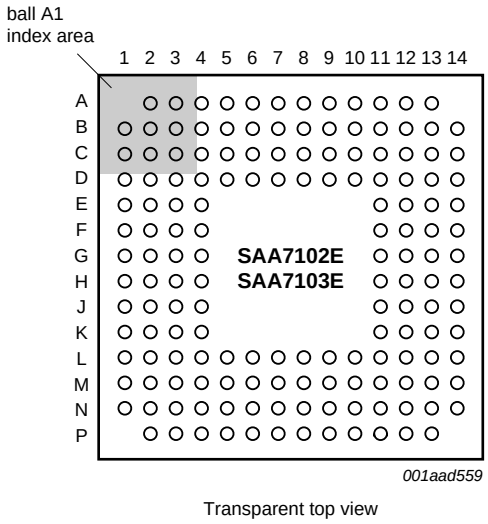

Fig 2. Pin configuration (LBGA156)

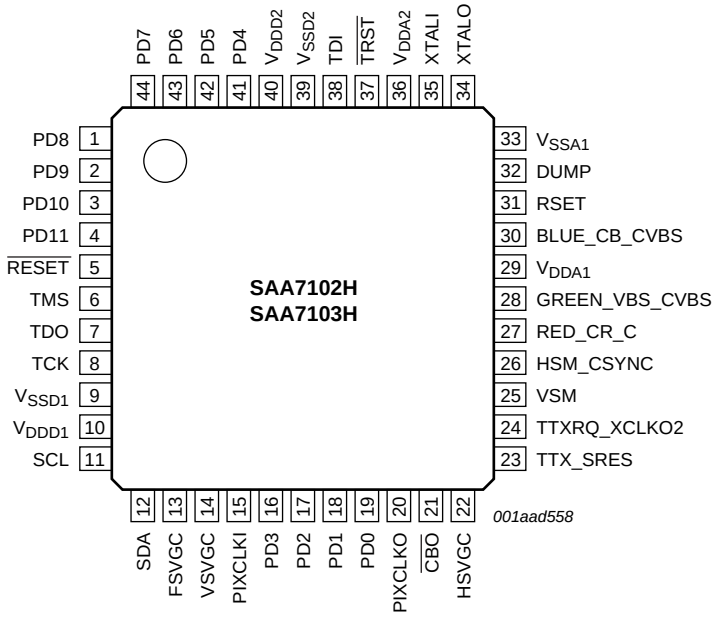

Fig 3. Pin configuration (QFP44)

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Table 3: Pin allocation table SAA7102E; SAA7103E

Pin	Symbol	Pin	Symbol
A2	PD7	A3	PD4
A4	$\overline{TRST}$	A5	XTALI
A6	XTALO	A7	DUMP
A8	V_{SSA1}	A9	RSET
A10	V_{DDA1}	B1	PD9
B2	PD8	B3	PD5
B4	PD6	B5	TDI
B6	V_{DDA2}	B7	DUMP
B8	V_{SSA1}	B9	V_{DDA1}
C1	PD11	C2	PD10
C3	TTX_SRES	C4	TTXRQ_XCLKO2
C5	V_{SSD2}	C6	BLUE_CB_CVBS
C7	GREEN_VBS_CVBS	C8	RED_CR_C
C9	V_{DDA1}	D1	TDO
D2	$\overline{RESET}$	D3	TMS
D4	V_{DDD2}	D5	V_{SSD2}
D6	V_{DDA2}	D7	VSM
D8	HSM_CSYNC	D9	V_{DDA1}
E1	TCK	E2	SCL
E3	HSVGC	E4	V_{SSD1}
F1	VSVGC	F2	PIXCLKI
F3	PD3	F4	V_{DDD1}
G1	FSVGC	G2	SDA
G3	$\overline{CBO}$	G4	PIXCLKO
H1	PD2	H2	PD1
H3	PD0		

6.2 Pin description

Table 4: Pin description

Symbol	Pin		Type [1]	Description
	LBGA156	QFP44		
PD8	B2	1	I	see Table 28 to Table 33 for pin assignment
PD9	B1	2	I	see Table 28 to Table 33 for pin assignment
PD10	C2	3	I	see Table 28 to Table 33 for pin assignment
PD11	C1	4	I	see Table 28 to Table 33 for pin assignment
$\overline{RESET}$	D2	5	I	reset input; active LOW
TMS	D3	6	I	test mode select input for BST [2]
TDO	D1	7	O	test data output for BST [2]
TCK	E1	8	I	test clock input for BST [2]
V_{SSD1}	E4	9	S	digital ground 1 (peripheral cells)

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Table 4: Pin description *...continued*

Symbol	Pin		Type [1]	Description
	LBGA156	QFP44		
V_{DDD1}	F4	10	S	digital supply voltage 1 (3.3 V for peripheral cells)
SCL	E2	11	I(/O)	serial clock input (I^2C-bus) with inactive output path
SDA	G2	12	I/O	serial data input/output (I^2C-bus)
FSVGC	G1	13	I/O	frame synchronization output to Video Graphics Controller (VGC) (optional input) [3]
VSVGC	F1	14	I/O	vertical synchronization output to VGC (optional input) [3]
PIXCLKI	F2	15	I	pixel clock input (looped through)
PD3	F3	16	I	MSB – 4 with C_B-Y-C_R 4 : 2 : 2; see Table 28 to Table 33 for pin assignment
PD2	H1	17	I	MSB – 5 with C_B-Y-C_R 4 : 2 : 2; see Table 28 to Table 33 for pin assignment
PD1	H2	18	I	MSB – 6 with C_B-Y-C_R 4 : 2 : 2; see Table 28 to Table 33 for pin assignment
PD0	H3	19	I	MSB – 7 with C_B-Y-C_R 4 : 2 : 2; see Table 28 to Table 33 for pin assignment
PIXCLKO	G4	20	O	pixel clock output to VGC
$\overline{CBO}$	G3	21	O	composite blanking output to VGC; active LOW [3]
HSVGC	E3	22	I/O	horizontal synchronization output to VGC (optional input) [3]
TTX_SRES	C3	23	I	teletext input or sync reset input
TTXRQ_XCLKO2	C4	24	O	teletext request output or 13.5 MHz clock output of the crystal oscillator [3]
VSM	D7	25	O	vertical synchronization output to monitor (non-interlaced auxiliary RGB)
HSM_CSYNC	D8	26	O	horizontal synchronization output to monitor (non-interlaced auxiliary RGB) or composite sync for RGB-SCART
RED_CR_C	C8	27	O	analog output of RED or C_R or C signal
GREEN_VBS_CVBS	C7	28	O	analog output of GREEN or VBS or CVBS signal
V_{DDA1}	A10, B9, C9, D9	29	S	analog supply voltage 1 (3.3 V for DACs)
BLUE_CB_CVBS	C6	30	O	analog output of BLUE or C_B or CVBS signal
RSET	A9	31	O	DAC reference pin; connected via 1 kΩ resistor to analog ground (do not use capacitor in parallel with 1 kΩ resistor)
DUMP	A7, B7	32	O	DAC reference pin; connected via 12 Ω resistor to analog ground
V_{SSA1}	A8, B8	33	S	analog ground 1
XTALO	A6	34	O	crystal oscillator output
XTALI	A5	35	I	crystal oscillator input

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Table 4: Pin description *...continued*

Symbol	Pin		Type [1]	Description
	LBGA156	QFP44		
V_{DDA2}	B6, D6	36	S	analog supply voltage 2 (3.3 V for DACs and oscillator)
$\overline{TRST}$	A4	37	I	test reset input for BST; active LOW [2] [4] [5]
TDI	B5	38	I	test data input for BST [2]
V_{SSD2}	C5, D5	39	S	digital ground 2
V_{DDD2}	D4	40	S	digital supply voltage 2 (3.3 V for core)
PD4	A3	41	I	MSB – 3 with C_B-Y-C_R 4 : 2 : 2; see Table 28 to Table 33 for pin assignment
PD5	B3	42	I	MSB – 2 with C_B-Y-C_R 4 : 2 : 2; see Table 28 to Table 33 for pin assignment
PD6	B4	43	I	MSB – 1 with C_B-Y-C_R 4 : 2 : 2; see Table 28 to Table 33 for pin assignment
PD7	A2	44	I	MSB with C_B-Y-C_R 4 : 2 : 2; see Table 28 to Table 33 for pin assignment

[1] Pin type: I = input, O = output, S = supply.

[2] In accordance with the *"IEEE1149.1"* standard the pins TDI, TMS, TCK and $\overline{TRST}$ are input pins with an internal pull-up resistor and TDO is a 3-state output pin.

[3] Pins FSVGC, VSVGC, $\overline{CBO}$, HSVGC and TTXRQ_XCLKO2 are used for bootstrapping; see Section 7.1.

[4] For board design without boundary scan implementation connect $\overline{TRST}$ to ground.

[5] This pin provides easy initialization of the BST circuit. $\overline{TRST}$ can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.

7. Functional description

The digital video encoder encodes digital luminance and color difference signals (C_B-Y-C_R) or digital RGB signals into analog CVBS, S-video and, optionally, RGB or C_R-Y-C_B signals. NTSC M, PAL B/G and sub-standards are supported.

The SAA7102; SAA7103 can be directly connected to a PC video graphics controller with a maximum resolution of 800 × 600 at a 50 Hz or 60 Hz frame rate. A programmable scaler scales the computer graphics picture so that it will fit into a standard TV screen with an adjustable underscan area. Non-interlaced-to-interlaced conversion is optimized with an adjustable anti-flicker filter for a flicker-free display at a very high sharpness.

Besides the most common 16-bit 4 : 2 : 2 C_B-Y-C_R input format (using 8 pins with double edge clocking), other C_B-Y-C_R and RGB formats are also supported; see Table 28 to Table 33.

A complete 3 × 256 bytes Look-Up Table (LUT), which can be used, for example, as a separate gamma corrector, is located in the RGB domain; it can be loaded either through the video input port Pixel Data (PD) or via the I^2C-bus.

The SAA7102; SAA7103 supports a 32-bit × 32-bit × 2-bit hardware cursor, the pattern of which can also be loaded through the video input port or via the I^2C-bus.

It is also possible to encode interlaced 4 : 2 : 2 video signals such as PC-DVD; for that the anti-flicker filter, and in most cases the scaler, will simply be bypassed.

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Besides the applications for video output, the SAA7102; SAA7103 can also be used for generating a kind of auxiliary VGA output, when the RGB non-interlaced input signal is fed to the DACs. This may be of interest for example, when the graphics controller provides a second graphics window at its video output port.

The basic encoder function consists of subcarrier generation, color modulation and insertion of synchronization signals at a crystal-stable clock rate of 13.5 MHz (independent of the actual pixel clock used at the input side), corresponding to an internal 4 : 2 : 2 bandwidth in the luminance/color difference domain. Luminance and chrominance signals are filtered in accordance with the standard requirements of *"RS-170-A"* and *"ITU-R BT.470-3"*.

For ease of analog post filtering the signals are twice oversampled to 27 MHz before digital-to-analog conversion.

The total filter transfer characteristics (scaler and anti-flicker filter are not taken into account) are illustrated in Figure 6 to Figure 11. All three DACs are realized with full 10-bit resolution. The C_R-Y-C_B to RGB dematrix can be bypassed (optionally) in order to provide the upsampled C_R-Y-C_B input signals.

The 8-bit multiplexed C_B-Y-C_R formats are *"ITU-R BT.656"* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in Slave mode. For assignment of the input data to the rising or falling clock edge see Table 28 to Table 34.

In order to display interlaced RGB signals through a euro-connector TV set, a separate digital composite sync signal (pin HSM_CSYNC) can be generated; it can be advanced up to 31 periods of the 27 MHz crystal clock in order to be adapted to the RGB processing of a TV set.

The SAA7102; SAA7103 synthesizes all necessary internal signals, color subcarrier frequency and synchronization signals from that clock.

Wide screen signalling data can be loaded via the I^2C-bus and is inserted into line 23 for standards using a 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCRs is loadable via the I^2C-bus.

The IC also contains closed caption and extended data services encoding (line 21), and supports teletext insertion for the appropriate bit stream format at a 27 MHz clock rate (see Figure 15). It is also possible to load data for the copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters such as:

- Black and blanking level control
- Color subcarrier frequency
- Variable burst amplitude etc.

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7.1 Reset conditions

To activate the reset a pulse at least of 2 crystal clocks duration is required.

During reset ($\overline{RESET}$ = LOW) plus an extra 32 crystal clock periods, FSVGC, VSVGC, $\overline{CBO}$, HSVGC and TTX_SRES are set to input mode and HSM_CSYNC and VSM are set to 3-state. A reset also forces the I^2C-bus interface to abort any running bus transfer and sets it into receive condition.

After reset, the state of the I/Os and other functions is defined by the strapping pins until an I^2C-bus access redefines the corresponding registers; see Table 5.

Table 5: Strapping pins

Pin	Tied	Preset
FSVGC	LOW	NTSC M encoding, PIXCLK fits to 640 × 480 graphics input
	HIGH	PAL B/G encoding, PIXCLK fits to 640 × 480 graphics input
VSVGC	LOW	4 : 2 : 2 Y-C_B-C_R graphics input (format 0)
	HIGH	4 : 4 : 4 RGB graphics input (format 3)
$\overline{CBO}$	LOW	input demultiplex phase: LSB = LOW
	HIGH	input demultiplex phase: LSB = HIGH
HSVGC	LOW	input demultiplex phase: MSB = LOW
	HIGH	input demultiplex phase: MSB = HIGH
TTXRQ_XCLKO2	LOW	slave (FSVGC, VSVGC and HSVGC are inputs, internal color bar is active)
	HIGH	master (FSVGC, VSVGC and HSVGC are outputs)

7.2 Input formatter

The input formatter converts all accepted PD input data formats, either RGB or Y-C_B-C_R, to a common internal RGB or Y-C_B-C_R data stream.

When double-edge clocking is used, the data is internally split into portions PPD1 and PPD2. The clock edge assignment must be set according to the I^2C-bus control bits EDGE1 and EDGE2 for correct operation.

If Y-C_B-C_R is being applied as a 27 MB/s data stream, the output of the input formatter can be used directly to feed the video encoder block.

7.3 RGB LUT

The three 256 byte RAMs of this block can be addressed by three 8-bit wide signals, thus it can be used to build any transformation, e.g. a gamma correction for RGB signals. In the event that the indexed color data is applied, the RAMs are addressed in parallel.

The LUTs can either be loaded by an I^2C-bus write access or can be part of the pixel data input through the PD port. In the latter case, 256 bytes × 3 bytes for the R, G and B LUT are expected at the beginning of the input video line, two lines before the line that has been defined as first active line, until the middle of the line immediately preceding the first active line. The first 3 bytes represent the first RGB LUT data, and so on.

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7.4 Cursor insertion

A 32 dots × 32 dots cursor can be overlaid as an option; the bit map of the cursor can be uploaded by an I²C-bus write access to specific registers or in the pixel data input through the PD port. In the latter case, the 256 bytes defining the cursor bit map (2 bits per pixel) are expected immediately following the last RGB LUT data in the line preceding the first active line.

The cursor bit map is set up as follows: each pixel occupies 2 bits. The meaning of these bits depends on the CMODE I²C-bus register as described in Table 8. Transparent means that the input pixels are passed through, the 'cursor colors' can be programmed in separate registers.

The bit map is stored with 4 pixels per byte, aligned to the least significant bit. So the first pixel is in bits 0 and 1, the next pixel in bits 3 and 4 and so on. The first index is the column, followed by the row; index 0,0 is the upper left corner.

Table 6: Layout of a byte in the cursor bit map

7	6	5	4	3	2	1	0
pixel n + 3		pixel n + 2		pixel n + 1		pixel n	
D1	D0	D1	D0	D1	D0	D1	D0

For each direction, there are 2 registers controlling the position of the cursor, one controls the position of the 'hot spot', the other register controls the insertion position. The hot spot is the 'tip' of the pointer arrow. It can have any position in the bit map. The actual position registers describe the co-ordinates of the hot spot. Again 0,0 is the upper left corner. While it is not possible to move the hot spot beyond the left respectively upper screen border this is perfectly legal for the right respectively lower border. It should be noted that the cursor position is described relative to the input resolution.

Table 7: Cursor bit map

Byte	7 6	5 4	3 2	1 0
0	row 0 column 3	row 0 column 2	row 0 column 1	row 0 column 0
1	row 0 column 7	row 0 column 6	row 0 column 5	row 0 column 4
2	row 0 column 11	row 0 column 10	row 0 column 9	row 0 column 8
...	...	...	...	...
6	row 0 column 27	row 0 column 26	row 0 column 25	row 0 column 24
7	row 0 column 31	row 0 column 30	row 0 column 29	row 0 column 28
...	...	...	...	...
254	row 31 column 27	row 31 column 26	row 31 column 25	row 31 column 24
255	row 31 column 31	row 31 column 30	row 31 column 29	row 31 column 28

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Table 8: Cursor modes

Cursor pattern	Cursor mode	
	CMODE = 0	CMODE = 1
00	second cursor color	second cursor color
01	first cursor color	first cursor color
10	transparent	transparent
11	inverted input	auxiliary cursor color

7.5 RGB Y-C_B-C_R matrix

RGB input signals to be encoded to PAL or NTSC are converted to the Y-C_B-C_R color space in this block. The color difference signals are fed through low-pass filters and formatted to a ITU-R BT.601 like 4 : 2 : 2 data stream for further processing.

The matrix and formatting blocks can be bypassed for Y-C_B-C_R graphics input.

When the auxiliary VGA mode is selected, the output of the cursor insertion block is immediately directed to the triple DAC.

7.6 Horizontal scaler

The high quality horizontal scaler operates on the 4 : 2 : 2 data stream. Its control engines compensate the color phase offset automatically.

The scaler starts processing after a programmable horizontal offset and continues with a number of input pixels. Each input pixel is a programmable fraction of the current output pixel (XINC/4096). A special case is XINC = 0, this sets the scaling factor to 1.

If the SAA7102; SAA7103 input data is in accordance with *"ITU-R BT.656"*, the scaler enters another mode. In this event, XINC needs to be set to 2048 for a scaling factor of 1. With higher values, upscaling will occur.

The phase resolution of the circuit is 12 bits, giving a maximum offset of 0.2 after 800 input pixels. Small FIFOs rearrange a 4 : 2 : 2 data stream at the scaler output.

7.7 Vertical scaler and anti-flicker filter

The functions scaling, Anti-Flicker Filter (AFF) and re-interlacing are implemented in the vertical scaler.

Besides the entire input frame, it receives the first and last lines of the border to allow anti-flicker filtering.

The circuit generates the interlaced output fields by scaling down the input frames with different offsets for odd and even fields. Increasing the YSKIP setting reduces the anti-flicker function. A YSKIP value of 4095 switches it off; see Table 91.

The programming is similar to the horizontal scaler. For the re-interlacing, the resolutions of the offset registers are not sufficient, so the weighting factors for the first lines can also be adjusted. YINC = 0 sets the scaling factor to 1; YIWGTO and YIWGTE must not be 0.

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Due to the re-interlacing, the circuit can perform upscaling. The maximum factor depends on the setting of the anti-flicker function and can be derived from the formulae given in Section 7.17.

7.8 FIFO

The FIFO acts as a buffer to translate from the PIXCLK clock domain to the XTAL clock domain. The write clock is PIXCLK and the read clock is XTAL. An underflow or overflow condition can be detected via the I^2C-bus read access.

In order to avoid underflows and overflows, it is essential that the frequency of the synthesized PIXCLK matches to the input graphics resolution and the desired scaling factor. It is suggested to refer to Table 9 to Table 26 for some representative combinations.

7.9 Border generator

When the graphics picture is to be displayed as interlaced PAL, NTSC, S-video or RGB on a TV screen, it is desired in many cases not to lose picture information due to the inherent overscanning of a TV set. The desired amount of underscan area, which is achieved through appropriate scaling in the vertical and horizontal direction, can be filled in the border generator with an arbitrary true color tint.

7.10 Oscillator and Discrete Time Oscillator (DTO)

The master clock generation is realized as a 27 MHz crystal oscillator, which can operate with either a fundamental wave crystal or a 3rd-harmonic crystal.

The crystal clock supplies the DTO of the pixel clock synthesizer, the video encoder and the I^2C-bus control block. It also usually supplies the triple DAC, with the exception of the auxiliary VGA mode, where the triple DAC is clocked by the pixel clock (PIXCLK).

The DTO can be programmed to synthesize all relevant pixel clock frequencies between circa 18 MHz and 44 MHz.

7.11 Low-pass Clock Generation Circuit (CGC)

This block reduces the phase jitter of the synthesized pixel clock. It works as a tracking filter for all relevant synthesized pixel clock frequencies.

7.12 Encoder

7.12.1 Video path

The encoder generates luminance and color subcarrier output signals from the Y, C_B and C_R baseband signals, which are suitable for use as CVBS or separate Y and C signals.

Input to the encoder, at 27 MHz clock (e.g. DVD), is either originated from computer graphics at pixel clock, fed through the FIFO and border generator, or a ITU-R BT.656 style signal.

Luminance is modified in gain and in offset (the offset is programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level, in accordance with standard composite synchronization

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schemes. Other manipulations used for the Macrovision anti-taping process, such as additional insertion of AGC super-white pulses (programmable in height), are supported by the SAA7102 only.

To enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figure 8 and Figure 9. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for C_B and C_R), and a standard dependent burst is inserted, before baseband color signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher color bandwidth, which can be used for the Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figure 6 and Figure 7.

The amplitude (beginning and ending) of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. After the succeeding quadrature modulator, color is provided on the subcarrier in 10-bit resolution.

The numeric ratio between the Y and C outputs is in accordance with the standards.

7.12.2 Teletext insertion and encoding (not simultaneously with real-time control)

Pin TTX_SRES receives a WST or NABTS teletext bitstream sampled at the crystal clock. At each rising edge of the output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX_SRES.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ_XCLKO2 provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which can be selected independently for both fields. The internal insertion window for text is set to 360 (PAL WST), 296 (NTSC WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Figure 15.

Alternatively, this pin can be provided with a buffered crystal clock (XCLK) of 13.5 MHz.

7.12.3 Video Programming System (VPS) encoding

Five bytes of VPS information can be loaded via the I^2C-bus and will be encoded in the appropriate format into line 16.

7.12.4 Closed caption encoder

Using this circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number in which data is to be encoded, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC M standard 32 times horizontal line frequency.

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Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

7.12.5 Anti-taping (SAA7102 only)

For more information contact your nearest Philips Semiconductors sales office.

7.13 RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before Y, C_B and C_R signals are de-matrixed, individual gain adjustment for Y and color difference signals and 2 times oversampling for luminance and 4 times oversampling for color difference signals is performed. The transfer curves of luminance and color difference components of RGB are illustrated in Figure 10 and Figure 11.

7.14 Triple DAC

Both Y and C signals are converted from digital-to-analog in a 10-bit resolution at the output of the video encoder. Y and C signals are also combined into a 10-bit CVBS signal.

The CVBS output signal occurs with the same processing delay as the Y, C and optional RGB or C_R-Y-C_B outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of the conversion ranges.

RED, GREEN and BLUE signals are also converted from digital-to-analog, each providing a 10-bit resolution.

The reference currents of all three DACs can be adjusted individually in order to adapt for different output signals. In addition, all reference currents can be adjusted commonly to compensate for small tolerances of the on-chip band gap reference voltage.

Alternatively, all currents can be switched off to reduce power dissipation.

All three outputs can be used to sense for an external load (usually 75 Ω) during a pre-defined output. A flag in the I^2C-bus status byte reflects whether a load is applied or not.

If the SAA7102; SAA7103 is required to drive a second (auxiliary) VGA monitor, the DACs receive the signal directly from the cursor insertion block. In this event, the DACs are clocked at the incoming PIXCLKI instead of the 27 MHz crystal clock used in the video encoder.

7.15 Timing generator

The synchronization of the SAA7102; SAA7103 is able to operate in two modes; Slave mode and Master mode.

In Slave mode, the circuit accepts sync pulses on the bidirectional FSVGC (frame sync), VSVGC (vertical sync) and HSVGC (horizontal sync) pins: the polarities of the signals can be programmed. The frame sync signal is only necessary when the input signal is

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interlaced, in other cases it may be omitted. If the frame sync signal is present, it is possible to derive the vertical and the horizontal phase from it by setting the HFS and VFS bits. HSVGC and VSVGC are not necessary in this case, so it is possible to switch the pins to output mode.

Alternatively, the device can be triggered by auxiliary codes in a ITU-R BT.656 data stream via PD7 to PD0.

Only vertical frequencies of 50 Hz and 60 Hz are allowed with the SAA7102; SAA7103. In Slave mode, it is not possible to lock the encoders color carrier to the line frequency with the PHRES bits.

In the (more common) Master mode, the time base of the circuit is continuously free-running. The IC can output a frame sync at pin FSVGC, a vertical sync at pin VSVGC, a horizontal sync at pin HSVGC and a composite blanking signal at pin $\overline{CBO}$. All of these signals are defined in the PIXCLK domain. The duration of HSVGC and VSVGC are fixed, they are 64 clocks for HSVGC and 1 line for VSVGC. The leading slopes are in phase and the polarities can be programmed.

The input line length can be programmed. The field length is always derived from the field length of the encoder and the pixel clock frequency that is being used.

$\overline{CBO}$ acts as a data request signal. The circuit accepts input data at a programmable number of clocks after $\overline{CBO}$ goes active. This signal is programmable and it is possible to adjust the following (see Figure 13 and Figure 14):

- The horizontal offset
- The length of the active part of the line
- The distance from active start to first expected data
- The vertical offset separately for odd and even fields
- The number of lines per input field

In most cases, the vertical offsets for odd and even fields are equal. If they are not, then the even field will start later. The SAA7102; SAA7103 will also request the first input lines in the even field, the total number of requested lines will increase by the difference of the offsets.

As stated above, the circuit can be programmed to accept the look-up and cursor data in the first 2 lines of each field. The timing generator provides normal data request pulses for these lines; the duration is the same as for regular lines. The additional request pulses will be suppressed with LUTL set to logic 0; see Table 101. The other vertical timings do not change in this case, so the first active line can be number 2, counted from 0.

7.16 I^{2}C-bus interface

The I^{2}C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbit/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and read, except two read only status bytes.

The register bit map consists of an RGB Look-Up Table (LUT), a cursor bit map and control registers. The LUT contains three banks of 256 bytes, where each RGB triplet is assigned to one address. Thus a write access needs the LUT address and three data

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bytes following subaddress FFh. For further write access auto-incrementing of the LUT address is performed. The cursor bit map access is similar to the LUT access but contains only a single byte per address.

The I^2C-bus slave address is defined as 88h.

7.17 Programming the SAA7102; SAA7103

In order to program the SAA7102; SAA7103 it is first necessary to determine the input and output field timings. The timings are controlled by decoding binary counters that index the position in the current line and field respectively. In both cases, 0 means the start of the sync pulse.

At 60 Hz, the first visible pixel has the index 256, 710 pixels can be encoded; at 50 Hz, the index is 284, 702 pixels can be visible. Some variables are defined below:

- InPix: the number of active pixels per input line
- InPpl: the length of the entire input line in pixel clocks
- InLin: the number of active lines per input field/frame
- TPclk: the pixel clock period
- OutPix: the number of active pixels per output line
- OutLin: the number of active lines per output field
- TXclk: the encoder clock period (37.037 ns)

The output lines should be centred on the screen. It should be noted that the encoder has 2 clocks per pixel; see Table 62.

ADWHS = 256 + 710 – OutPix (60 Hz); ADWHS = 284 + 702 – OutPix (50 Hz);
ADWHE = ADWHS + OutPix × 2 (all frequencies)

For vertical, the procedure is the same. At 60 Hz, the first line with video information is number 19, 240 lines can be active. For 50 Hz, the numbers are 23 and 287; see Table 70 to Table 72.

$FAL = 19 + \frac{240 - OutLin}{2}$ (60 Hz); $FAL = 23 + \frac{287 - OutLin}{2}$ (50 Hz);

LAL = FAL + OutLin (all frequencies).

Most TV sets use overscan, and not all pixels respectively lines are visible. There is no standard for the factor, it is highly recommended to make the number of output pixels and lines adjustable. A reasonable underscan factor is 10 %, giving approximately 640 output pixels per line.

The total number of pixel clocks per line and the input horizontal offset need to be chosen next. The only constraint is that the horizontal blanking has at least 10 clock pulses.

The required pixel clock frequency can be determined in the following way: Due to the limited internal FIFO size, the input path has to provide all pixels in the same time frame as the encoders vertical active time. The scaler also has to process the first and last border lines for the anti-flicker function. Thus:

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$$TPclk = \frac{262.5 \times 1716 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 262.5\right)}$$ (60 Hz)

$$TPclk = \frac{312.5 \times 1728 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 312.5\right)}$$ (50 Hz) and for the pixel clock generator

$$PCL = \frac{TXclk}{TPclk} \times 2^{21}$$ (all frequencies); see Table 74.

The input vertical offset can be taken from the assumption that the scaler should just have finished writing the first line when the encoder starts reading it:

$$YOFS = \frac{FAL \times 1716 \times TXclk}{InPpl \times TPclk} - 2$$ (60 Hz) $$YOFS = \frac{FAL \times 1728 \times TXclk}{InPpl \times TPclk} - 2$$ (50 Hz)

In most cases the vertical offsets will be the same for odd and even fields. The results should be rounded down.

Once the timings are known the scaler can be programmed.

XOFS can be chosen arbitrarily, the condition being that XOFS + XPIX ≤ HLEN is fulfilled. Values given by the VESA display timings are preferred.

HLEN = InPpl – 1

$$XPIX = \frac{InPix}{2}$$

$$XINC = \frac{OutPix}{InPix} \times 4096$$

XINC needs to be rounded up, it needs to be set to 0 for a scaling factor of 1.

YPIX = InLin

YSKIP defines the anti-flicker function. 0 means maximum flicker reduction but minimum vertical bandwidth, 4095 gives no flicker reduction and maximum bandwidth.

$$YINC = \frac{OutLin}{InLin + 2} \times \left(1 + \frac{YSKIP}{4095}\right) \times 4096$$

$$YIWGTO = \frac{YINC}{2} + 2048$$

$$YIWGTE = \frac{YINC - YSKIP}{2}$$

When YINC = 0 it sets the scaler to scaling factor 1. The initial weighting factors must not be set to 0 in this case. YIWGTE may go negative. In this event, YINC should be added and YOFSE incremented. This can be repeated as often as necessary to make YIWGTE positive.

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Due to the limited amount of memory it is not possible to get valid vertical scaler settings only from the formulae above. In some cases it is necessary to adjust the vertical offsets or the scaler increment to get valid settings. Table 9 to Table 26 show verified settings. They are organized in the following way: The tables are separate for the standard to be encoded, the input resolution and three different anti-flicker filter settings. Each table contains 5 vertical sizes with 5 different offsets. They are intended to be selected according to the current TV set. The corresponding horizontal resolutions of 640 pixels give proper aspect ratios. They can be adjusted according to the formulae above. The next line gives a minimum size intended to fit on the screen under all circumstances. The corresponding horizontal resolution is 620 pixels. Overscan is only possible with an input resolution of 800 × 600 pixels. Where possible, the corresponding settings are given on the last lines of the tables.

7.18 Input levels and formats

The SAA7102; SAA7103 accepts digital Y, C_B, C_R or RGB data with levels (digital codes) in accordance with *"ITU-R BT.601"*; see Table 27.

For C and CVBS outputs, deviating amplitudes of the color difference signals can be compensated for by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively C_R-Y-C_B path features an individual gain setting for luminance (GY) and color difference signals (GCD). Reference levels are measured with a color bar, 100 % white, 100 % amplitude and 100 % saturation.

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Table 9: Y scaler programming at NTSC, input frame size: 640 × 400, full anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
212	–4	29	241	1851099	2163	0	52	52	3128	1080
212	–2	31	243	1851099	2163	0	56	56	3128	1080
212	0	33	245	1851099	2163	0	60	60	3128	1080
212	2	35	247	1851099	2163	0	63	63	3128	1080
212	4	37	249	1851099	2163	0	67	67	3128	1080
214	–4	28	242	1836201	2181	0	50	50	3138	1090
214	–2	30	244	1836201	2181	0	54	54	3138	1090
214	0	32	246	1836201	2181	0	57	57	3138	1090
214	2	34	248	1836201	2181	0	61	61	3138	1090
214	4	36	250	1836201	2181	0	65	65	3138	1090
216	–4	27	243	1817578	2202	0	47	47	3148	1100
216	–2	29	245	1817578	2202	0	51	51	3148	1100
216	0	31	247	1817578	2202	0	55	55	3148	1100
216	2	33	249	1817578	2202	0	58	58	3148	1100
216	4	35	251	1817578	2202	0	62	62	3148	1100
218	–4	26	244	1802680	2222	0	45	45	3158	1110
218	–2	28	246	1802680	2222	0	49	49	3158	1110
218	0	30	248	1802680	2222	0	53	53	3158	1110
218	2	32	250	1802680	2222	0	56	56	3158	1110
218	4	34	252	1802680	2222	0	60	60	3158	1110
220	–4	25	245	1784057	2245	0	43	43	3168	1120
220	–2	27	247	1784057	2245	0	46	46	3168	1120
220	0	29	249	1784057	2245	0	50	50	3168	1120
220	2	31	251	1784057	2245	0	54	54	3168	1120
220	4	33	253	1784057	2245	0	57	57	3168	1120
Overscan (horizontal size: 710 pixels)										
241	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
204	0	37	241	1925590	2079	0	70	70	3087	1039

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Table 10: Y scaler programming at NTSC, input frame size: 640 × 400, half anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
212	–4	29	241	1851099	3123	1820	52	52	3668	596
212	–2	31	243	1851099	3123	1820	56	56	3668	596
212	0	33	245	1851099	3123	1820	60	60	3668	596
212	2	35	247	1851099	3123	1820	64	64	3668	596
212	4	37	249	1851099	3123	1820	67	67	3668	596
214	–4	28	242	1836201	3135	1790	50	50	3683	611
214	–2	30	244	1836201	3135	1790	54	54	3683	611
214	0	32	246	1836201	3135	1790	58	58	3683	611
214	2	34	248	1836201	3135	1790	61	61	3683	611
214	4	36	250	1836201	3135	1790	65	65	3683	611
216	–4	27	243	1817578	3145	1750	48	48	3698	626
216	–2	29	245	1817578	3145	1750	51	51	3698	626
216	0	31	247	1817578	3145	1750	55	55	3698	626
216	2	33	249	1817578	3145	1750	59	59	3698	626
216	4	35	251	1817578	3145	1750	63	63	3698	626
218	–4	26	244	1802680	3155	1720	45	45	3714	642
218	–2	28	246	1802680	3155	1720	49	49	3714	642
218	0	30	248	1802680	3155	1720	53	53	3714	642
218	2	32	250	1802680	3155	1720	56	56	3714	642
218	4	34	252	1802680	3155	1720	60	60	3714	642
220	–4	25	245	1784057	3165	1680	43	43	3729	657
220	–2	27	247	1784057	3165	1680	47	47	3729	657
220	0	29	249	1784057	3165	1680	50	50	3729	657
220	2	31	251	1784057	3165	1680	54	54	3729	657
220	4	33	253	1784057	3165	1680	58	58	3729	657
Full size (horizontal size: 710 pixels)										
241	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
204	0	37	241	1925590	3087	1980	70	70	3589	551

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Table 11: Y scaler programming at NTSC, input frame size: 640 × 400, no anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
212	–4	29	241	1851099	4094	3655	52	52	4092	216
212	–2	31	243	1851099	4094	3655	56	56	4092	216
212	0	33	245	1851099	4094	3655	60	60	4092	216
212	2	35	247	1851099	4094	3655	64	64	4092	216
212	4	37	249	1851099	4094	3655	68	68	4092	216
214	–4	28	242	1836201	4090	3580	50	50	4091	253
214	–2	30	244	1836201	4090	3580	54	54	4091	253
214	0	32	246	1836201	4090	3580	58	58	4091	253
214	2	34	248	1836201	4088	3580	61	61	4091	253
214	4	36	250	1836201	4088	3580	65	65	4091	253
216	–4	27	243	1817578	4093	3510	48	48	4091	288
216	–2	29	245	1817578	4093	3510	52	52	4091	288
216	0	31	247	1817578	4093	3510	55	55	4091	288
216	2	33	249	1817578	4093	3510	59	59	4091	288
216	4	35	251	1817578	4093	3510	63	63	4091	288
218	–4	26	244	1802680	4092	3445	46	46	4092	322
218	–2	28	246	1802680	4092	3445	49	49	4092	322
218	0	30	248	1802680	4092	3445	53	53	4092	322
218	2	32	250	1802680	4092	3445	57	57	4092	322
218	4	34	252	1802680	4092	3445	60	60	4092	322
220	–4	25	245	1784057	4090	3370	43	43	4091	358
220	–2	27	247	1784057	4090	3370	47	47	4091	358
220	0	29	249	1784057	4090	3370	50	50	4091	358
220	2	31	251	1784057	4090	3370	54	54	4091	358
220	4	33	253	1784057	4090	3370	58	58	4091	358
Full size (horizontal size: 710 pixels)										
241	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
204	0	37	241	1925590	4087	3950	70	70	4089	66

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Table 12: Y scaler programming at NTSC, input frame size: 640 × 480, full anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
212	–4	29	241	2219829	1804	0	63	63	2948	900
212	–2	31	243	2219829	1804	0	67	67	2948	900
212	0	33	245	2219829	1804	0	72	72	2948	900
212	2	35	247	2219829	1804	0	77	77	2948	900
212	4	37	249	2219829	1804	0	81	81	2948	900
214	–4	28	242	2201206	1819	0	60	60	2957	909
214	–2	30	244	2201206	1819	0	65	65	2957	909
214	0	32	246	2201206	1819	0	69	69	2957	909
214	2	34	248	2201206	1819	0	73	73	2957	909
214	4	36	250	2201206	1819	0	78	78	2957	909
216	–4	27	243	2178859	1836	0	57	57	2965	917
216	–2	29	245	2178859	1836	0	61	61	2965	917
216	0	31	247	2178859	1836	0	66	66	2965	917
216	2	33	249	2178859	1836	0	70	70	2965	917
216	4	35	251	2178859	1836	0	75	75	2965	917
218	–4	26	244	2160236	1853	0	54	54	2974	926
218	–2	28	246	2160236	1853	0	59	59	2974	926
218	0	30	248	2160236	1853	0	63	63	2974	926
218	2	32	250	2160236	1853	0	68	68	2974	926
218	4	34	252	2160236	1853	0	72	72	2974	926
220	–4	25	245	2141613	1870	0	52	52	2982	934
220	–2	27	247	2141613	1870	0	56	56	2982	934
220	0	29	249	2141613	1870	0	61	61	2982	934
220	2	31	251	2141613	1870	0	65	65	2982	934
220	4	33	253	2141613	1870	0	69	69	2982	934
Full size (horizontal size: 710 pixels)										
241	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
204	0	37	241	2309218	1734	0	84	84	2941	866

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Table 13: Y scaler programming at NTSC, input frame size: 640 × 480, half anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
212	–4	29	241	2219829	2704	2048	63	63	3399	327
212	–2	31	243	2219829	2704	2048	67	67	3399	327
212	0	33	245	2219829	2704	2048	72	72	3399	327
212	2	35	247	2219829	2704	2048	77	77	3399	327
212	4	37	249	2219829	2704	2048	81	81	3399	327
214	–4	28	242	2201206	2730	2048	60	60	3412	340
214	–2	30	244	2201206	2730	2048	65	65	3412	340
214	0	32	246	2201206	2730	2048	69	69	3412	340
214	2	34	248	2201206	2730	2048	74	74	3412	340
214	4	36	250	2201206	2730	2048	78	78	3412	340
216	–4	27	243	2178859	2756	2048	57	57	3424	352
216	–2	29	245	2178859	2756	2048	62	62	3424	352
216	0	31	247	2178859	2756	2048	66	66	3424	352
216	2	33	249	2178859	2756	2048	71	71	3424	352
216	4	35	251	2178859	2756	2048	75	75	3424	352
218	–4	26	244	2160236	2781	2048	55	55	3437	365
218	–2	28	246	2160236	2781	2048	59	59	3437	365
218	0	30	248	2160236	2781	2048	63	63	3437	365
218	2	32	250	2160236	2781	2048	68	68	3437	365
218	4	34	252	2160236	2781	2048	72	72	3437	365
220	–4	25	245	2141613	2807	2048	52	52	3450	378
220	–2	27	247	2141613	2807	2048	57	57	3450	378
220	0	29	249	2141613	2807	2048	61	61	3450	378
220	2	31	251	2141613	2807	2048	65	65	3450	378
220	4	33	253	2141613	2807	2048	70	70	3450	378
Full size (horizontal size: 710 pixels)										
241	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
204	0	37	241	2309218	2602	2048	84	84	3348	276

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Table 14: Y scaler programming at NTSC, input frame size: 640 × 480, no anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
212	–4	29	241	2219829	3607	4095	63	64	3849	3362
212	–2	31	243	2219829	3607	4095	68	69	3849	3362
212	0	33	245	2219829	3607	4095	72	73	3849	3362
212	2	35	247	2219829	3607	4095	77	78	3849	3362
212	4	37	249	2219829	3607	4095	81	82	3849	3362
214	–4	28	242	2201206	3639	4095	60	61	3866	3413
214	–2	30	244	2201206	3639	4095	65	66	3866	3413
214	0	32	246	2201206	3639	4095	69	70	3866	3413
214	2	34	248	2201206	3639	4095	74	75	3866	3413
214	4	36	250	2201206	3639	4095	78	79	3866	3413
216	–4	27	243	2178859	3675	4095	57	58	3883	3464
216	–2	29	245	2178859	3675	4095	62	63	3883	3464
216	0	31	247	2178859	3675	4095	66	67	3883	3464
216	2	33	249	2178859	3675	4095	71	72	3883	3464
216	4	35	251	2178859	3675	4095	75	76	3883	3464
218	–4	26	244	2160236	3709	4095	55	56	3900	3515
218	–2	28	246	2160236	3709	4095	59	60	3900	3515
218	0	30	248	2160236	3709	4095	64	65	3900	3515
218	2	32	250	2160236	3709	4095	68	69	3900	3515
218	4	34	252	2160236	3709	4095	73	74	3900	3515
220	–4	25	245	2141613	3741	4095	52	53	3917	3566
220	–2	27	247	2141613	3741	4095	57	58	3917	3566
220	0	29	249	2141613	3741	4095	61	62	3917	3566
220	2	31	251	2141613	3741	4095	65	66	3917	3566
220	4	33	253	2141613	3741	4095	70	71	3917	3566
Full size (horizontal size: 710 pixels)										
241	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
204	0	37	241	2309218	3471	4095	85	86	3781	3158

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Table 15: Y scaler programming at NTSC, input frame size: 800 × 600, full anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
212	–4	29	241	3551726	1443	0	79	79	2769	721
212	–2	31	243	3551726	1443	0	84	84	2769	721
212	0	33	245	3551726	1443	0	90	90	2769	721
212	2	35	247	3551726	1443	0	96	96	2769	721
212	4	37	249	3551726	1443	0	102	102	2769	721
214	–4	28	242	3518354	1457	0	75	75	2776	728
214	–2	30	244	3518354	1457	0	81	81	2776	728
214	0	32	246	3518354	1457	0	86	86	2776	728
214	2	34	248	3518354	1457	0	92	92	2776	728
214	4	36	250	3518354	1457	0	98	98	2776	728
216	–4	27	243	3484982	1470	0	72	72	2782	734
216	–2	29	245	3484982	1470	0	77	77	2782	734
216	0	31	247	3484982	1470	0	82	82	2782	734
216	2	33	249	3484982	1470	0	88	88	2782	734
216	4	35	251	3484982	1470	0	94	94	2782	734
218	–4	26	244	3451610	1484	0	68	68	2789	741
218	–2	28	246	3451610	1484	0	73	73	2789	741
218	0	30	248	3451610	1484	0	79	79	2789	741
218	2	32	250	3451610	1484	0	85	85	2789	741
218	4	34	252	3451610	1484	0	90	90	2789	741
220	–4	25	245	3423006	1497	0	65	65	2796	748
220	–2	27	247	3423006	1497	0	71	71	2796	748
220	0	29	249	3423006	1497	0	76	76	2796	748
220	2	31	251	3423006	1497	0	81	81	2796	748
220	4	33	253	3423006	1497	0	87	87	2796	748
Full size (horizontal size: 710 pixels)										
241	0	18	259	3122659	1642	0	42	42	2867	819
Small size (horizontal size: 620 pixels)										
204	0	37	241	3689981	1389	0	106	106	2742	694

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Table 16: Y scaler programming at NTSC, input frame size: 800 × 600, half anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
212	–4	29	241	3551726	2165	2048	79	79	3129	57
212	–2	31	243	3551726	2165	2048	85	85	3129	57
212	0	33	245	3551726	2165	2048	91	91	3129	57
212	2	35	247	3551726	2165	2048	96	96	3129	57
212	4	37	249	3551726	2165	2048	102	102	3129	57
214	–4	28	242	3518354	2185	2048	75	75	3140	68
214	–2	30	244	3518354	2185	2048	81	81	3140	68
214	0	32	246	3518354	2185	2048	87	87	3140	68
214	2	34	248	3518354	2185	2048	92	92	3140	68
214	4	36	250	3518354	2185	2048	98	98	3140	68
216	–4	27	243	3484982	2205	2048	72	72	3150	78
216	–2	29	245	3484982	2205	2048	77	77	3150	78
216	0	31	247	3484982	2205	2048	83	83	3150	78
216	2	33	249	3484982	2205	2048	89	89	3150	78
216	4	35	251	3484982	2205	2048	94	94	3150	78
218	–4	26	244	3451610	2226	2048	68	68	3160	88
218	–2	28	246	3451610	2226	2048	74	74	3160	88
218	0	30	248	3451610	2226	2048	80	80	3160	88
218	2	32	250	3451610	2226	2048	85	85	3160	88
218	4	34	252	3451610	2226	2048	90	90	3160	88
220	–4	25	245	3423006	2246	2048	65	65	3170	98
220	–2	27	247	3423006	2246	2048	71	71	3170	98
220	0	29	249	3423006	2246	2048	76	76	3170	98
220	2	31	251	3423006	2246	2048	81	81	3170	98
220	4	33	253	3423006	2246	2048	87	87	3170	98
Full size (horizontal size: 710 pixels)										
241	0	18	259	3122659	2461	2048	42	42	3277	205
Small size (horizontal size: 620 pixels)										
204	0	37	241	3689981	2083	2048	106	106	3089	17

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Table 17: Y scaler programming at NTSC, input frame size: 800 × 600, no anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
212	–4	29	241	3551726	2887	4095	79	80	3490	2282
212	–2	31	243	3551726	2887	4095	85	86	3490	2282
212	0	33	245	3551726	2887	4095	91	92	3490	2282
212	2	35	247	3551726	2887	4095	96	97	3490	2282
212	4	37	249	3551726	2887	4095	102	103	3490	2282
214	–4	28	242	3518354	2912	4095	76	77	3504	2323
214	–2	30	244	3518354	2912	4095	81	82	3504	2323
214	0	32	246	3518354	2912	4095	87	88	3504	2323
214	2	34	248	3518354	2912	4095	92	93	3504	2323
214	4	36	250	3518354	2912	4095	98	99	3504	2323
216	–4	27	243	3484982	2941	4095	72	73	3517	2364
216	–2	29	245	3484982	2941	4095	78	79	3517	2364
216	0	31	247	3484982	2941	4095	83	84	3517	2364
216	2	33	249	3484982	2941	4095	89	90	3517	2364
216	4	35	251	3484982	2941	4095	94	95	3517	2364
218	–4	26	244	3451610	2969	4095	69	70	3531	2405
218	–2	28	246	3451610	2969	4095	74	75	3531	2405
218	0	30	248	3451610	2969	4095	80	81	3531	2405
218	2	32	250	3451610	2969	4095	85	86	3531	2405
218	4	34	252	3451610	2969	4095	90	91	3531	2405
220	–4	25	245	3423006	2994	4095	65	66	3544	2446
220	–2	27	247	3423006	2994	4095	71	72	3544	2446
220	0	29	249	3423006	2994	4095	76	77	3544	2446
220	2	31	251	3423006	2994	4095	82	83	3544	2446
220	4	33	253	3423006	2994	4095	87	88	3544	2446
Full size (horizontal size: 710 pixels)										
241	0	18	259	3122659	3282	4095	42	43	3687	2875
Small size (horizontal size: 620 pixels)										
204	0	37	241	3689981	2778	4095	106	107	3436	2119

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Table 18: Y scaler programming at PAL, input frame size: 640 × 400, full anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
255	–4	35	290	1528590	2600	0	52	52	3347	1299
255	–2	37	292	1528590	2602	0	55	55	3347	1299
255	0	39	294	1528590	2602	0	59	59	3347	1299
255	2	41	296	1528590	2602	0	62	62	3347	1299
255	4	43	298	1528590	2602	0	65	65	3347	1299
257	–4	34	291	1516163	2621	0	50	50	3357	1309
257	–2	36	293	1516163	2623	0	53	53	3357	1309
257	0	38	295	1516163	2623	0	57	57	3357	1309
257	2	40	297	1516163	2623	0	60	60	3357	1309
257	4	42	299	1516163	2623	0	63	63	3357	1309
259	–4	33	292	1506842	2641	0	49	49	3367	1319
259	–2	35	294	1506842	2641	0	52	52	3367	1319
259	0	37	296	1506842	2641	0	55	55	3367	1319
259	2	39	298	1506842	2641	0	58	58	3367	1319
259	4	41	300	1506842	2641	0	61	61	3367	1319
261	–4	32	293	1494414	2661	0	47	47	3377	1329
261	–2	34	295	1494414	2661	0	50	50	3377	1329
261	0	36	297	1494414	2661	0	53	53	3377	1329
261	2	38	299	1494414	2661	0	56	56	3377	1329
261	4	40	301	1494414	2661	0	59	59	3377	1329
263	–4	31	294	1481987	2684	0	45	45	3387	1339
263	–2	33	296	1481987	2684	0	48	48	3387	1339
263	0	35	298	1481987	2684	0	51	51	3387	1339
263	2	37	300	1481987	2684	0	54	54	3387	1339
263	4	39	302	1481987	2684	0	57	57	3387	1339
Full size (horizontal size: 702 pixels)										
288	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
250	0	41	291	1559659	2549	0	63	63	3321	1273

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Table 19: Y scaler programming at PAL, input frame size: 640 × 400, half anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
255	–4	35	290	1528590	3346	1170	53	53	3996	924
255	–2	37	292	1528590	3346	1170	56	56	3996	924
255	0	39	294	1528590	3346	1170	59	59	3996	924
255	2	41	296	1528590	3346	1170	62	62	3996	924
255	4	43	298	1528590	3346	1170	65	65	3996	924
257	–4	34	291	1516163	3360	1150	51	51	4012	940
257	–2	36	293	1516163	3360	1150	54	54	4012	940
257	0	38	295	1516163	3360	1150	57	57	4012	940
257	2	40	297	1516163	3360	1150	60	60	4012	940
257	4	42	299	1516163	3360	1150	63	63	4012	940
259	–4	33	292	1506842	3362	1120	49	49	4070	998
259	–2	35	294	1506842	3362	1120	52	52	4070	998
259	0	37	296	1506842	3362	1120	55	55	4070	998
259	2	39	298	1506842	3362	1120	58	58	4070	998
259	4	41	300	1506842	3362	1120	61	61	4070	998
261	–4	32	293	1494414	3378	1100	47	47	4042	970
261	–2	34	295	1494414	3378	1100	50	50	4042	970
261	0	36	297	1494414	3378	1100	53	53	4042	970
261	2	38	299	1494414	3378	1100	56	56	4042	970
261	4	40	301	1494414	3378	1100	59	59	4042	970
263	–4	31	294	1481987	3384	1070	45	45	4057	985
263	–2	33	296	1481987	3384	1070	48	48	4057	985
263	0	35	298	1481987	3384	1070	51	51	4057	985
263	2	37	300	1481987	3384	1070	54	54	4057	985
263	4	39	302	1481987	3384	1070	57	57	4057	985
Full size (horizontal size: 702 pixels)										
288	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
250	0	41	291	1559659	3322	1240	63	63	3707	1039

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Table 20: Y scaler programming at PAL, input frame size: 640 × 400, no anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
255	–4	35	290	1528590	4095	2350	53	53	4092	869
255	–2	37	292	1528590	4095	2350	56	56	4092	869
255	0	39	294	1528590	4095	2350	59	59	4092	869
255	2	41	296	1528590	4095	2350	62	62	4092	869
255	4	43	298	1528590	4095	2350	65	65	4092	869
257	–4	34	291	1516163	4095	2300	51	51	4092	894
257	–2	36	293	1516163	4095	2300	54	54	4092	894
257	0	38	295	1516163	4095	2300	57	57	4092	894
257	2	40	297	1516163	4095	2300	60	60	4092	894
257	4	42	299	1516163	4095	2300	63	63	4092	894
259	–4	33	292	1506842	4093	2250	49	49	4092	919
259	–2	35	294	1506842	4093	2250	52	52	4092	919
259	0	37	296	1506842	4093	2250	55	55	4092	919
259	2	39	298	1506842	4091	2250	58	58	4092	919
259	4	42	301	1506842	4091	2250	63	63	4092	919
261	–4	32	293	1494414	4094	2200	47	47	4092	944
261	–2	34	295	1494414	4094	2200	50	50	4092	944
261	0	36	297	1494414	4094	2200	53	53	4092	944
261	2	38	299	1494414	4093	2200	56	56	4092	944
261	4	40	301	1494414	4093	2200	59	59	4092	944
263	–4	31	294	1481987	4092	2150	45	45	4091	968
263	–2	33	296	1481987	4092	2150	48	48	4091	968
263	0	35	298	1481987	4092	2150	51	51	4091	968
263	2	37	300	1481987	4092	2150	54	54	4091	968
263	4	39	302	1481987	4092	2150	57	57	4091	968
Full size (horizontal size: 702 pixels)										
288	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
250	0	41	291	1559659	4087	2470	63	63	4089	806

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Table 21: Y scaler programming at PAL, input frame size: 640 × 480, full anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
255	–4	35	290	1833066	2168	0	63	63	3131	1083
255	–2	37	292	1833066	2168	0	67	67	3131	1083
255	0	39	294	1833066	2168	0	71	71	3131	1083
255	2	41	296	1833066	2168	0	74	74	3131	1083
255	4	43	298	1833066	2168	0	78	78	3131	1083
257	–4	34	291	1820638	2185	0	61	61	3139	1091
257	–2	36	293	1820638	2185	0	65	65	3139	1091
257	0	38	295	1820638	2185	0	69	69	3139	1091
257	2	40	297	1820638	2185	0	72	72	3139	1091
257	4	42	299	1820638	2185	0	76	76	3139	1091
259	–4	33	292	1805104	2202	0	58	58	3148	1100
259	–2	35	294	1805104	2202	0	62	62	3148	1100
259	0	37	296	1805104	2202	0	66	66	3148	1100
259	2	39	298	1805104	2204	0	70	70	3148	1100
259	4	41	300	1805104	2202	0	73	73	3148	1100
261	–4	32	293	1792676	2219	0	56	56	3156	1108
261	–2	34	295	1792676	2219	0	60	60	3156	1108
261	0	36	297	1792676	2219	0	64	64	3156	1108
261	2	38	299	1792676	2219	0	67	67	3156	1108
261	4	40	301	1792676	2219	0	71	71	3156	1108
263	–4	31	294	1777142	2238	0	54	54	3165	1117
263	–2	33	296	1777142	2238	0	58	58	3165	1117
263	0	35	298	1777142	2238	0	61	61	3165	1117
263	2	37	300	1777142	2238	0	65	65	3165	1117
263	4	39	302	1777142	2238	0	69	69	3165	1117
Full size (horizontal size: 702 pixels)										
288	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
250	0	41	291	1870348	2125	0	76	76	3110	1062

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Table 22: Y scaler programming at PAL, input frame size: 640 × 480, half anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
255	–4	35	290	1833066	3254	2048	63	63	3673	601
255	–2	37	292	1833066	3254	2048	67	67	3673	601
255	0	39	294	1833066	3254	2048	71	71	3673	601
255	2	41	296	1833066	3254	2048	75	75	3673	601
255	4	43	298	1833066	3254	2048	79	79	3673	601
257	–4	34	291	1820638	3277	2048	61	61	3686	614
257	–2	36	293	1820638	3277	2048	65	65	3686	614
257	0	38	295	1820638	3277	2048	69	69	3686	614
257	2	40	297	1820638	3277	2048	72	72	3686	614
257	4	42	299	1820638	3277	2048	76	76	3686	614
259	–4	33	292	1805104	3305	2048	59	59	3698	626
259	–2	35	294	1805104	3305	2048	63	63	3698	626
259	0	37	296	1805104	3305	2048	66	66	3698	626
259	2	39	298	1805104	3305	2048	70	70	3698	626
259	4	41	300	1805104	3305	2048	74	74	3698	626
261	–4	32	293	1792676	3328	2048	57	57	3711	639
261	–2	34	295	1792676	3328	2048	60	60	3711	639
261	0	36	297	1792676	3328	2048	64	64	3711	639
261	2	38	299	1792676	3328	2048	68	68	3711	639
261	4	40	301	1792676	3328	2048	71	71	3711	639
263	–4	31	294	1777142	3354	2048	54	54	3724	652
263	–2	33	296	1777142	3354	2048	58	58	3724	652
263	0	35	298	1777142	3354	2048	61	61	3724	652
263	2	37	300	1777142	3354	2048	65	65	3724	652
263	4	39	302	1777142	3354	2048	69	69	3724	652
Full size (horizontal size: 702 pixels)										
288	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
250	0	41	291	1870348	3108	1890	76	76	3600	607

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Table 23: Y scaler programming at PAL, input frame size: 640 × 480, no anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
255	–4	35	290	1833066	4093	3630	64	64	4091	228
255	–2	37	292	1833066	4093	3630	67	67	4091	228
255	0	39	294	1833066	4093	3630	71	71	4091	228
255	2	41	296	1833066	4093	3630	75	75	4091	228
255	4	43	298	1833066	4093	3630	79	79	4091	228
257	–4	34	291	1820638	4090	3570	61	61	4091	258
257	–2	36	293	1820638	4090	3570	65	65	4091	258
257	0	38	295	1820638	4090	3570	69	69	4091	258
257	2	40	297	1820638	4090	3570	73	73	4091	258
257	4	42	299	1820638	4090	3570	76	76	4091	258
259	–4	33	292	1805104	4092	3510	59	59	4091	288
259	–2	35	294	1805104	4092	3510	63	63	4091	288
259	0	37	296	1805104	4092	3510	66	66	4091	288
259	2	39	298	1805104	4092	3510	70	70	4091	288
259	4	41	300	1805104	4092	3510	74	74	4091	288
261	–4	32	293	1792676	4088	3450	57	57	4091	318
261	–2	34	295	1792676	4088	3450	60	60	4091	318
261	0	36	297	1792676	4088	3450	64	64	4091	318
261	2	38	299	1792676	4088	3450	68	68	4091	318
261	4	40	301	1792676	4088	3450	71	71	4091	318
263	–4	31	294	1777142	4095	3400	54	54	4095	345
263	–2	33	296	1777142	4095	3400	58	58	4095	345
263	0	35	298	1777142	4095	3400	62	62	4095	345
263	2	37	300	1777142	4095	3400	65	65	4095	345
263	4	39	302	1777142	4095	3400	69	69	4095	345
Full size (horizontal size: 702 pixels)										
288	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
250	0	41	291	1870348	4088	3780	76	76	4090	152

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Table 24: Y scaler programming at PAL, input frame size: 800 × 600, full anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
255	–4	35	290	2930917	1736	0	79	79	2915	867
255	–2	37	292	2930917	1736	0	84	84	2915	867
255	0	39	294	2930917	1736	0	89	89	2915	867
255	2	41	296	2930917	1736	0	93	93	2915	867
255	4	43	298	2930917	1736	0	98	98	2915	867
257	–4	34	291	2911033	1749	0	77	77	2922	874
257	–2	36	293	2911033	1749	0	81	81	2922	874
257	0	38	295	2911033	1749	0	86	86	2922	874
257	2	40	297	2911033	1749	0	91	91	2922	874
257	4	42	299	2911033	1749	0	95	95	2922	874
259	–4	33	292	2887172	1763	0	73	73	2929	881
259	–2	35	294	2887172	1763	0	78	78	2929	881
259	0	37	296	2887172	1763	0	83	83	2929	881
259	2	39	298	2887172	1763	0	87	87	2929	881
259	4	41	300	2887172	1763	0	92	92	2929	881
261	–4	32	293	2863311	1778	0	71	71	2935	887
261	–2	34	295	2863311	1778	0	75	75	2935	887
261	0	36	297	2863311	1778	0	80	80	2935	887
261	2	38	299	2863311	1778	0	85	85	2935	887
261	4	40	301	2863311	1778	0	89	89	2935	887
263	–4	31	294	2843427	1790	0	68	68	2942	894
263	–2	33	296	2843427	1790	0	72	72	2942	894
263	0	35	298	2843427	1790	0	77	77	2942	894
263	2	37	300	2843427	1790	0	82	82	2942	894
263	4	39	302	2843427	1790	0	86	86	2942	894
Full size (horizontal size: 702 pixels)										
288	0	22	310	2596864	1960	0	43	43	3027	979
Small size (horizontal size: 620 pixels)										
250	0	41	291	2990569	1701	0	95	95	2898	850

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Table 25: Y scaler programming at PAL, input frame size: 800 × 600, half anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
255	–4	35	290	2930917	2604	2048	80	80	3349	277
255	–2	37	292	2930917	2604	2048	84	84	3349	277
255	0	39	294	2930917	2604	2048	89	89	3349	277
255	2	41	296	2930917	2604	2048	94	94	3349	277
255	4	43	298	2930917	2604	2048	98	98	3349	277
257	–4	34	291	2911033	2625	2048	77	77	3359	287
257	–2	36	293	2911033	2625	2048	82	82	3359	287
257	0	38	295	2911033	2625	2048	86	86	3359	287
257	2	40	297	2911033	2625	2048	91	91	3359	287
257	4	42	299	2911033	2625	2048	96	96	3359	287
259	–4	33	292	2887172	2645	2048	74	74	3369	297
259	–2	35	294	2887172	2645	2048	79	79	3369	297
259	0	37	296	2887172	2645	2048	83	83	3369	297
259	2	39	298	2887172	2645	2048	88	88	3369	297
259	4	41	300	2887172	2645	2048	92	92	3369	297
261	–4	32	293	2863311	2666	2048	71	71	3379	307
261	–2	34	295	2863311	2666	2048	75	75	3379	307
261	0	36	297	2863311	2666	2048	80	80	3379	307
261	2	38	299	2863311	2666	2048	85	85	3379	307
261	4	40	301	2863311	2666	2048	89	89	3379	307
263	–4	31	294	2843427	2686	2048	68	68	3390	318
263	–2	33	296	2843427	2686	2048	73	73	3390	318
263	0	35	298	2843427	2686	2048	77	77	3390	318
263	2	37	300	2843427	2686	2048	82	82	3390	318
263	4	39	302	2843427	2686	2048	86	86	3390	318
Full size (horizontal size: 702 pixels)										
288	0	22	310	2596864	2940	2048	43	43	3517	445
Small size (horizontal size: 620 pixels)										
250	0	41	291	2990569	2553	2048	96	96	3323	251

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Table 26: Y scaler programming at PAL, input frame size: 800 × 600, no anti-flicker filter

TV line	Offset	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ± 10 pixels)										
255	–4	35	290	2930917	3473	4095	80	81	3783	3161
255	–2	37	292	2930917	3473	4095	84	85	3783	3161
255	0	39	294	2930917	3473	4095	89	90	3783	3161
255	2	41	296	2930917	3473	4095	94	95	3783	3161
255	4	43	298	2930917	3473	4095	99	100	3783	3161
257	–4	34	291	2911033	3500	4095	77	78	3796	3202
257	–2	36	293	2911033	3500	4095	82	83	3796	3202
257	0	38	295	2911033	3500	4095	87	88	3796	3202
257	2	40	297	2911033	3500	4095	91	92	3796	3202
257	4	42	299	2911033	3500	4095	96	97	3796	3202
259	–4	33	292	2887172	3527	4095	74	75	3810	3242
259	–2	35	294	2887172	3527	4095	79	80	3810	3242
259	0	37	296	2887172	3527	4095	83	84	3810	3242
259	2	39	298	2887172	3527	4095	88	89	3810	3242
259	4	41	300	2887172	3527	4095	93	94	3810	3242
261	–4	32	293	2863311	3555	4095	71	72	3823	3284
261	–2	34	295	2863311	3555	4095	76	77	3823	3284
261	0	36	297	2863311	3555	4095	80	81	3823	3284
261	2	38	299	2863311	3555	4095	85	86	3823	3284
261	4	40	301	2863311	3555	4095	89	90	3823	3284
263	–4	31	294	2843427	3582	4095	68	69	3837	3324
263	–2	33	296	2843427	3582	4095	73	74	3837	3324
263	0	35	298	2843427	3582	4095	78	79	3837	3324
263	2	37	300	2843427	3582	4095	82	83	3837	3324
263	4	39	302	2843427	3582	4095	87	88	3837	3324
Full size (horizontal size: 702 pixels)										
288	0	22	310	2596864	3923	4095	44	45	4007	3836
Small size (horizontal size: 620 pixels)										
250	0	41	291	2990569	3405	4095	96	97	3748	3059

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Table 27: *"ITU-R BT.601"* signal component levels

Color	Signals [1]					
	Y	C_B	C_R	R	G	B
White	235	128	128	235	235	235
Yellow	210	16	146	235	235	16
Cyan	170	166	16	16	235	235
Green	145	54	34	16	235	16
Magenta	106	202	222	235	16	235
Red	81	90	240	235	16	16
Blue	41	240	110	16	16	235
Black	16	128	128	16	16	16

[1] Transformation:

$R = Y + 1.3707 \times (C_R - 128)$

$G = Y - 0.3365 \times (C_B - 128) - 0.6982 \times (C_R - 128)$

$B = Y + 1.7324 \times (C_B - 128)$.

Table 28: Pin assignment for input format 0

8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB/C_B-Y-C_R		
Pin	**Falling clock edge**	**Rising clock edge**
PD11	G3/Y3	R7/C_R7
PD10	G2/Y2	R6/C_R6
PD9	G1/Y1	R5/C_R5
PD8	G0/Y0	R4/C_R4
PD7	B7/C_B7	R3/C_R3
PD6	B6/C_B6	R2/C_R2
PD5	B5/C_B5	R1/C_R1
PD4	B4/C_B4	R0/C_R0
PD3	B3/C_B3	G7/Y7
PD2	B2/C_B2	G6/Y6
PD1	B1/C_B1	G5/Y5
PD0	B0/C_B0	G4/Y4

Table 29: Pin assignment for input format 1

5 + 5 + 5-bit 4 : 4 : 4 non-interlaced RGB		
Pin	**Falling clock edge**	**Rising clock edge**
PD7	G2	X
PD6	G1	R4
PD5	G0	R3
PD4	B4	R2
PD3	B3	R1
PD2	B2	R0
PD1	B1	G4
PD0	B0	G3

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Table 30: Pin assignment for input format 2

5 + 6 + 5-bit 4 : 4 : 4 non-interlaced RGB		
Pin	**Falling clock edge**	**Rising clock edge**
PD7	G2	R4
PD6	G1	R3
PD5	G0	R2
PD4	B4	R1
PD3	B3	R0
PD2	B2	G5
PD1	B1	G4
PD0	B0	G3

Table 31: Pin assignment for input format 3

8 + 8 + 8-bit 4 : 2 : 2 non-interlaced C_B-Y-C_R				
Pin	**Falling clock edge n**	**Rising clock edge n**	**Falling clock edge n + 1**	**Rising clock edge n + 1**
PD7	$C_B7(0)$	Y7(0)	$C_R7(0)$	Y7(1)
PD6	$C_B6(0)$	Y6(0)	$C_R6(0)$	Y6(1)
PD5	$C_B5(0)$	Y5(0)	$C_R5(0)$	Y5(1)
PD4	$C_B4(0)$	Y4(0)	$C_R4(0)$	Y4(1)
PD3	$C_B3(0)$	Y3(0)	$C_R3(0)$	Y3(1)
PD2	$C_B2(0)$	Y2(0)	$C_R2(0)$	Y2(1)
PD1	$C_B1(0)$	Y1(0)	$C_R1(0)$	Y1(1)
PD0	$C_B0(0)$	Y0(0)	$C_R0(0)$	Y0(1)

Table 32: Pin assignment for input format 4

8 + 8 + 8-bit 4 : 2 : 2 interlaced C_B-Y-C_R (ITU-R BT.656, 27 MHz clock)				
Pin	**Rising clock edge n**	**Rising clock edge n + 1**	**Rising clock edge n + 2**	**Rising clock edge n + 3**
PD7	$C_B7(0)$	Y7(0)	$C_R7(0)$	Y7(1)
PD6	$C_B6(0)$	Y6(0)	$C_R6(0)$	Y6(1)
PD5	$C_B5(0)$	Y5(0)	$C_R5(0)$	Y5(1)
PD4	$C_B4(0)$	Y4(0)	$C_R4(0)$	Y4(1)
PD3	$C_B3(0)$	Y3(0)	$C_R3(0)$	Y3(1)
PD2	$C_B2(0)$	Y2(0)	$C_R2(0)$	Y2(1)
PD1	$C_B1(0)$	Y1(0)	$C_R1(0)$	Y1(1)
PD0	$C_B0(0)$	Y0(0)	$C_R0(0)$	Y0(1)

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Table 33: Pin assignment for input format 5 [1]

8-bit non-interlaced index color		
Pin	**Falling clock edge**	**Rising clock edge**
PD11	X	X
PD10	X	X
PD9	X	X
PD8	X	X
PD7	INDEX7	X
PD6	INDEX6	X
PD5	INDEX5	X
PD4	INDEX4	X
PD3	INDEX3	X
PD2	INDEX2	X
PD1	INDEX1	X
PD0	INDEX0	X

[1] X = don't care.

Table 34: Pin assignment for input format 6

8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB/C_B-Y-C_R		
Pin	**Falling clock edge**	**Rising clock edge**
PD11	G4/Y4	R7/C_R7
PD10	G3/Y3	R6/C_R6
PD9	G2/Y2	R5/C_R5
PD8	B7/C_B7	R4/C_R4
PD7	B6/C_B6	R3/C_R3
PD6	B5/C_B5	G7/Y7
PD5	B4/C_B4	G6/Y6
PD4	B3/C_B3	G5/Y5
PD3	G0/Y0	R2/C_R2
PD2	B2/C_B2	R1/C_R1
PD1	B1/C_B1	R0/C_R0
PD0	B0/C_B0	G1/Y1

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8. Register description

8.1 Bit allocation map

Table 35: Slave receiver (slave address 88h)

Register function	Subaddress (hexadecimal)	7	6	5	4	3	2	1	0
Status byte (read only)	00	VER2	VER1	VER0	CCRDO	CCRDE	-	FSEQ	O_E
Null	01 to 15	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Common DAC adjust fine	16	[1]	[1]	[1]	[1]	DACF3	DACF2	DACF1	DACF0
R DAC adjust coarse	17	[1]	[1]	[1]	RDACC4	RDACC3	RDACC2	RDACC1	RDACC0
G DAC adjust coarse	18	[1]	[1]	[1]	GDACC4	GDACC3	GDACC2	GDACC1	GDACC0
B DAC adjust coarse	19	[1]	[1]	[1]	BDACC4	BDACC3	BDACC2	BDACC1	BDACC0
MSM threshold	1A	MSMT7	MSMT6	MSMT5	MSMT4	MSMT3	MSMT2	MSMT1	MSMT0
Monitor sense mode	1B	MSM	[1]	[1]	[1]	[1]	RCOMP	GCOMP	BCOMP
Chip ID (02h or 03h, read only)	1C	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
Wide screen signal	26	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27	WSSON	[1]	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Real-time control, burst start	28	[1]	[1]	BS5	BS4	BS3	BS2	BS1	BS0
Sync reset enable, burst end	29	SRES	[1]	BE5	BE4	BE3	BE2	BE1	BE0
Copy generation 0	2A	CG07	CG06	CG05	CG04	CG03	CG02	CG01	CG00
Copy generation 1	2B	CG15	CG14	CG13	CG12	CG11	CG10	CG09	CG08
CG enable, copy generation 2	2C	CGEN	[1]	[1]	[1]	CG19	CG18	CG17	CG16
Output port control	2D	VBSEN	CVBSEN1	CVBSEN0	CEN	ENCOFF	CLK2EN	[1]	[1]
Null	2E to 37	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Gain luminance for RGB	38	[1]	[1]	[1]	GY4	GY3	GY2	GY1	GY0
Gain color difference for RGB	39	[1]	[1]	[1]	GCD4	GCD3	GCD2	GCD1	GCD0
Input port control 1	3A	CBENB	[1]	[1]	SYMP	DEMOFF	CSYNC	Y2C	UV2C
VPS enable, input control 2	54	VPSEN	[1]	[1]	[1]	[1]	[1]	EDGE2	EDGE1
VPS byte 5	55	VPS57	VPS56	VPS55	VPS54	VPS53	VPS52	VPS51	VPS50
VPS byte 11	56	VPS117	VPS116	VPS115	VPS114	VPS113	VPS112	VPS111	VPS110
VPS byte 12	57	VPS127	VPS126	VPS125	VPS124	VPS123	VPS122	VPS121	VPS120
VPS byte 13	58	VPS137	VPS136	VPS135	VPS134	VPS133	VPS132	VPS131	VPS130
VPS byte 14	59	VPS147	VPS146	VPS145	VPS144	VPS143	VPS142	VPS141	VPS140
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0

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Table 35: Slave receiver (slave address 88h) *...continued*

Register function	Subaddress (hexadecimal)	7	6	5	4	3	2	1	0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	[1]	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	[1]	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, blanking level VBI	5F	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Standard control	61	DOWND	DOWNA	[1]	YGS	[1]	SCBW	PAL	FISE
Burst amplitude	62	[1]	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
Null	6B	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Trigger control	6C	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6D	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6E	[1]	BLCKON	PHRES1	PHRES0	LDEL1	LDEL0	FLC1	FLC0
Closed caption, teletext enable	6F	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
Active display window horizontal start	70	ADWHS7	ADWHS6	ADWHS5	ADWHS4	ADWHS3	ADWHS2	ADWHS1	ADWHS0
Active display window horizontal end	71	ADWHE7	ADWHE6	ADWHE5	ADWHE4	ADWHE3	ADWHE2	ADWHE1	ADWHE0
MSBs ADWH	72	[1]	ADWHE10	ADWHE9	ADWHE8	[1]	ADWHS10	ADWHS9	ADWHS8
TTX request horizontal start	73	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request horizontal delay	74	[1]	[1]	[1]	[1]	TTXHD3	TTXHD2	TTXHD1	TTXHD0
CSYNC advance	75	CSYNCA4	CSYNCA3	CSYNCA2	CSYNCA1	CSYNCA0	[1]	[1]	[1]
TTX odd request vertical start	76	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request vertical end	77	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0
TTX even request vertical start	78	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0

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Table 35: Slave receiver (slave address 88h) *...continued*

Register function	Subaddress (hexadecimal)	7	6	5	4	3	2	1	0
TTX even request vertical end	79	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7A	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7B	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
TTX mode, MSB vertical	7C	TTX60	LAL8	[1]	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7D	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Disable TTX line	7E	LINE12	LINE11	LINE10	LINE9	LINE8	LINE7	LINE6	LINE5
Disable TTX line	7F	LINE20	LINE19	LINE18	LINE17	LINE16	LINE15	LINE14	LINE13
FIFO status (read only)	80	-	-	-	-	-	-	OVFL	UDFL
Pixel clock 0	81	PCL07	PCL06	PCL05	PCL04	PCL03	PCL02	PCL01	PCL00
Pixel clock 1	82	PCL15	PCL14	PCL13	PCL12	PCL11	PCL10	PCL09	PCL08
Pixel clock 2	83	PCL23	PCL22	PCL21	PCL20	PCL19	PCL18	PCL17	PCL16
Null	84 to 8F	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Horizontal offset	90	XOFS7	XOFS6	XOFS5	XOFS4	XOFS3	XOFS2	XOFS1	XOFS0
Pixel number	91	XPIX7	XPIX6	XPIX5	XPIX4	XPIX3	XPIX2	XPIX1	XPIX0
Vertical offset odd	92	YOFSO7	YOFSO6	YOFSO5	YOFSO4	YOFSO3	YOFSO2	YOFSO1	YOFSO0
Vertical offset even	93	YOFSE7	YOFSE6	YOFSE5	YOFSE4	YOFSE3	YOFSE2	YOFSE1	YOFSE0
MSBs	94	YOFSE9	YOFSE8	YOFSO9	YOFSO8	XPIX9	XPIX8	XOFS9	XOFS8
Line number	95	YPIX7	YPIX6	YPIX5	YPIX4	YPIX3	YPIX2	YPIX1	YPIX0
Scaler CTRL, MCB YPIX	96	EFS	PCBN	SLAVE	ILC	YFIL	HSL	YPIX9	YPIX8
Sync control	97	HFS	VFS	OFS	PFS	OVS	PVS	OHS	PHS
Line length	98	HLEN7	HLEN6	HLEN5	HLEN4	HLEN3	HLEN2	HLEN1	HLEN0
Input delay, MSB line length	99	IDEL3	IDEL2	IDEL1	IDEL0	[1]	HLEN10	HLEN9	HLEN8
Horizontal increment	9A	XINC7	XINC6	XINC5	XINC4	XINC3	XINC2	XINC1	XINC0
Vertical increment	9B	YINC7	YINC6	YINC5	YINC4	YINC3	YINC2	YINC1	YINC0
MSBs vertical and horizontal increment	9C	YINC11	YINC10	YINC9	YINC8	XINC11	XINC10	XINC9	XINC8
Weighting factor odd	9D	YIWGTO7	YIWGTO6	YIWGTO5	YIWGTO4	YIWGTO3	YIWGTO2	YIWGTO1	YIWGTO0
Weighting factor even	9E	YIWGTE7	YIWGTE6	YIWGTE5	YIWGTE4	YIWGTE3	YIWGTE2	YIWGTE1	YIWGTE0
Weighting factor MSB	9F	YIWGTE11	YIWGTE10	YIWGTE9	YIWGTE8	YIWGTO11	YIWGTO10	YIWGTO9	YIWGTO8
Vertical line skip	A0	YSKIP7	YSKIP6	YSKIP5	YSKIP4	YSKIP3	YSKIP2	YSKIP1	YSKIP0

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Table 35: Slave receiver (slave address 88h) *...continued*

Register function	Subaddress (hexadecimal)	7	6	5	4	3	2	1	0
Blank enable for NI-bypass, vertical line skip MSB	A1	BLEN	[1]	[1]	[1]	YSKIP11	YSKIP10	YSKIP9	YSKIP8
Border color Y	A2	BCY7	BCY6	BCY5	BCY4	BCY3	BCY2	BCY1	BCY0
Border color U	A3	BCU7	BCU6	BCU5	BCU4	BCU3	BCU2	BCU1	BCU0
Border color V	A4	BCV7	BCV6	BCV5	BCV4	BCV3	BCV2	BCV1	BCV0
Cursor color 1 R	F0	CC1R7	CC1R6	CC1R5	CC1R4	CC1R3	CC1R2	CC1R1	CC1R0
Cursor color 1 G	F1	CC1G7	CC1G6	CC1G5	CC1G4	CC1G3	CC1G2	CC1G1	CC1G0
Cursor color 1 B	F2	CC1B7	CC1B6	CC1B5	CC1B4	CC1B3	CC1B2	CC1B1	CC1B0
Cursor color 2 R	F3	CC2R7	CC2R6	CC2R5	CC2R4	CC2R3	CC2R2	CC2R1	CC2R0
Cursor color 2 G	F4	CC2G7	CC2G6	CC2G5	CC2G4	CC2G3	CC2G2	CC2G1	CC2G0
Cursor color 2 B	F5	CC2B7	CC2B6	CC2B5	CC2B4	CC2B3	CC2B2	CC2B1	CC2B0
Auxiliary cursor color R	F6	AUXR7	AUXR6	AUXR5	AUXR4	AUXR3	AUXR2	AUXR1	AUXR0
Auxiliary cursor color G	F7	AUXG7	AUXG6	AUXG5	AUXG4	AUXG3	AUXG2	AUXG1	AUXG0
Auxiliary cursor color B	F8	AUXB7	AUXB6	AUXB5	AUXB4	AUXB3	AUXB2	AUXB1	AUXB0
Horizontal cursor position	F9	XCP7	XCP6	XCP5	XCP4	XCP3	XCP2	XCP1	XCP0
Horizontal hot spot, MSB XCP	FA	XHS4	XHS3	XHS2	XHS1	XHS0	XCP10	XCP9	XCP8
Vertical cursor position	FB	YCP7	YCP6	YCP5	YCP4	YCP3	YCP2	YCP1	YCP0
Vertical hot spot, MSB YCP	FC	YHS4	YHS3	YHS2	YHS1	YHS0	[1]	YCP9	YCP8
Input path control	FD	LUTOFF	CMODE	LUTL	IF2	IF1	IF0	MATOFF	DFOFF
Cursor bit map	FE	RAM address (see Table 102)							
Color look-up table	FF	RAM address (see Table 103)							

[1] All unused control bits must be programmed with logic 0 to ensure compatibility to future enhancements.

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8.2 I²C-bus format

S	1000 1000	A	SUBADDRESS	A	DATA 0	A	.....	DATA n	A	P

001aad411

a. to control registers

S	1000 1000	A	FEh	A	RAM ADDRESS	A	DATA 0	A	.....	DATA n	A	P

001aad413

b. to cursor bit map (subaddress FEh)

S	1000 1000	A	FFh	A	RAM ADDRESS	A	DATA 0R	A	DATA 0G	A	DATA 0B	A	.....	P

001aad414

c. to color look-up table (subaddress FFh)

See Table 36 for explanations.

Fig 4. I²C-bus write access

S	1000 1000	A	SUBADDRESS	A	Sr	1000 1001	A	DATA 0	Am	.....	DATA n	Am	P

001aad415

a. to control registers

S	1000 1000	A	FEh or FFh	A	RAM ADDRESS	A	Sr	1000 1001	A	DATA 0	Am	.....	DATA n	Am	P

001aad416

b. to cursor bit map or color LUT

See Table 36 for explanations.

Fig 5. I²C-bus read access

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Table 36: Explanations of Figure 4 and Figure 5

Code	Description
S	START condition
Sr	repeated START condition
1000 100X [1]	slave address
A	acknowledge generated by the slave
Am	acknowledge generated by the master
SUBADDRESS [2]	subaddress byte
DATA	data byte
--------	continued data bytes and acknowledges
P	STOP condition
RAM ADDRESS	start address for RAM access

[1] X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read.

[2] If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

8.3 Slave receiver

Table 37: Common DAC adjust fine register, subaddress 16h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	DACF[3:0]	R/W		DAC fine output voltage adjustment, 1 % steps for all DACs
			0111	7 %
			0110	6 %
			0101	5 %
			0100	4 %
			0011	3 %
			0010	2 %
			0001	1 %
			0000*	0 %
			1000	0 %
			1001	–1 %
			1010	–2 %
			1011	–3 %
			1100	–4 %
			1101	–5 %
			1110	–6 %
			1111	–7 %

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Table 38: RGB DAC adjust coarse registers, subaddresses 17h to 19h, bit description

Subaddress	Bit	Symbol	Description
17h to 19h	7 to 5	-	must be programmed with logic 0 to ensure compatibility to future enhancements
17h	4 to 0	RDACC[4:0]	output level coarse adjustment for RED DAC; default after reset is 1Bh for output of C signal 0 0000b ≡ 0.585 V to 1 1111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion
18h	4 to 0	GDACC[4:0]	output level coarse adjustment for GREEN DAC; default after reset is 1Bh for output of VBS signal 0 0000b ≡ 0.585 V to 1 1111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion
19h	4 to 0	BDACC[4:0]	output level coarse adjustment for BLUE DAC; default after reset is 1Fh for output of CVBS signal 0 0000b ≡ 0.585 V to 1 1111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion

Table 39: MSM threshold, subaddress 1Ah, bit description

Bit	Symbol	Description
7 to 0	MSMT[7:0]	monitor sense mode threshold for DAC output voltage, should be set to 70h

Table 40: Monitor sense mode register, subaddress 1Bh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	MSM	R/W		monitor sense mode
			0*	off; RCOMP, GCOMP and BCOMP bits are not valid
			1	on
6 to 3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
2	RCOMP	R		check comparator at DAC on pin RED_CR_C
			0	active, output is loaded
			1	inactive, output is not loaded
1	GCOMP	R		check comparator at DAC on pin GREEN_VBS_CVBS
			0	active, output is loaded
			1	inactive, output is not loaded
0	BCOMP	R		check comparator at DAC on pin BLUE_CB_CVBS
			0	active, output is loaded
			1	inactive, output is not loaded

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Table 41: Wide screen signal registers, subaddresses 26h and 27h, bit description
*Legend: * = default value after reset.*

Subaddress	Bit	Symbol	Access	Value	Description
27h	7	WSSON	R/W	0*	wide screen signalling output is disabled
				1	wide screen signalling output is enabled
	6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	5 to 3	WSS[13:11]	R/W	-	wide screen signalling bits, reserved
	2 to 0	WSS[10:8]	R/W	-	wide screen signalling bits, subtitles
26h	7 to 4	WSS[7:4]	R/W	-	wide screen signalling bits, enhanced services
	3 to 0	WSS[3:0]	R/W	-	wide screen signalling bits, aspect ratio

Table 42: Real-time control and burst start register, subaddress 28h, bit description
*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 and 6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5 to 0	BS[5:0]	R/W		starting point of burst in clock cycles
			21h*	PAL: BS = 33; strapping pin FSVGC tied to HIGH
			19h*	NTSC: BS = 25; strapping pin FSVGC tied to LOW

Table 43: Sync reset enable and burst end register, subaddress 29h, bit description
*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	SRES	R/W	0*	pin TTX_SRES accepts a teletext bit stream (TTX)
			1	pin TTX_SRES accepts a sync reset input (SRES); a HIGH impulse resets synchronization of the encoder (first field, first line)
6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5 to 0	BE[5:0]	R/W		ending point of burst in clock cycles
			1Dh*	PAL: BE = 29; strapping pin FSVGC tied to HIGH
			1Dh*	NTSC: BE = 29; strapping pin FSVGC tied to LOW

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Table 44: Copy generation 0, 1, 2 and CG enable registers, subaddresses 2Ah to 2Ch, bit description

*Legend: * = default value after reset.*

Subaddress	Bit	Symbol	Access	Value	Description
2Ch	7	CGEN	R/W		copy generation data output
				0*	disabled
				1	enabled
	6 to 4	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	3 to 0	CG[19:16]	R/W	-	LSBs of the respective bytes are encoded immediately after run-in, the MSBs of the respective bytes have to carry the CRCC bits, in accordance with the definition of copy generation management system encoding format.
2Bh	7 to 0	CG[15:8]			
2Ah	7 to 0	CG[7:0]			

Table 45: Output port control register, subaddress 2Dh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	VBSEN	R/W		pin GREEN_VBS_CVBS provides a
			0	component GREEN signal (CVBSEN1 = 0) or CVBS signal (CVBSEN1 = 1)
			1*	luminance (VBS) signal
6	CVBSEN1	R/W		pin GREEN_VBS_CVBS provides a
			0*	component GREEN (G) or luminance (VBS) signal
			1	CVBS signal
5	CVBSEN0	R/W		pin BLUE_CB_CVBS provides a
			0	component BLUE (B) or color difference BLUE (C_B) signal
			1*	CVBS signal
4	CEN	R/W		pin RED_CR_C provides a
			0	component RED (R) or color difference RED (C_R) signal
			1*	chrominance signal (C) as modulated subcarrier for S-video
3	ENCOFF	R/W		encoder
			0*	active
			1	bypass, DACs are provided with RGB signal after cursor insertion block
2	CLK2EN	R/W		pin TTXRQ_XCLKO2 provides
			0	teletext request signal (TTXRQ)
			1*	buffered crystal clock divided by two (13.5 MHz)
1 and 0	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements

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Table 46: Gain luminance for RGB register, subaddress 38h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
4 to 0	GY[4:0]	R/W	-	Gain luminance of RGB (C_R, Y and C_B) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$. Suggested nominal value = 0, depending on external application.

Table 47: Gain color difference for RGB register, subaddress 39h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
4 to 0	GCD[4:0]	R/W	-	Gain color difference of RGB (C_R, Y and C_B) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$. Suggested nominal value = 0, depending on external application.

Table 48: Input port control 1 register, subaddress 3Ah, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	CBENB	R/W	0	data from input ports is encoded
			1	color bar with fixed colors is encoded
6 and 5	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
4	SYMP	R/W		horizontal and vertical trigger
			0*	taken from FSVGC or both VSVGC and HSVGC
			1	decoded out of *'ITU-R BT.656'* compatible data at PD port
3	DEMOFF	R/W		$Y\text{-}C_B\text{-}C_R$ to RGB dematrix
			0*	active
			1	bypassed
2	CSYNC	R/W		pin HSM_CSYNC provides
			0	horizontal sync for non-interlaced VGA components output (at PIXCLK)
			1	composite sync for interlaced components output (at XTAL clock)
1	Y2C	R/W		input luminance data
			0	twos complement from PD input port
			1*	straight binary from PD input port
0	UV2C	R/W		input color difference data
			0	twos complement from PD input port
			1*	straight binary from PD input port

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Table 49: VPS enable, input control 2, subaddress 54h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	VPSEN	R/W		video programming system data insertion
			0*	is disabled
			1	in line 16 is enabled
6 to 2	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
1	EDGE2	R/W		internal PPD2 data is sampled with
			0	rising clock edges
			1*	falling clock edges; see Table 28 to Table 34
0	EDGE1	R/W		internal PPD1 data is sampled with
			0*	rising clock edges
			1	falling clock edges; see Table 28 to Table 34

Table 50: VPS byte 5, 11, 12, 13 and 14 registers, subaddresses 55h to 59h, bit description [1]

Subaddress	Bit	Symbol	Access	Value	Description
55h	7 to 0	VPS5[7:0]	R/W	-	fifth byte of video programming system data
56h	7 to 0	VPS11[7:0]	R/W	-	eleventh byte of video programming system data
57h	7 to 0	VPS12[7:0]	R/W	-	twelfth byte of video programming system data
58h	7 to 0	VPS13[7:0]	R/W	-	thirteenth byte of video programming system data
59h	7 to 0	VPS14[7:0]	R/W	-	fourteenth byte of video programming system data

[1] In line 16; LSB first; all other bytes are not relevant for VPS.

Table 51: Chrominance phase register, subaddress 5Ah, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	CHPS[7:0]	R/W	00h*	phase of encoded color subcarrier (including burst) relative to horizontal sync; can be adjusted in steps of 360/256 degrees
			6Bh	PAL B/G and data from input ports in Master mode
			16h	PAL B/G and data from look-up table
			25h	NTSC M and data from input ports in Master mode
			46h	NTSC M and data from look-up table

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Table 52: Gain U and gain U MSB, black level registers, subaddresses 5Bh and 5Dh, bit description

Subaddress	Bit	Symbol	Conditions	Remarks
5Bh	7 to 0	GAINU[8:0] [1]	white-to-black = 92.5 IRE	GAINU = –2.17 × nominal to +2.16 × nominal
5Dh	7		GAINU = 0	output subcarrier of U contribution = 0
			GAINU = 118 (76h)	output subcarrier of U contribution = nominal
			white-to-black = 100 IRE	GAINU = –2.05 × nominal to +2.04 × nominal
			GAINU = 0	output subcarrier of U contribution = 0
			GAINU = 125 (7Dh)	output subcarrier of U contribution = nominal
	6	-	must be programmed with logic 0 to ensure compatibility to future enhancements	
	5 to 0	BLCKL[5:0] [2]	white-to-sync = 140 IRE [3]	recommended value: BLCKL = 58 (3Ah)
			BLCKL = 0 [3]	output black level = 29 IRE
			BLCKL = 63 (3Fh) [3]	output black level = 49 IRE
			white-to-sync = 143 IRE [4]	recommended value: BLCKL = 51 (33h)
			BLCKL = 0 [4]	output black level = 27 IRE
			BLCKL = 63 (3Fh) [4]	output black level = 47 IRE

[1] Variable gain for C_B signal; input representation in accordance with *'ITU-R BT.601'*.

[2] Variable black level; input representation in accordance with *'ITU-R BT.601'*.

[3] Output black level/IRE = BLCKL × 2/6.29 + 28.9.

[4] Output black level/IRE = BLCKL × 2/6.18 + 26.5.

Table 53: Gain V and gain V MSB, blanking level registers, subaddresses 5Ch and 5Eh, bit description

Subaddress	Bit	Symbol	Conditions	Remarks
5Ch	7 to 0	GAINV[8:0] [1]	white-to-black = 92.5 IRE	GAINV = –1.55 × nominal to +1.55 × nominal
5Eh	7		GAINV = 0	output subcarrier of V contribution = 0
			GAINV = 165 (A5h)	output subcarrier of V contribution = nominal
			white-to-black = 100 IRE	GAINV = –1.46 × nominal to +1.46 × nominal
			GAINV = 0	output subcarrier of V contribution = 0
			GAINV = 175 (AFh)	output subcarrier of V contribution = nominal
	6	-	must be programmed with logic 0 to ensure compatibility to future enhancements	
	5 to 0	BLNNL[5:0] [2]	white-to-sync = 140 IRE [3]	recommended value: BLNNL = 46 (2Eh)
			BLNNL = 0 [3]	output blanking level = 25 IRE
			BLNNL = 63 (3Fh) [3]	output blanking level = 45 IRE
			white-to-sync = 143 IRE [4]	recommended value: BLNNL = 53 (35h)
			BLNNL = 0 [4]	output blanking level = 26 IRE
			BLNNL = 63 (3Fh) [4]	output blanking level = 46 IRE

[1] Variable gain for C_R signal; input representation in accordance with *'ITU-R BT.601'*.

[2] Variable blanking level.

[3] Output black level/IRE = BLNNL × 2/6.29 + 25.4.

[4] Output black level/IRE = BLNNL × 2/6.18 + 25.9; default after reset: 35h.

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Table 54: CCR and blanking level VBI register, subaddress 5Fh, bit description

Bit	Symbol	Access	Value	Description
7 and 6	CCRS[1:0]	R/W		select cross-color reduction filter in luminance; for overall transfer characteristic of luminance see Figure 8
			00	no cross-color reduction
			01	cross-color reduction #1 active
			10	cross-color reduction #2 active
			11	cross-color reduction #3 active
5 to 0	BLNVB[5:0]	R/W	-	variable blanking level during vertical blanking interval is typically identical to value of BLNNL

Table 55: Standard control register, subaddress 61h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	DOWND	R/W		digital core
			0*	in normal operational mode
			1	in Sleep mode and is reactivated with an I^2C-bus address
6	DOWNA	R/W		DACs
			0*	in normal operational mode
			1	in Power-down mode
5	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
4	YGS	R/W		luminance gain for white – black
			0	100 IRE
			1	92.5 IRE including 7.5 IRE set-up of black
3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
2	SCBW	R/W		bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figure 6 and Figure 7)
			0	enlarged
			1*	standard
1	PAL	R/W		encoding
			0	NTSC (non-alternating V component)
			1	PAL (alternating V component)
0	FISE	R/W		total pixel clocks per line
			0	864
			1	858

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Table 56: Burst amplitude register, subaddress 62h, bit description

*Legend: * = default value after reset, ^ = recommended value.*

Bit	Symbol	Access	Value	Description
7	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
6 to 0	BSTA[6:0]	R/W		amplitude of color burst; input representation in accordance with *'ITU-R BT.601'*
			3Fh (63)^	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding; BSTA = 0 to 2.02 × nominal
			2Dh (45)^	white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding; BSTA = 0 to 2.82 × nominal
			43h (67)^	white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding; BSTA = 0 to 1.90 × nominal
			2Fh (47)*^	white-to-black = 100 IRE; burst = 43 IRE; PAL encoding; BSTA = 0 to 3.02 × nominal

Table 57: Subcarrier 0, 1, 2 and 3 registers, subaddresses 63h to 66h, bit description

Subaddress	Bit	Symbol	Access	Value	Description
66h	7 to 0	FSC[31:24]	R/W	-	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency); FSC[31:24] = most significant byte; FSC[07:00] = least significant byte [1]
65h	7 to 0	FSC[23:16]	R/W	-	
64h	7 to 0	FSC[15:08]	R/W	-	
63h	7 to 0	FSC[07:00]	R/W	-	

[1] $$FSC = \text{round}\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$$

Examples:

a) NTSC M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F0 7C1Fh).

b) PAL B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A09 8ACBh).

Table 58: Line 21 odd 0, 1 and even 0, 1 registers, subaddresses 67h to 6Ah, bit description [1]

Subaddress	Bit	Symbol	Access	Value	Description
67h	7 to 0	L21O[07:00]	R/W	-	first byte of captioning data, odd field
68h	7 to 0	L21O[17:10]	R/W	-	second byte of captioning data, odd field
69h	7 to 0	L21E[07:00]	R/W	-	first byte of extended data, even field
6Ah	7 to 0	L21E[17:10]	R/W	-	second byte of extended data, even field

[1] LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.

Table 59: Trigger control registers, subaddresses 6Ch and 6Dh, bit description

*Legend: * = default value after reset.*

Subaddress	Bit	Symbol	Access	Value	Description
6Ch	7 to 0	HTRIG[7:0]	R/W	00h*	sets the horizontal trigger phase related to chip-internal horizontal input [1]
6Dh	7 to 5	HTRIG[10:8]	R/W	0h*	
	4 to 0	VTRIG[4:0]	R/W	00h*	sets the vertical trigger phase related to chip-internal vertical input [2]

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[1] Values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed; increasing HTRIG decreases delays of all internally generated timing signals.

[2] Increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines; variation range of VTRIG = 0 to 31 (1Fh).

Table 60: Multi control register, subaddress 6Eh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
6	BLCKON	R/W	0*	encoder in normal operation mode
			1	output signal is forced to blanking level
5 and 4	PHRES[1:0]	R/W		selects the phase reset mode of the color subcarrier generator
			00	no subcarrier reset
			01	subcarrier reset every two lines
			10	subcarrier reset every eight fields
			11	subcarrier reset every four fields
3 and 2	LDEL[1:0]	R/W		selects the delay on luminance path with reference to chrominance path
			00*	no luminance delay
			01	1 LLC luminance delay
			10	2 LLC luminance delay
			11	3 LLC luminance delay
1 and 0	FLC[1:0]	R/W		field length control
			00*	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz
			01	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
			10	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
			11	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 61: Closed caption, teletext enable register, subaddress 6Fh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 and 6	CCEN[1:0]	R/W		enables individual line 21 encoding
			00*	line 21 encoding off
			01	enables encoding in field 1 (odd)
			10	enables encoding in field 2 (even)
			11	enables encoding in both fields

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Table 61: Closed caption, teletext enable register, subaddress 6Fh, bit description
...continued

Bit	Symbol	Access	Value	Description
5	TTXEN	R/W		teletext insertion
			0*	disabled
			1	enabled
4 to 0	SCCLN[4:0]	R/W	-	selects the actual line, where closed caption or extended data are encoded; line = (SCCLN + 4) for M-systems; line = (SCCLN + 1) for other systems

Table 62: Active Display Window Horizontal (ADWH) start and end registers, subaddresses 70h to 72h, bit description

Subaddress	Bit	Symbol	Access	Value	Description
70h	7 to 0	ADWHS[7:0]	R/W	-	active display window horizontal start; defines the start of the active TV display portion after the border color [1]
71h	7 to 0	ADWHE[7:0]	R/W	-	active display window horizontal end; defines the end of the active TV display portion before the border color [1]
72h	7	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	6 to 4	ADWHE[10:8]	R/W	-	active display window horizontal end; defines the end of the active TV display portion before the border color [1]
	3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	2 to 0	ADWHS[10:8]	R/W	-	active display window horizontal start; defines the start of the active TV display portion after the border color [1]

[1] Values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed.

Table 63: TTX request horizontal start register, subaddress 73h, bit description
*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXHS[7:0]	R/W		start of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0); see Figure 15
			42h*	if strapped to PAL
			54h*	if strapped to NTSC

Table 64: TTX request horizontal delay register, subaddress 74h, bit description
*Legend: * = default value after reset and minimum value.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	0h	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	TTXHD[3:0]	R/W	2h*	indicates the delay in clock cycles between rising edge of TTXRQ output signal on pin TTXRQ_XCLKO2 (CLK2EN = 0) and valid data at pin TTX_SRES

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Table 65: CSYNC advance register, subaddress 75h, bit description

Bit	Symbol	Access	Value	Description
7 to 3	CSYNCA[4:0]	R/W	-	advanced composite sync against RGB output from 0 XTAL clocks to 31 XTAL clocks
2 to 0	-	R/W	000	must be programmed with logic 0 to ensure compatibility to future enhancements

Table 66: TTX odd request vertical start register, subaddress 76h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXOVS[7:0]	R/W		with TTXOVS8 (see Table 72) first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in odd field, line = (TTXOVS + 4) for M-systems and line = (TTXOVS + 1) for other systems
			05h*	if strapped to PAL
			06h*	if strapped to NTSC

Table 67: TTX odd request vertical end register, subaddress 77h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXOVE[7:0]	R/W		with TTXOVE8 (see Table 72) last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in odd field, line = (TTXOVE + 3) for M-systems and line = TTXOVE for other systems
			16h*	if strapped to PAL
			10h*	if strapped to NTSC

Table 68: TTX even request vertical start register, subaddress 78h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXEVS[7:0]	R/W		with TTXEVS8 (see Table 72) first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in even field, line = (TTXEVS + 4) for M-systems and line = (TTXEVS + 1) for other systems
			04h*	if strapped to PAL
			05h*	if strapped to NTSC

Table 69: TTX even request vertical end register, subaddress 79h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXEVE[7:0]	R/W		with TTXEVE8 (see Table 72) last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in even field, line = (TTXEVE + 3) for M-systems and line = TTXEVE for other systems
			16h*	if strapped to PAL
			10h*	if strapped to NTSC

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Table 70: First active line register, subaddress 7Ah, bit description

Bit	Symbol	Access	Value	Description
7 to 0	FAL[7:0]	R/W		with FAL8 (see Table 72) first active line = (FAL + 4) for M-systems and (FAL + 1) for other systems, measured in lines
			00h	coincides with the first field synchronization pulse

Table 71: Last active line register, subaddress 7Bh, bit description

Bit	Symbol	Access	Value	Description
7 to 0	LAL[7:0]	R/W		with LAL8 (see Table 72) last active line = (LAL + 3) for M-systems and LAL for other system, measured in lines
			00h	coincides with the first field synchronization pulse

Table 72: TTX mode, MSB vertical register, subaddress 7Ch, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	TTX60	R/W	0*	enables NABTS (FISE = 1) or European TTX (FISE = 0)
			1	enables world standard teletext 60 Hz (FISE = 1)
6	LAL8	R/W		see Table 71
5	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
4	FAL8	R/W		see Table 70
3	TTXEVE8	R/W		see Table 69
2	TTXOVE8	R/W		see Table 67
1	TTXEVS8	R/W		see Table 68
0	TTXOVS8	R/W		see Table 66

Table 73: Disable TTX line registers, subaddresses 7Eh and 7Fh, bit description [1]

Subaddress	Bit	Symbol	Access	Value	Description
7Eh	7 to 0	LINE[12:5]	R/W	-	individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits, disabled line = LINExx (50 Hz field rate)
7Fh	7 to 0	LINE[20:13]	R/W	-	

[1] This bit mask is effective only if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE.

Table 74: Pixel clock 0, 1 and 2 registers, subaddresses 81h to 83h, bit description

Subaddress	Bit	Symbol	Access	Value	Description
81h	7 to 0	PCL[07:00]	R/W		defines the frequency of the synthesized pixel clock PIXCLKO; $f_{PIXCLK} = \left(\frac{PCL}{2^{24}} \times f_{XTAL}\right) \times 8$; f_{XTAL} = 27 MHz nominal
82h	7 to 0	PCL[15:08]			
83h	7 to 0	PCL[23:16]			
				20 F63Bh	640 × 480 to NTSC M
				1B 5A73h	640 × 480 to PAL B/G (as by strapping pins)

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Table 75: Horizontal offset register, subaddress 90h, bit description

Bit	Symbol	Description
7 to 0	XOFS[7:0]	with XOFS[9:8] (see Table 79) horizontal offset; defines the number of PIXCLKs from horizontal sync (HSVGC) output to composite blanking ($\overline{CBO}$) output

Table 76: Pixel number register, subaddress 91h, bit description

Bit	Symbol	Description
7 to 0	XPIX[7:0]	with XPIX[9:8] (see Table 79) pixel in X direction; defines half the number of active pixels per input line (identical to the length of $\overline{CBO}$ pulses)

Table 77: Vertical offset odd register, subaddress 92h, bit description

Bit	Symbol	Description
7 to 0	YOFSO[7:0]	with YOFSO[9:8] (see Table 79) vertical offset in odd field; defines (in the odd field) the number of lines from VSVGC to first line with active $\overline{CBO}$; if no LUT data is requested, the first active $\overline{CBO}$ will be output at YOFSO + 2; usually, YOFSO = YOFSE with the exception of extreme vertical downscaling and interlacing

Table 78: Vertical offset even register, subaddress 93h, bit description

Bit	Symbol	Description
7 to 0	YOFSE[7:0]	with YOFSE[9:8] (see Table 79) vertical offset in even field; defines (in the even field) the number of lines from VSVGC to first line with active $\overline{CBO}$; if no LUT data is requested, the first active $\overline{CBO}$ will be output at YOFSE + 2; usually, YOFSE = YOFSO with the exception of extreme vertical downscaling and interlacing

Table 79: MSBs register, subaddress 94h, bit description

Bit	Symbol	Description
7 and 6	YOFSE[9:8]	see Table 78
5 and 4	YOFSO[9:8]	see Table 77
3 and 2	XPIX[9:8]	see Table 76
1 and 0	XOFS[9:8]	see Table 75

Table 80: Line number register, subaddress 95h, bit description

Bit	Symbol	Description
7 to 0	YPIX[7:0]	with YPIX[9:8] (see Table 81) defines the number of requested input lines from the feeding device; number of requested lines = YPIX + YOFSE – YOFSO

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Table 81: Scaler CTRL, MCB and YPIX register, subaddress 96h, bit description

Bit	Symbol	Access	Value	Description
7	EFS	R/W		in Slave mode frame sync signal at pin FSVGC
			0	ignored
			1	accepted
6	PCBN	R/W		polarity of $\overline{CBO}$ signal
			0	normal (HIGH during active video)
			1	inverted (LOW during active video)
5	SLAVE	R/W		from the SAA7102; SAA7103 the timing to the graphics controller is
			0	master
			1	slave
4	ILC	R/W		if hardware cursor insertion is active
			0	set LOW for non-interlaced input signals
			1	set HIGH for interlaced input signals
3	YFIL	R/W		luminance sharpness booster
			0	disabled
			1	enabled
2	HSL	R/W		trigger event for the horizontal state machine (device is slave to HSVGC input)
			0	not shifted
			1	shifted 128 PIXCLKs adapted to a late HSVGC
1 and 0	YPIX[9:8]			see Table 80

Table 82: Sync control register, subaddress 97h, bit description

Bit	Symbol	Access	Value	Description
7	HFS	R/W		horizontal sync is derived from
			0	input signal (Save mode) at pin HSVGC
			1	a frame sync signal (Slave mode) at pin FSVGC (only if EFS is set HIGH)
6	VFS	R/W		vertical sync (field sync) is derived from
			0	input signal (Slave mode) at pin VSVGC
			1	a frame sync signal (Slave mode) at pin FSVGC (only if EFS is set HIGH)
5	OFS	R/W		pin FSVGC is
			0	input
			1	active output
4	PFS	R/W		polarity of signal at pin FSVGC in output mode (Master mode) is
			0	active HIGH; rising edge of the input signal is used in Slave mode
			1	active LOW; falling edge of the input signal is used in Slave mode

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Table 82: Sync control register, subaddress 97h, bit description *...continued*

Bit	Symbol	Access	Value	Description
3	OVS	R/W		pin VSVGC is
			0	input
			1	active output
2	PVS	R/W		polarity of signal at pin VSVGC in output mode (Master mode) is
			0	active HIGH; rising edge of the input signal is used in Slave mode
			1	active LOW; falling edge of the input signal is used in Slave mode
1	OHS	R/W		pin HSVGC is
			0	input
			1	active output
0	PHS	R/W		polarity of signal at pin HSVGC in output mode (Master mode) is
			0	active HIGH; rising edge of the input signal is used in Slave mode
			1	active LOW; falling edge of the input signal is used in Slave mode

Table 83: Line length register, subaddress 98h, bit description

Bit	Symbol	Description
7 to 0	HLEN[7:0]	with HLEN[10:8] (see Table 84) horizontal length; $\mathrm{HLEN} = \frac{\text{number of PIXCLKs}}{\text{line}} - 1$

Table 84: Input delay, MSB line length register, subaddress 99h, bit description

Bit	Symbol	Description
7 to 4	IDEL[3:0]	input delay; defines the distance in PIXCLKs between the active edge of $\overline{\text{CBO}}$ and the first received valid pixel
3	-	must be programmed with logic 0 to ensure compatibility to future enhancements
2 to 0	HLEN[10:8]	see Table 83

Table 85: Horizontal increment register, subaddress 9Ah, bit description

Bit	Symbol	Description
7 to 0	XINC[7:0]	with XINC[11:8] (see Table 87) incremental fraction of the horizontal scaling engine; $\mathrm{XINC} = \frac{\frac{\text{number of output pixels}}{\text{line}}}{\frac{\text{number of input pixels}}{\text{line}}} \times 4096$

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Table 86: Vertical increment register, subaddress 9Bh, bit description

Bit	Symbol	Description
7 to 0	YINC[7:0]	with YINC[11:8] (see Table 87) incremental fraction of the vertical scaling engine; $\mathrm{YINC} = \frac{\text{number of active output lines}}{\text{number of active input lines}} \times 4096$

Table 87: MSBs vertical and horizontal increment register, subaddress 9Ch, bit description

Bit	Symbol	Description
7 to 4	YINC[11:8]	see Table 86
3 to 0	XINC[11:8]	see Table 85

Table 88: Weighting factor odd register, subaddress 9Dh, bit description

Bit	Symbol	Description
7 to 0	YIWGTO[7:0]	with YIWGTO[11:8] (see Table 90) weighting factor for the first line of the odd field; $\mathrm{YIWGTO} = \frac{\mathrm{YINC}}{2} + 2048$

Table 89: Weighting factor even, subaddress 9Eh, bit description

Bit	Symbol	Description
7 to 0	YIWGTE[7:0]	with YIWGTE[11:8] (see Table 90) weighting factor for the first line of the even field; $\mathrm{YIWGTE} = \frac{\mathrm{YINC} - \mathrm{YSKIP}}{2}$

Table 90: Weighting factor MSB register, subaddress 9Fh, bit description

Bit	Symbol	Description
7 to 4	YIWGTE[11:8]	see Table 89
3 to 0	YIWGTO[11:8]	see Table 88

Table 91: Vertical line skip register, subaddress A0h, bit description

Bit	Symbol	Access	Value	Description
7 to 0	YSKIP[7:0]	R/W		with YSKIP[11:8] (see Table 92) vertical line skip; defines the effectiveness of the anti-flicker filter
			000h	most effective
			FFFh	anti-flicker filter switched off

Table 92: Blank enable for NI-bypass, vertical line skip MSB register, subaddress A1h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	BLEN	R/W		for non-interlaced graphics in bypass mode
			0*	no internal blanking
			1	forced internal blanking
6 to 4	-	R/W	000	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	YSKIP[11:8]	R/W		see Table 91

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Table 93: Border color Y register, subaddress A2h, bit description

Bit	Symbol	Description
7 to 0	BCY[7:0]	luminance portion of border color in underscan area

Table 94: Border color U register, subaddress A3h, bit description

Bit	Symbol	Description
7 to 0	BCU[7:0]	color difference portion of border color in underscan area

Table 95: Border color V register, subaddress A4h, bit description

Bit	Symbol	Description
7 to 0	BCV[7:0]	color difference portion of border color in underscan area

Table 96: Cursor color 1 R, G and B registers, subaddresses F0h to F2h, bit description

Subaddress	Bit	Symbol	Description
F0h	7 to 0	CC1R[7:0]	RED portion of first cursor color
F1h	7 to 0	CC1G[7:0]	GREEN portion of first cursor color
F2h	7 to 0	CC1B[7:0]	BLUE portion of first cursor color

Table 97: Cursor color 2 R, G and B registers, subaddresses F3h to F5h, bit description

Subaddress	Bit	Symbol	Description
F3h	7 to 0	CC2R[7:0]	RED portion of second cursor color
F4h	7 to 0	CC2G[7:0]	GREEN portion of second cursor color
F5h	7 to 0	CC2B[7:0]	BLUE portion of second cursor color

Table 98: Auxiliary cursor color R, G and B registers, subaddresses F6h to F8h, bit description

Subaddress	Bit	Symbol	Description
F6h	7 to 0	AUXR[7:0]	RED portion of auxiliary cursor color
F7h	7 to 0	AUXG[7:0]	GREEN portion of auxiliary cursor color
F8h	7 to 0	AUXB[7:0]	BLUE portion of auxiliary cursor color

Table 99: Horizontal cursor position and horizontal hot spot, MSB XCP registers, subaddresses F9h and FAh, bit description

Subaddress	Bit	Symbol	Description
FAh	7 to 3	XHS[4:0]	horizontal hot spot of cursor
	2 to 0	XCP[10:8]	horizontal cursor position
F9h	7 to 0	XCP[7:0]	

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Table 100: Vertical cursor position and vertical hot spot, MSB YCP registers, subaddresses FBh and FCh, bit description

Subaddress	Bit	Symbol	Description
FCh	7 to 3	YHS[4:0]	vertical hot spot of cursor
	2	-	must be programmed with logic 0 to ensure compatibility to future enhancements
	1 and 0	YCP[9:8]	vertical cursor position
FBh	7 to 0	YCP[7:0]	

Table 101: Input path control register, subaddress FDh, bit description

Bit	Symbol	Access	Value	Description
7	LUTOFF	R/W		color look-up table
			0	active
			1	bypassed
6	CMODE	R/W		cursor mode
			0	cursor mode; input color will be inverted
			1	auxiliary cursor color will be inserted
5	LUTL	R/W		LUT loading via input data stream
			0	inactive
			1	color and cursor LUTs are loaded
4 to 2	IF[2:0]	R/W		input format
			000	8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB or C_B-Y-C_R
			001	5 + 5 + 5-bit 4 : 4 : 4 non-interlaced RGB
			010	5 + 6 + 5-bit 4 : 4 : 4 non-interlaced RGB
			011	8 + 8 + 8-bit 4 : 2 : 2 non-interlaced C_B-Y-C_R
			100	8 + 8 + 8-bit 4 : 2 : 2 interlaced C_B-Y-C_R (ITU-R BT.656, 27 MHz clock) (in subaddresses 91h and 94h set XPIX = number of active pixels/line)
			101	8-bit non-interlaced index color
			110	8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB or C_B-Y-C_R (special bit ordering)
1	MATOFF	R/W		RGB to C_R-Y-C_B matrix
			0	active
			1	bypassed
0	DFOFF	R/W		down formatter
			0	(4 : 4 : 4 to 4 : 2 : 2) in input path is active
			1	bypassed

Table 102: Cursor bit map register, subaddress FEh, bit description

Data byte	Description
CURSA	RAM start address for cursor bit map; the byte following subaddress FEh points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition

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Table 103: Color look-up table register, subaddress FFh, bit description

Data byte	Description
COLSA	RAM start address for color LUT; the byte following subaddress FFh points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition

In subaddresses 5Bh, 5Ch, 5Dh, 5Eh and 62h all IRE values are rounded up.

8.4 Slave transmitter

Table 104: Status byte register, subaddress 00h, bit description

Bit	Symbol	Access	Value	Description
7 to 5	VER[2:0]	R	101	version identification of the device: it will be changed with all versions of the IC that have different programming models; current version is 010 binary
4	CCRDO	R	1	set immediately after the closed caption bytes of the odd field have been encoded
			0	reset after information has been written to the subaddresses 67h and 68h
3	CCRDE	R	1	set immediately after the closed caption bytes of the even field have been encoded
			0	reset after information has been written to the subaddresses 69h and 6Ah
2	-	R	0	-
1	FSEQ	R	1	during first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields)
			0	not first field of a sequence
0	O_E	R	1	during even field
			0	during odd field

Table 105: Slave transmitter (slave address 89h)

Register function	Subaddress	Data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	00h	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E
Chip ID	1Ch	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
FIFO status	80h	0	0	0	0	0	0	OVFL	UDFL

Table 106: Chip ID register, subaddress 1Ch, bit description

Bit	Symbol	Access	Value	Description
7 to 0	CID[7:0]	R		chip ID
			02h	SAA7102
			03h	SAA7103

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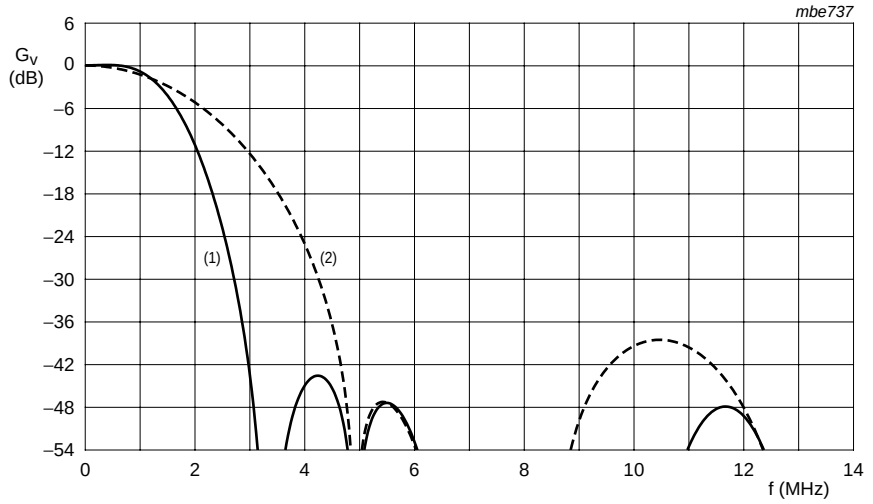
Table 107: FIFO status register, subaddress 80h, bit description

Bit	Symbol	Access	Value	Description
7 to 2	-	R	0h	-
1	OVFL	R	0	no FIFO overflow
			1	FIFO overflow has occurred; this bit is reset after this subaddress has been read
0	UDFL	R	0	no FIFO underflow
			1	FIFO underflow has occurred; this bit is reset after this subaddress has been read



(1) SCBW = 1.

(2) SCBW = 0.

Fig 6. Chrominance transfer characteristic 1

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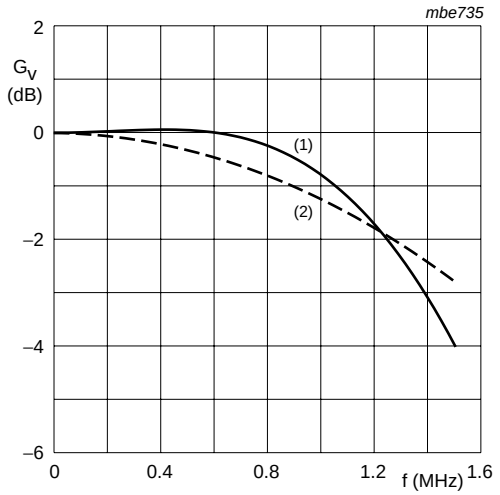
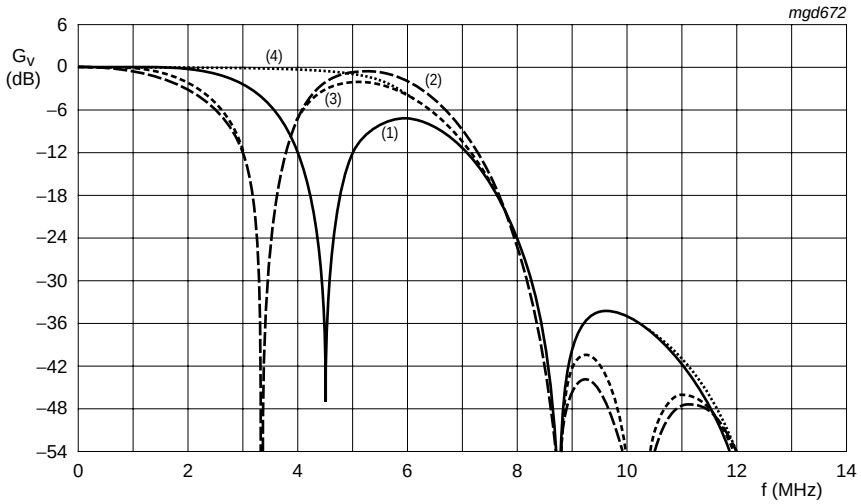


(1) SCBW = 1.

(2) SCBW = 0.

Fig 7. Chrominance transfer characteristic 2



(1) CCRS[1:0] = 01.

(2) CCRS[1:0] = 10.

(3) CCRS[1:0] = 11.

(4) CCRS[1:0] = 00.

Fig 8. Luminance transfer characteristic 1 (excluding scaler)

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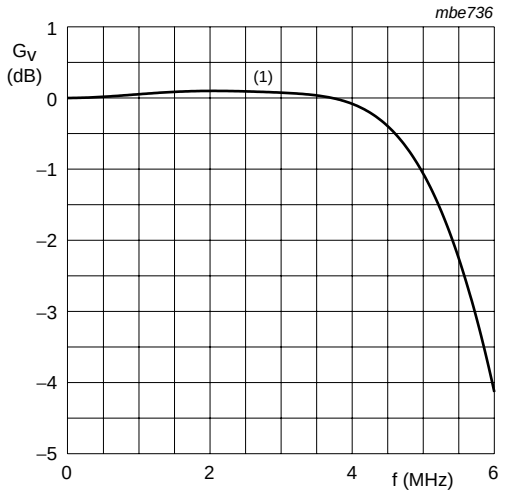

(1) CCRS[1:0] = 00

Fig 9. Luminance transfer characteristic 2 (excluding scaler)

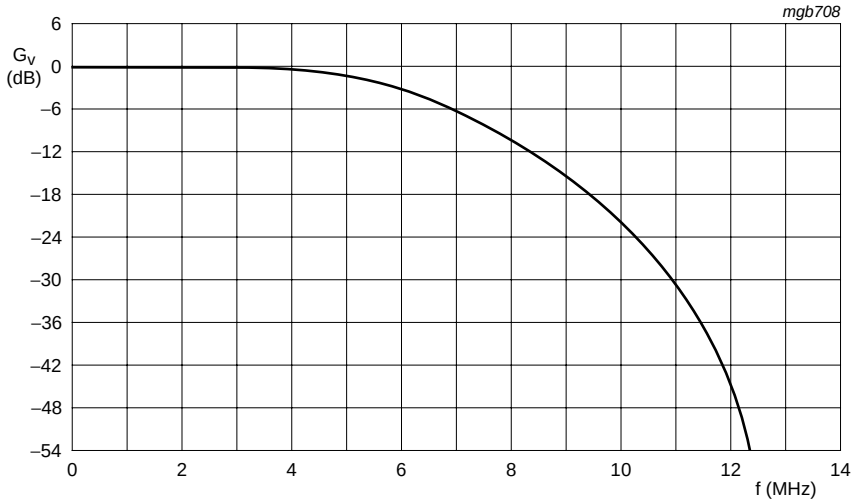

Fig 10. Luminance transfer characteristic in RGB (excluding scaler)

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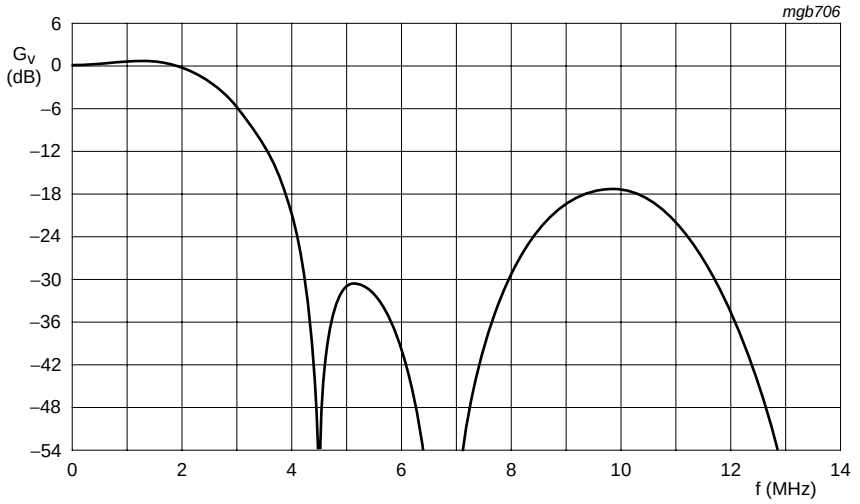

Fig 11. Color difference transfer characteristic in RGB (excluding scaler)

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9. Limiting values

Table 108: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All ground pins connected together and grounded (0 V); all supply pins connected together.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDD}	digital supply voltage			–0.5	+4.6	V
V_{DDA}	analog supply voltage			–0.5	+4.6	V
$V_{i(A)}$	input voltage at analog inputs			–0.5	+4.6	V
$V_{i(n)}$	input voltage at pins XTALI, SDA and SCL			–0.5	V_{DDD} + 0.5	V
$V_{i(D)}$	input voltage at digital inputs or I/O pins	outputs in 3-state		–0.5	+4.6	V
		outputs in 3-state	[1]	–0.5	+5.5	V
ΔV_{SS}	voltage difference between $V_{SSA(n)}$ and $V_{SSD(n)}$			-	100	mV
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			0	70	°C
V_{esd}	electrostatic discharge voltage	human body model	[2]	-	±2000	V
		machine model	[3]	-	±150	V

[1] Condition for maximum voltage at digital inputs or I/O pins: 3.0 V < V_{DDD} < 3.6 V.

[2] Class 2 according to JESD22-A114-B.

[3] Class A according to EIA/JESD22-A115-A.

10. Thermal characteristics

Table 109: Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient				
	SAA7102E	in free air	[1]	38	K/W
	SAA7103E	in free air	[1]	38	K/W
	SAA7102H	in free air	[1]	53	K/W
	SAA7103H	in free air	[1]	53	K/W

[1] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample copper area directly under the SAA7102; SAA7103 with a number of through-hole plating, connected to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

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11. Characteristics

Table 110: Characteristics

V_{DDD} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C (typical values excluded); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DDA}	analog supply voltage			3.15	3.3	3.45	V
V_{DDD}	digital supply voltage			3.0	3.3	3.6	V
I_{DDA}	analog supply current		[1]	1	110	140	mA
I_{DDD}	digital supply current		[2]	1	70	90	mA
Inputs							
V_{IL}	LOW-level input voltage at all digital input pins except pins SDA and SCL			–0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage at all digital input pins except pins SDA and SCL			2.0	-	V_{DDD} + 0.3	V
I_{LI}	input leakage current			-	-	10	µA
C_i	input capacitance	clocks		-	-	10	pF
		data		-	-	8	pF
		I/Os at high-impedance		-	-	8	pF
Outputs; all digital output pins except pin SDA							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA		2.4	-	-	V
I^2C-bus; pins SDA and SCL							
V_{IL}	LOW-level input voltage			–0.5	-	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DDD}$	-	V_{DDD} + 0.3	V
I_i	input current	V_i = LOW or HIGH		–10	-	+10	µA
V_{OL}	LOW-level output voltage (pin SDA)	I_{OL} = 3 mA		-	-	0.4	V
I_o	output current	during acknowledge		3	-	-	mA
Clock timing; pins PIXCLKI and PIXCLKO							
T_{PIXCLK}	cycle time		[3]	22.5	-	100	ns
$t_{d(CLKD)}$	delay from PIXCLKO to PIXCLKI		[4]	-	-	-	ns
δ	duty factor	t_{HIGH}/T_{PIXCLK}	[3]	40	50	60	%
		t_{HIGH}/T_{CLKO2}; output		40	50	60	%
t_r	rise time		[3]	-	-	3	ns
t_f	fall time		[3]	-	-	3	ns
Input timing							
$t_{SU;DAT}$	input data set-up time			5	-	-	ns
$t_{HD;DAT}$	input data hold time			0	-	-	ns
Crystal oscillator							
f_{nom}	nominal frequency			-	27	-	MHz
$\Delta f/f_{nom}$	permissible deviation of nominal frequency		[5]	-50×10^{-6}	-	$+50 \times 10^{-6}$	

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Table 110: Characteristics *...continued*

V_{DDD} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C (typical values excluded); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Crystal specification						
T_{amb}	ambient temperature		0	-	70	°C
C_L	load capacitance		8	-	-	pF
R_S	series resistance		-	-	80	Ω
C_1	motional capacitance (typical)		1.2	1.5	1.8	fF
C_0	parallel capacitance (typical)		2.8	3.5	4.2	pF
Data and reference signal output timing						
$C_{o(L)}$	output load capacitance		8	-	40	pF
$t_{o(h)}$	output hold time		2	-	-	ns
$t_{o(d)}$	output delay time		-	-	16	ns
CVBS and RGB outputs						
$V_{o(CVBS)(p-p)}$	output voltage CVBS (peak-to-peak value)	see Table 111	-	1.23	-	V
$V_{o(VBS)(p-p)}$	output voltage VBS (S-video) (peak-to-peak value)	see Table 111	-	1.0	-	V
$V_{o(C)(p-p)}$	output voltage C (S-video) (peak-to-peak value)	see Table 111	-	0.89	-	V
$V_{o(RGB)(p-p)}$	output voltage R, G, B (peak-to-peak value)	see Table 111	-	0.7	-	V
ΔV_o	inequality of output signal voltages		-	2	-	%
R_L	load resistance		-	37.5	-	Ω
B_{DAC}	output signal bandwidth of DACs	–3 dB	15	-	-	MHz
$ILE_{lf(DAC)}$	low frequency integral linearity error of DACs		-	-	±3	LSB
$DLE_{lf(DAC)}$	low frequency differential linearity error of DACs		-	-	±1	LSB

[1] Minimum value for I^2C-bus bit DOWNA = 1.

[2] Minimum value for I^2C-bus bit DOWND = 1.

[3] The data is for both input and output direction.

[4] This parameter is arbitrary, if PIXCLKI is looped through the VGC.

[5] If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.

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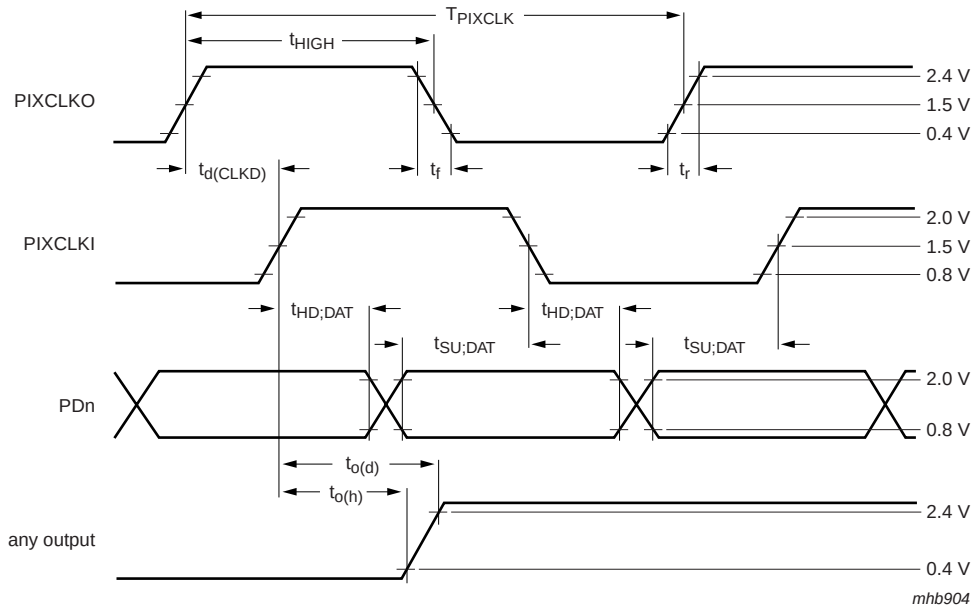

Fig 12. Input/output timing specification

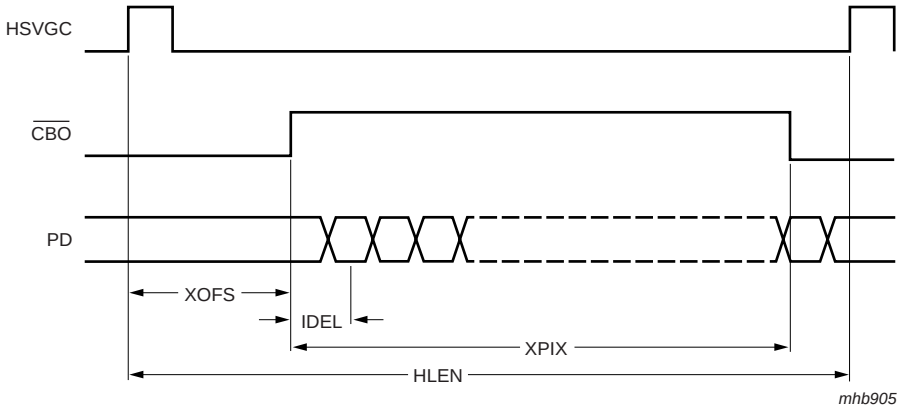

Fig 13. Horizontal input timing

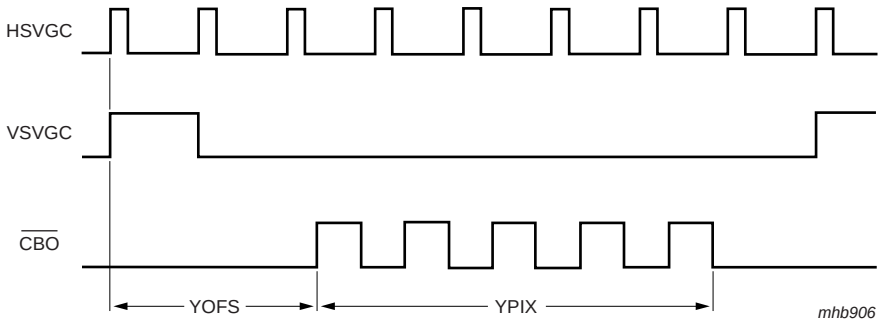

Fig 14. Vertical input timing

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11.1 Teletext timing

Time t_{FD} is the time needed to interpolate input data TTX and insert it into the CVBS and VBS output signal, such that it appears at t_{TTX} = 9.78 µs (PAL) or t_{TTX} = 10.5 µs (NTSC) after the leading edge of the horizontal synchronization pulse.

Time t_{PD} is the pipeline delay time introduced by the source that is gated by TTXRQ_XCLKO2 in order to deliver TTX data. This delay is programmable by register TTXHD. For every active HIGH state at output pin TTXRQ_XCLKO2, a new teletext bit must be provided by the source.

Since the beginning of the pulses representing the TTXRQ signal and the delay between the rising edge of TTXRQ and valid teletext input data are fully programmable (TTXHS and TTXHD), the TTX data is always inserted at the correct position after the leading edge of the outgoing horizontal synchronization pulse.

Time $t_{i(TTXW)}$ is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits at a text data rate of 6.9375 Mbit/s (PAL), 296 teletext bits at a text data rate of 5.7272 Mbit/s (world standard TTX) or 288 teletext bits at a text data rate of 5.7272 Mbit/s (NABTS). The insertion window is not opened if the control bit TTXEN is zero.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

It is essential to note that the two pins used for teletext insertion must be configured for this purpose by the correct I²C-bus register settings.

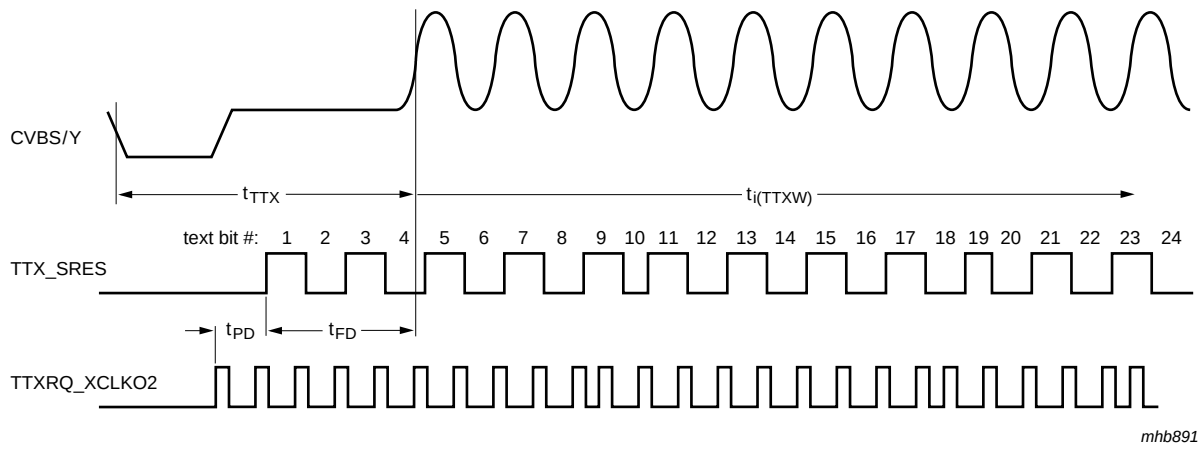

Fig 15. Teletext timing

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12. Application information

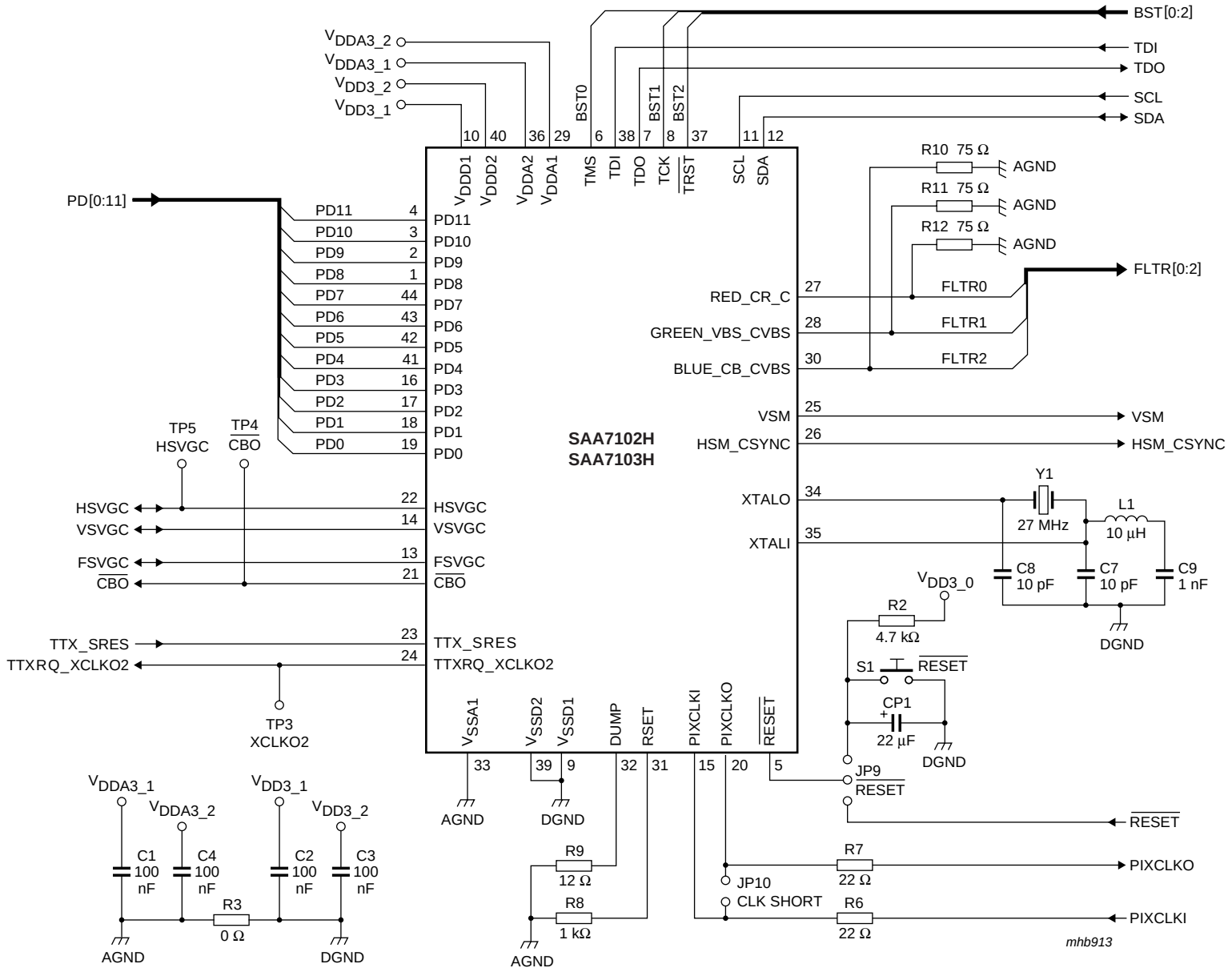

Fig 16. Application circuit

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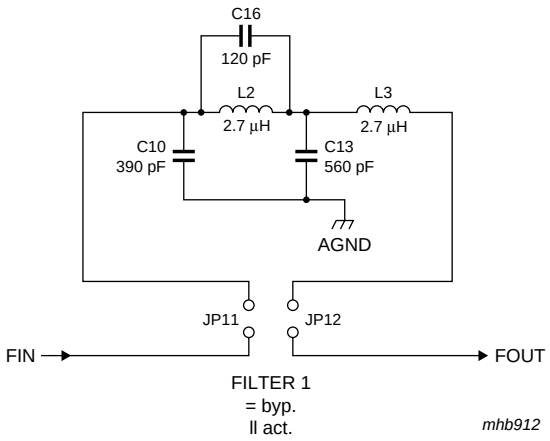

Fig 17. FLTR0, FLTR1 and FLTR2 of Figure 16

12.1 Analog output voltages

The analog output voltages are dependent on the total load (typical value 37.5 Ω), the digital gain parameters and the I²C-bus settings of the DAC reference currents (analog settings).

The digital output signals in front of the DACs under nominal (nominal here stands for the settings given in Table 52 to Table 56 for example a standard PAL or NTSC signal) conditions occupy different conversion ranges, as indicated in Table 111 for a $^{100}/_{100}$ color bar signal.

By setting the reference currents of the DACs as shown in Table 111, standard compliant amplitudes can be achieved for all signal combinations; it is assumed that in subaddress 16h, parameter DACF = 0000b, that means the fine adjustment for all DACs in common is set to 0 %.

If S-video output is desired, the adjustment for the C (chrominance subcarrier) output should be identical to the one for VBS (luminance plus sync) output.

Table 111: Digital output signals conversion range

Set/out	CVBS, sync tip-to-white	VBS, sync tip-to-white	RGB, black-to-white
Digital settings	see Table 52 to Table 56	see Table 52 to Table 56	see Table 46 and Table 47
Digital output	1014	881	876
Analog settings	e.g. B DAC = 1Fh	e.g. G DAC = 1Bh	e.g. R DAC = G DAC = B DAC = 0Bh
Analog output	1.23 V (p-p)	1.00 V (p-p)	0.70 V (p-p)

12.2 Suggestions for a board layout

Use separate ground planes for analog and digital ground. Connect these planes only at one point directly under the device, by using a 0 Ω resistor directly at the supply stage. Use separate supply lines for the analog and digital supply. Place the supply decoupling capacitors close to the supply pins.

Use L_{bead} (ferrite coil) in each digital supply line close to the decoupling capacitors to minimize radiation energy (EMC).

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Place the analog coupling (clamp) capacitors close to the analog input pins. Place the analog termination resistors close to the coupling capacitors.

Be careful of hidden layout capacitors around the crystal application.

Use serial resistors in clock, sync and data lines, to avoid clock or data reflection effects and to soften data energy.

13. Test information

13.1 Boundary scan test

The SAA7102; SAA7103 has built-in logic and 5 dedicated pins to support boundary scan testing which allows board testing without special hardware (nails). The SAA7102; SAA7103 follows the *"IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture"* set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset ($\overline{TRST}$), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported; see Table 112. Details about the JTAG BST-TEST can be found in the specification *"IEEE Std. 1149.1"*. A file containing the detailed Boundary Scan Description Language (BSDL) of the SAA7102; SAA7103 is available on request.

Table 112: BST instructions supported by the SAA7102; SAA7103

Instruction	Description
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.

13.1.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the $\overline{TRST}$ pin LOW.

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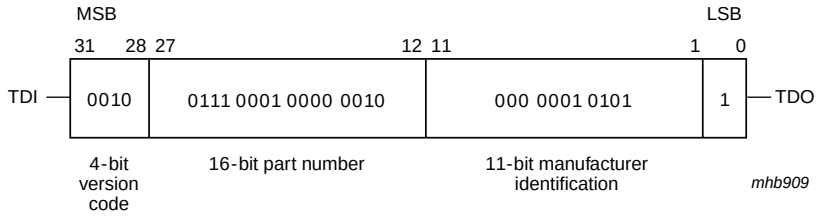
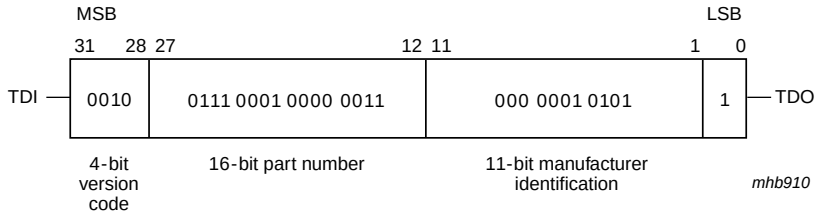
13.1.2 Device identification codes

A device identification register is specified in *"IEEE Std. 1149.1b-1994"*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and to determine the version number of the ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between pins TDI and TDO of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller, this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO); see Figure 18.



a. SAA7102.



b. SAA7103.

Fig 18. 32 bits of identification code

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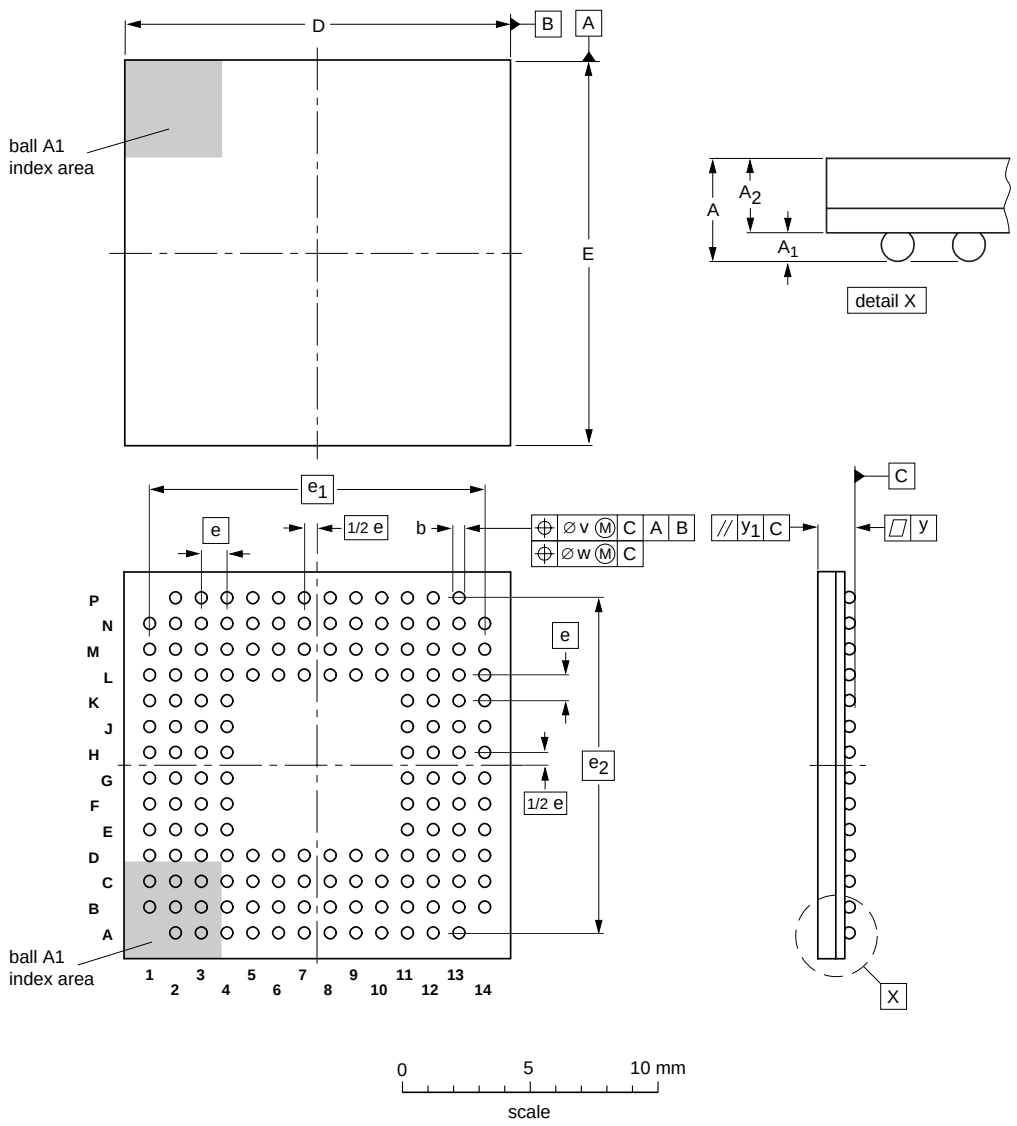
14. Package outline

LBGA156: plastic low profile ball grid array package; 156 balls; body 15 x 15 x 1.05 mm **SOT700-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.65	0.45 0.35	1.20 0.95	0.55 0.45	15.2 14.8	15.2 14.8	1	13	13	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT700-1	- - -	MO-192	- - -			~~01-05-11~~ 01-11-06

Fig 19. Package outline SOT700-1 (LBGA156)

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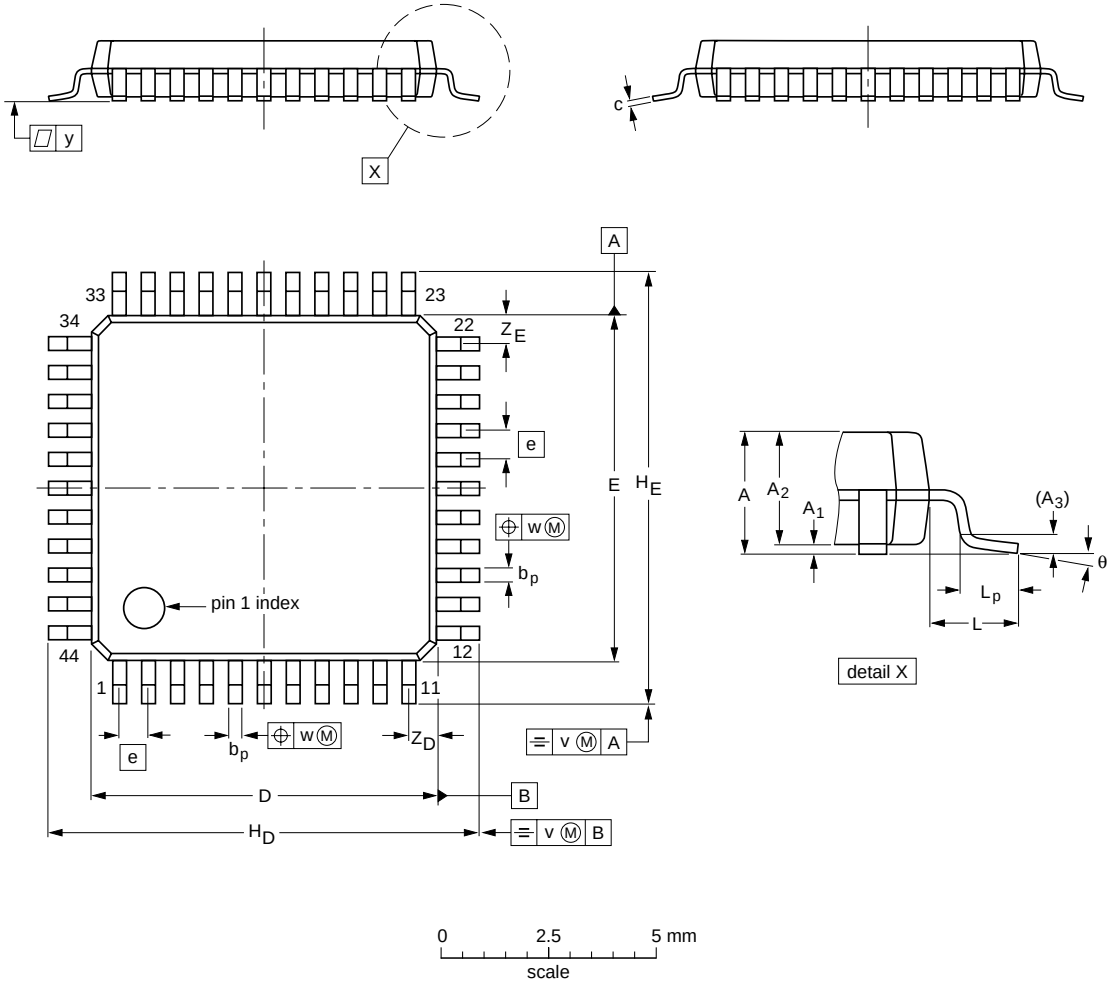
QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	2.1	0.25 0.05	1.85 1.65	0.25	0.4 0.2	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT307-2						~~97-08-01~~ 03-02-25

Fig 20. Package outline SOT307-2 (QFP44)

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15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

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- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 113: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

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[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Revision history

Table 114: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
SAA7102_SAA7103_4	20060118	Product data sheet	CPCN200505019	-	SAA7102_SAA7103_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Table 4: pin SCL corrected from I to I(/O) and updated description • Table 4: updated description for pin SDA • Package outline changed from SOT472-1 to SOT700-1				
SAA7102_SAA7103_3	20040301	Product specification	-	9397 750 11445	SAA7102_03_2
SAA7102_03_2	20020218	Product specification	-	9397 750 09214	SAA7102_03_1
SAA7102_03_1	20010925	Product specification	-	9397 750 08371	-

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17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

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