# DATA SHEET

# TEA1111A
## Speech circuit with dialler interface, regulated supply and earpiece volume control

Product specification
Supersedes data of 1999 Nov 22
File under Integrated Circuits, IC03

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Philips Semiconductors

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# Speech circuit with dialler interface, regulated supply and earpiece volume control

# TEA1111A

## FEATURES

- Low DC line voltage; operates down to 1.5 V (excluding voltage drop across external polarity guard)
- Line voltage regulator with adjustable DC voltage
- 3.25 V regulated strong supply point for peripheral circuits compatible with:
  - Speech mode
  - Ringer mode
  - Trickle mode.
- Transmit stage with:
  - Microphone amplifier with symmetrical high impedance inputs
  - DTMF amplifier with confidence tone on earpiece.
- Receive stage with:
  - Earpiece amplifier with adjustable gain and volume control.
- $\overline{\text{MUTE}}$ input for pulse or DTMF dialling
- AGC line loss compensation for microphone and earpiece
- LED control output.

## APPLICATIONS

- Line powered telephone sets with LCD module
- Cordless telephones
- Fax machines
- Answering machines.

## GENERAL DESCRIPTION

The TEA1111A is a bipolar integrated circuit that performs all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between speech and dialling. The IC operates at a line voltage down to 1.5 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

When the line current is high enough, a fixed amount of current is derived from the LN pin in order to create a strong supply point at pin $V_{DD}$. The voltage at pin $V_{DD}$ is regulated to 3.25 V to supply peripherals such as dialler, LCD module and microcontroller.

## QUICK REFERENCE DATA

$I_{line}$ = 15 mA; $V_{EE}$ = 0 V; $V_{VCI}$ = 0 V; $R_{SLPE}$ = 20 Ω; AGC pin connected to $V_{EE}$; $Z_{line}$ = 600 Ω; f = 1 kHz; measured according to test circuits given in Figs 15, 16 and 17; $T_{amb}$ = 25 °C; $T_j$ = 25 °C for TEA1111AUH; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{line}$ | line current operating range | normal operation | 11 | – | 140 | mA |
| | | with reduced performance | 1 | – | 11 | mA |
| $V_{LN}$ | DC line voltage | | 3.7 | 4.0 | 4.3 | V |
| $I_{CC}$ | internal current consumption | $V_{CC}$ = 3.3 V | – | 1.15 | 1.4 | mA |
| $V_{CC}$ | supply voltage for internal circuitry (unregulated) | $I_P$ = 0 mA | – | 3.3 | – | V |
| $V_{DD}$ | regulated supply voltage for peripherals | | | | | |
| | speech mode | $I_{DD}$ = –3 mA | 2.95 | 3.25 | 3.55 | V |
| | ringer mode | $I_{DD}$ = 75 mA | 3.0 | 3.3 | 3.6 | V |
| $I_{DD}$ | available supply current for peripherals | | – | – | –3 | mA |
| $G_{v(TX)}$ | typical voltage gain for microphone amplifier | $V_{MIC}$ = 4 mV (RMS) | 43.2 | 44.2 | 45.2 | dB |
| $G_{v(QR)}$ | typical voltage gain for earpiece amplifier | $V_{IR}$ = 4 mV (RMS) | 26.4 | 27.4 | 28.4 | dB |
| $\Delta G_{v(QR)}$ | volume control range for earpiece amplifier | | 0 | 14.5 | – | dB |
| $\Delta G_{v(trx)}$ | gain control range for microphone and earpiece amplifiers with respect to $I_{line}$ = 15 mA | $I_{line}$ = 85 mA | – | 6.0 | – | dB |
| $\Delta G_{v(trx)(m)}$ | gain reduction for microphone and earpiece amplifiers | $\overline{\text{MUTE}}$ = LOW | – | 80 | – | dB |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TEA1111AT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| TEA1111AUH | – | bare die; on foil | – |

## BLOCK DIAGRAM

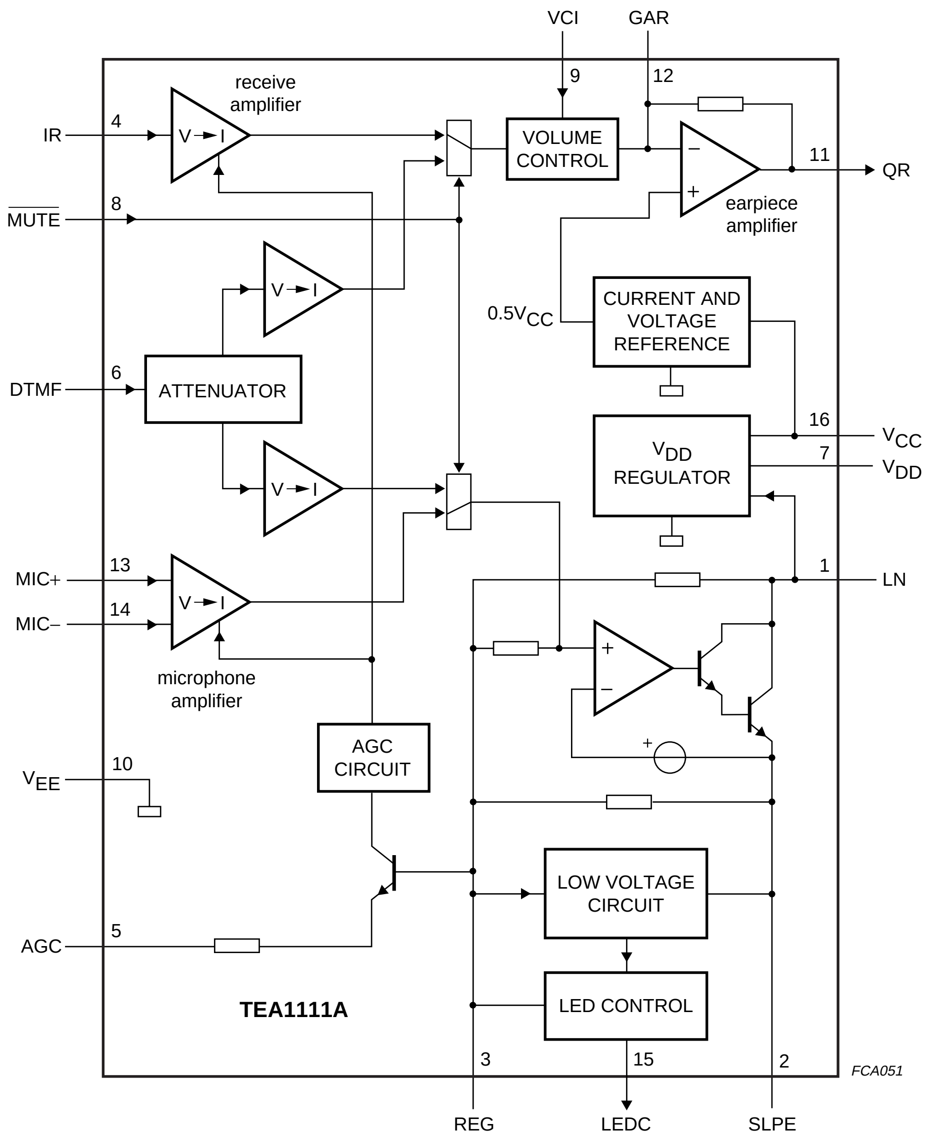



Fig.1 Block diagram.

**PINNING**

| SYMBOL | PIN | PAD | DESCRIPTION |
|---|---|---|---|
| | TEA1111TV | TEA1111AUH | |
| LN | 1 | 1 | positive line terminal |
| SLPE | 2 | 2 | slope (DC resistance) adjustment |
| REG | 3 | 3 | line voltage regulator decoupling |
| IR | 4 | 4 | receive amplifier input |
| AGC | 5 | 5 | automatic gain control/ line loss compensation |
| DTMF | 6 | 6 | dual-tone multi-frequency input |
| $V_{DD}$ | 7 | 7 | regulated supply for peripherals |
| $\overline{MUTE}$ | 8 | 8 | mute input to select speech or dialling mode (active LOW) |
| n.c. | – | 9 | not connected |
| VCI | 9 | 10 | volume control input |
| $V_{EE}$ | 10 | 11, 12 | negative line terminal |
| QR | 11 | 13 | earpiece amplifier output |
| GAR | 12 | 14 | earpiece amplifier gain adjustment |
| MIC+ | 13 | 15 | non-inverting microphone amplifier input |
| MIC– | 14 | 16 | inverting microphone amplifier input |
| LEDC | 15 | 17 | LED control output |
| $V_{CC}$ | 16 | 18 | supply voltage for internal circuit |

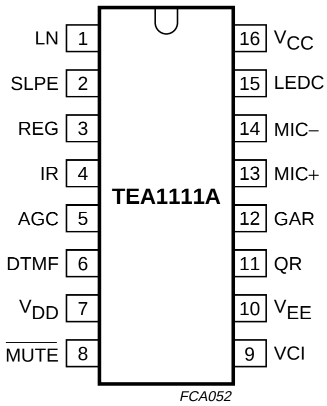



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

All data given in this chapter concerns typical values, except when otherwise specified.

### Supply (pins LN, SLPE, REG, $V_{CC}$ and $V_{DD}$)

The supply for the TEA1111A and its peripherals is obtained from the telephone line (see Fig.3).

#### THE LINE INTERFACE (PINS LN, SLPE AND REG)

The IC generates a stabilized reference voltage ($V_{ref}$) across pins LN and SLPE. $V_{ref}$ is temperature compensated and can be adjusted by using an external resistor ($R_{VA}$). $V_{ref}$ equals 3.8 V and can be increased by connecting $R_{VA}$ between pins REG and SLPE or decreased by connecting $R_{VA}$ between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate $V_{ref}$ and is decoupled by $C_{REG}$, which is connected to $V_{EE}$. This capacitor, converted to an equivalent inductance, (see Section “Set impedance”) determines the set impedance conversion from its DC value ($R_{SLPE}$) to its AC value ($R_{CC}$ in the audio-frequency range). The voltage at pin SLPE is proportional to the line current.

The voltage at pin LN is:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_{P} - I_{SUP} - I_{LEDC}$$

where:

- $I_{line}$ = line current
- $I_{CC}$ = current consumption of the IC
- $I_{P}$ = supply current for external circuits
- $I_{SUP}$ = current consumed between LN and $V_{EE}$ by the $V_{DD}$ regulator
- $I_{LEDC}$ = supply current for external LED circuitry.

The preferred value for $R_{SLPE}$ is 20 Ω. Changing $R_{SLPE}$ will affect more than the DC characteristics; it also influences the microphone and DTMF gains, the gain control characteristics, the sidetone level and the maximum output swing on the line.

The DC line current flowing into the set is determined by the exchange supply voltage ($V_{EXCH}$), the feeding bridge resistance ($R_{EXCH}$), the DC resistance of the telephone line ($R_{line}$) and the reference voltage ($V_{ref}$). With line currents below $I_{low}$ (9 mA), the internal reference voltage (generating $V_{ref}$) is automatically adjusted to a lower value.

This means that several sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.5 V. At line currents below $I_{low}$, the circuit has limited sending and receiving levels. This is called the low voltage area.

#### THE INTERNAL SUPPLY POINT (PIN $V_{CC}$)

The internal circuitry of the TEA1111A is supplied from pin $V_{CC}$. This voltage supply is derived from the line voltage by means of a resistor ($R_{CC}$) and must be decoupled by a capacitor $C_{VCC}$. It may also be used to supply some external circuits.

The $V_{CC}$ voltage (see also Figs 4 and 5) depends on the current consumed by the IC and the peripheral circuits as:

$$V_{CC0} = V_{LN} - R_{CC} \times I_{CC}$$

$$V_{CC} = V_{CC0} - R_{CC} \times (I_{P} + I_{rec})$$

Where $I_{rec}$ is the current consumed by the output stage of the earpiece amplifier.

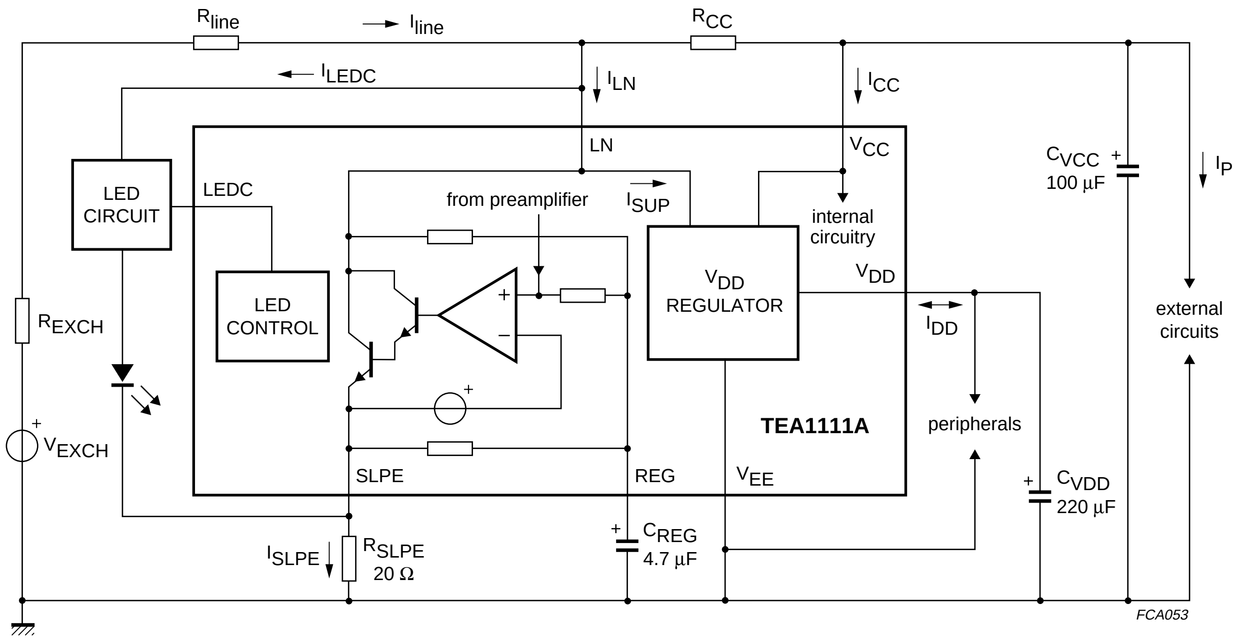



Fig.3 Supply configuration.

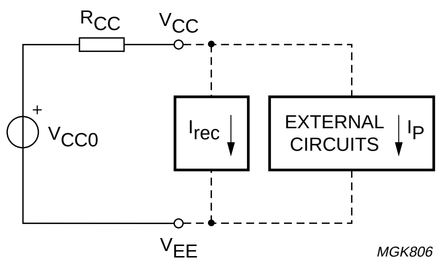
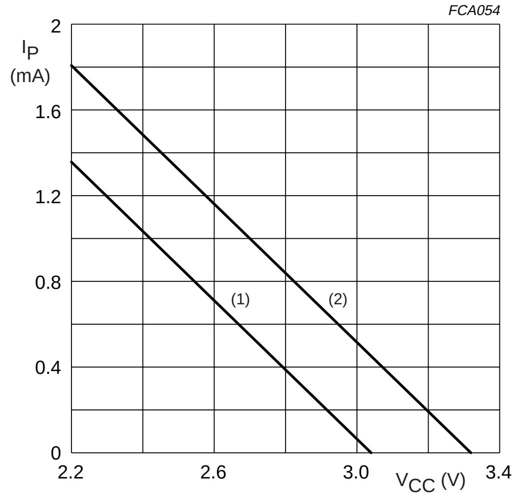



Fig.4 $V_{CC}$ used as supply voltage for external circuits.




$V_{CC} \geq 2.2$ V; $V_{LN} = 4$ V at $I_{line} = 15$ mA; $R_{CC} = 619\ \Omega$; $R_{SLPE} = 20\ \Omega$.

(1) Curve 1 is valid when the earpiece amplifier is driven: $V_{QR(rms)} = 150$ mV; $R_L = 150\ \Omega$.

(2) Curve 2 is valid when the earpiece amplifier is not loaded.

Fig.5 Typical current $I_P$ available from $V_{CC}$ for peripheral circuitry.

THE REGULATED SUPPLY POINT (PIN $V_{DD}$)

The $V_{DD}$ regulator delivers a stabilized voltage for the peripherals in transmission mode (nominal $V_{LN}$) as well as in ringer mode ($V_{LN} = 0$ V). The regulator (see Fig.6) consists of a sense input circuit fed by pin LN, a current switch and a $V_{DD}$ output stabilizer.

The regulator function depends on the transmission, ringer and trickle modes as follows:

- Transmission mode: The regulator operates as a current source at the LN input; it takes a constant current of $I_{SUP} = 4.3$ mA (at nominal conditions) from pin LN. The current switch reduces the distortion on the line at large signal swings. Output $V_{DD}$ follows the DC voltage at pin LN (with typically 0.35 V difference) up to $V_{DD} = 3.25$ V. The input current of the regulator is constant while the output (source) current is determined by the consumption of the peripherals. The difference between input and output currents is shunted by the internal $V_{DD}$ stabilizer.
- Ringer mode: The regulator operates as a shunt stabilizer to keep $V_{DD}$ at 3.3 V. The input voltage $V_{LN}$ equals 0 V while the input current into pin $V_{DD}$ is delivered by the ringing signal. $V_{DD}$ has to be decoupled by a capacitor $C_{VDD}$.
- Trickle mode: When $V_{DD}$ is below 2 V, the regulator is inhibited. The current consumption of the $V_{DD}$ regulator in trickle mode is very low to save most of the trickle current for memory retention of a dialler.

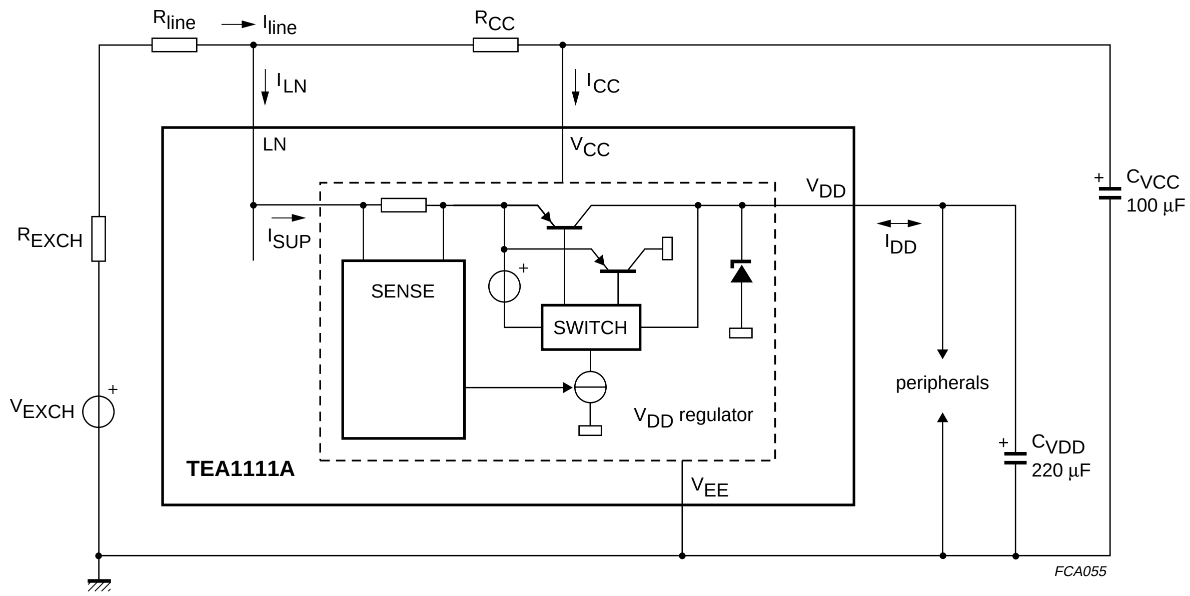



Fig.6 $V_{DD}$ regulator configuration.

### LED control (pin LEDC)

The TEA1111A gives an on-hook/off-hook status indication. This is achieved by a current made available at pin LEDC to drive an external LED circuit connected between pins SLPE and LN (see Fig.7). In the low voltage area, which corresponds to low line current conditions, no current is available for this LED. For line currents higher than a threshold, the LEDC current increases proportionally to the line current (with a ratio of 1:150). The LEDC current is internally limited to 470 µA (see Fig.8).

For 12 mA < $I_{line}$ < 82 mA: $$I_{LEDC} = \frac{I_{line} - 12}{150}$$

This LED circuit is referenced to SLPE. Consequently, all the LED supply current will flow through the $R_{SLPE}$ resistor, and does not affect the behaviour of the AGC.

### Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the $R_{CC}$ resistor. The equivalent impedance of the circuit is illustrated in Fig.9.

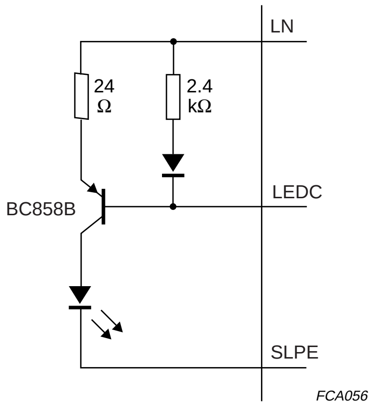



Fig.7 LED circuit configuration.

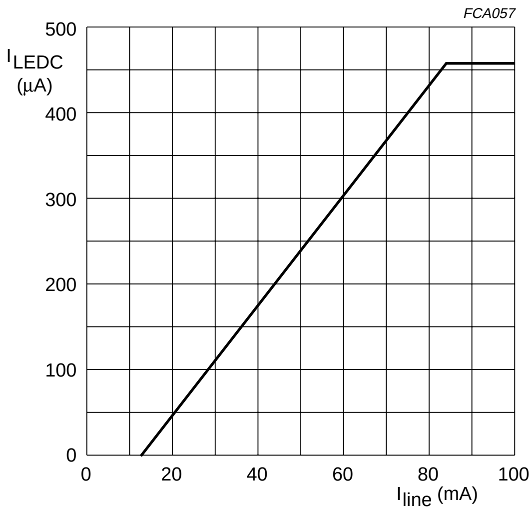
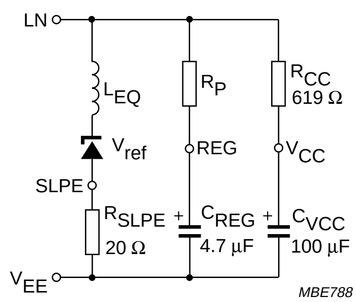



Fig.8 LEDC current versus line current.




$L_{EQ} = C_{REG} \times R_{SLPE} \times R_P$.
$R_P$ = internal resistance.
$R_P$ = 17.5 kΩ.

Fig.9 Equivalent impedance between LN and $V_{EE}$.

**Transmit stage (pins MIC+, MIC– and DTMF)**

MICROPHONE AMPLIFIER (PINS MIC+ AND MIC–)

The TEA1111A has symmetrical microphone inputs. The input impedance between pins MIC+ and MIC– is 68 kΩ (2 × 34 kΩ). The voltage gain from pins MIC+/MIC– to pin LN is set at 44.2 dB (typical) at 600 Ω line load.

Automatic gain control is provided on this amplifier for line loss compensation.

DTMF AMPLIFIER (PIN DTMF)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones are also sent to the receive output QR at a low level (confidence tone), the level is controlled by pin VCI.

The TEA1111A has an asymmetrical DTMF input. The input impedance between DTMF and $V_{EE}$ is 20 kΩ and it is biased at $V_{EE}$. The voltage gain from pin DTMF to pin LN is set at 25.9 dB.

Automatic gain control has no effect on the DTMF amplifier.

**Receiving stage (pins IR, GAR, QR and VCI)**

The receive part consists of an earpiece amplifier and a volume control block.

EARPIECE AMPLIFIER

The earpiece amplifier has one input (IR) and one output (QR). The input impedance between pin IR and pin $V_{EE}$ is 22 kΩ. When pin VCI is tied to $V_{EE}$, the voltage gain from pin IR to pin QR is set at 27.4 dB (typical) which reduces the attenuation of the receive signal by the anti-sidetone network from 32 dB to 4.6 dB. The gain can be decreased by connecting an external resistor $R_{GARext}$ between pins GAR and QR; the adjustment range is 6 dB. Two external capacitors $C_{GAR}$ (connected between pins GAR and QR) and $C_{GARS}$ (connected between pins GAR and $V_{EE}$) ensure stability. Capacitor $C_{GAR}$ provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times R_{GARint}$. Where $R_{GARint}$ is the internal resistor (123 kΩ typical) which sets the gain. The relationship $C_{GARS} = 10 \times C_{GAR}$ must be complied with to ensure stability.

The output voltage of the earpiece amplifier is specified for continuous wave drive. The maximum output swing depends on the DC line voltage, the $R_{CC}$ resistor, the $I_{CC}$ current consumption of the circuit, the $I_P$ current consumption of the peripheral circuits and the load impedance.

Automatic gain control is provided on this amplifier for line loss compensation.

VOLUME CONTROL (PIN VCI)

A positive DC voltage applied to pin VCI allows the gain of the earpiece amplifier to be increased in steps of 4.85 dB. The volume control range is 27.4 to 41.9 dB (14.5 dB typical). A proportional voltage decoder at pin VCI defines a gain of 27.4 dB when $V_{VCI}$ equals $V_{EE}$ and a gain of 41.9 dB when $V_{VCI}$ equals $V_{DD}$.

The intermediate steps correspond to: $V_{VCI} = \frac{1}{3}V_{DD}$

and $V_{VCI} = \frac{2}{3}V_{DD}$ .

### Automatic gain control (pin AGC)

The TEA1111A performs automatic line loss compensation. The automatic gain control varies the gain of the microphone amplifier and the gain of the receive amplifier in accordance with the DC line current.

The control range is 6.0 dB (which corresponds approximately to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).

The IC can be used with different configurations of feeding bridge (supply voltage and bridge resistance) by connecting an external resistor $R_{AGC}$ between pins AGC and $V_{EE}$. This resistor enables the $I_{start}$ and $I_{stop}$ line currents to be increased (the ratio between $I_{start}$ and $I_{stop}$ is not affected by the resistor). The AGC function is disabled when pin AGC is left open circuit.

### Mute function (pin $\overline{\text{MUTE}}$)

The mute function performs the switching between the speech mode and the dialling mode.

When $\overline{\text{MUTE}}$ is LOW, the DTMF input is enabled and the microphone and receive amplifier inputs are disabled.
In this mode, the DTMF tones are sent to the receive output at a low level (confidence tone).

When $\overline{\text{MUTE}}$ is HIGH, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled. The $\overline{\text{MUTE}}$ input is provided with an internal pull-up current source to $V_{DD}$.

### Sidetone suppression

The TEA1111A anti-sidetone network comprising $R_{CC}$ // $Z_{line}$, $R_{ast1}$, $R_{ast2}$, $R_{ast3}$, $R_{SLPE}$ and $Z_{bal}$ (see Fig.10) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{R_{ast2} \times (R_{ast3} + R_{SLPE})}{R_{ast1} \times R_{SLPE}}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for $Z_{bal}$.

In practice, $Z_{line}$ varies considerably with the line type and the line length. Therefore, the value of $Z_{bal}$ should be for an average line length, which gives satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between $Z_{bal}$ and the impedance of the average line.

The anti-sidetone network for the TEA1111A attenuates the receive signal from the line by 32 dB before it enters the receive stage. The attenuation is almost constant over the whole audio frequency range.

A Wheatstone bridge configuration (see Fig.11) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *“Semiconductors for Wired Telecom Systems; Applications Handbook IC03b”*.

For ordering information, please contact the Philips Semiconductors sales office.

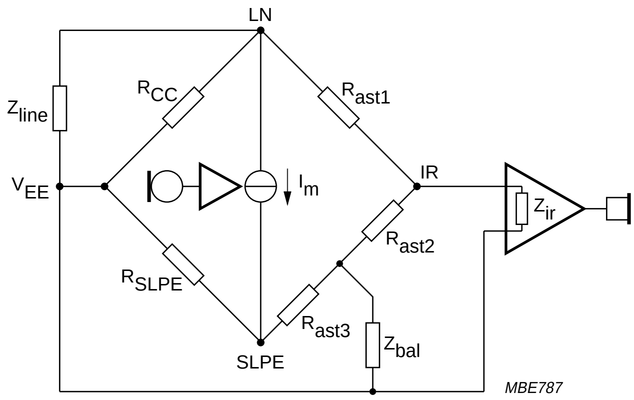



Fig.10 Equivalent circuit of TEA1111A anti-sidetone bridge.

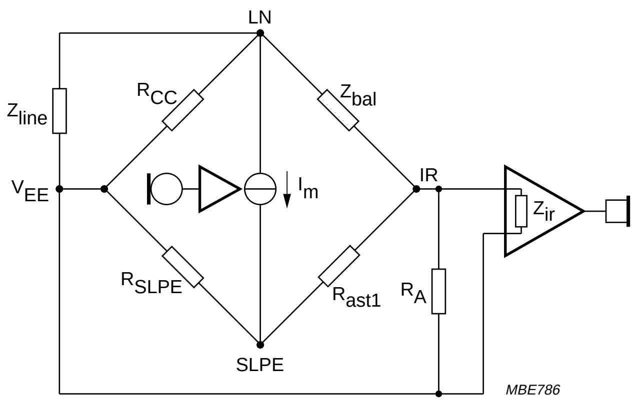



Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{LN}$ | positive continuous line voltage | | $V_{EE}$ – 0.4 | 12 | V |
| | repetitive line voltage during switch-on or line interruption | | $V_{EE}$ – 0.4 | 13.2 | V |
| $I_{DD}$ | maximum input current at pin $V_{DD}$ | | – | 75 | mA |
| $V_{CC}$ | supply voltage | | $V_{EE}$ – 0.4 | 12 | V |
| $V_{\overline{MUTE}}$, $V_{VCI}$ | maximum voltage on pins $\overline{MUTE}$ and VCI | | $V_{EE}$ – 0.4 | $V_{DD}$ + 0.4 | V |
| $V_{n(max)}$ | maximum voltage on all pins except pins $V_{DD}$, $\overline{MUTE}$ and VCI | | $V_{EE}$ – 0.4 | $V_{CC}$ + 0.4 | V |
| $I_{line}$ | line current | $R_{SLPE}$ = 20 Ω; see Fig.12 | – | 140 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = 75 °C | | | |
| | TEA1111AT; (see Fig.12) | | – | 400 | mW |
| | TEA1111AUH; note 1 | | – | – | mW |
| $T_{stg}$ | storage temperature | | –40 | +125 | °C |
| $T_{amb}$ | ambient temperature | | –25 | +75 | °C |
| $T_j$ | junction temperature | | – | +125 | °C |

**Note**

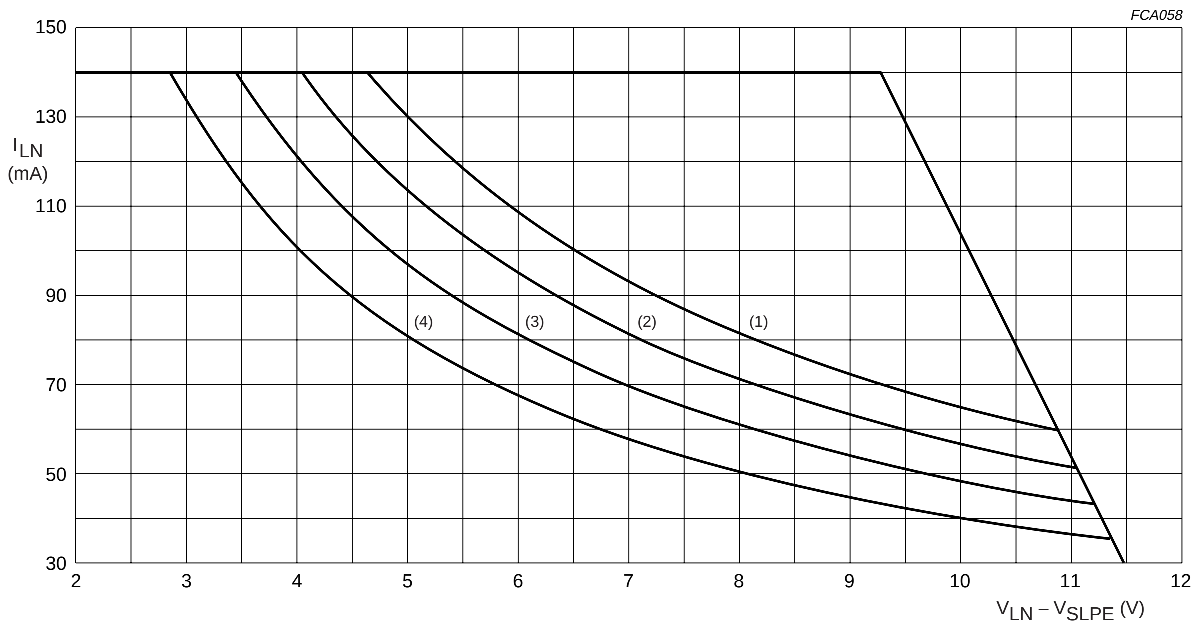
1. Mostly dependent on the maximum required ambient temperature, on the voltage between LN and SLPE and on the thermal resistance between die ambient temperature. This thermal resistance depends on the application board layout and on the materials used. Figure 13 shows the safe operating area versus this thermal resistance for ambient temperature $T_{amb}$ = 75 °C

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; note 1 | | |
| | TEA1111AT | | 110 | K/W |
| | TEA1111AUH | | tbf by customer in application | K/W |

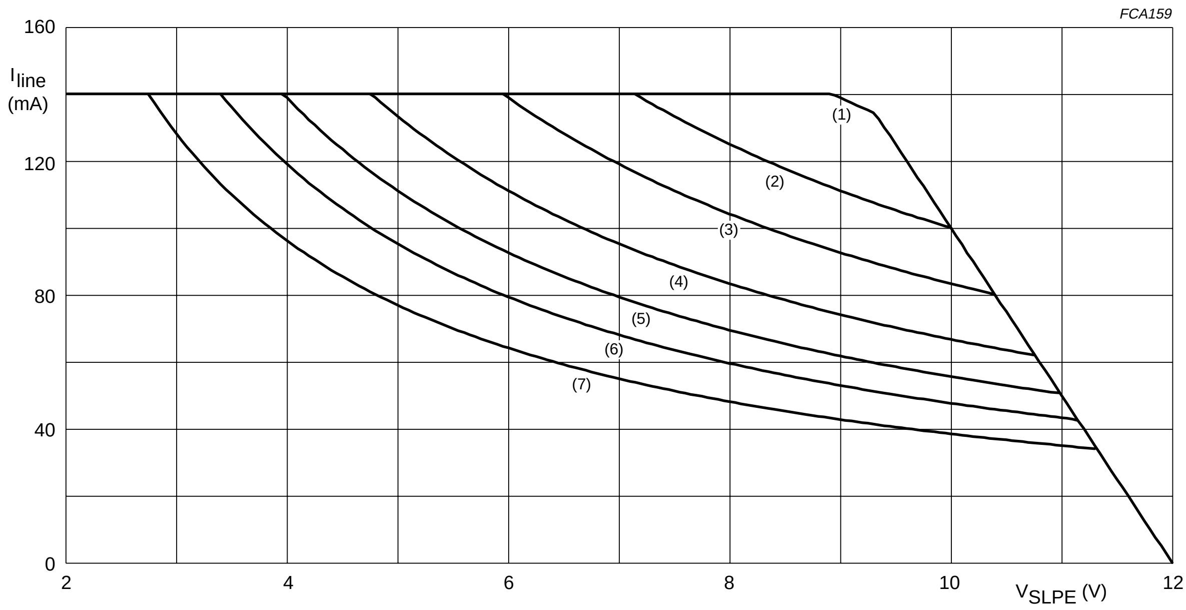
**Note**

1. Mounted on epoxy board 40.1 × 19.1 × 1.5 mm.




(1) $T_{amb}$ = 45 °C; $P_{tot}$ = 0.666 W.
(2) $T_{amb}$ = 55 °C; $P_{tot}$ = 0.583 W.
(3) $T_{amb}$ = 65 °C; $P_{tot}$ = 0.500 W.
(4) $T_{amb}$ = 75 °C; $P_{tot}$ = 0.416 W.

Fig.12 SO16 safe operating area (TEA1111AT).




| LINE | $R_{th(j-a)}$ (K/W) |
|---|---|
| (1) | 40 |
| (2) | 50 |
| (3) | 60 |
| (4) | 75 |
| (5) | 90 |
| (6) | 105 |
| (7) | 130 |

Fig.13 Safe operating area at $T_{amb}$ = 75 °C (TEA1111AUH).

## CHARACTERISTICS

$I_{line}$ = 15 mA; $V_{EE}$ = 0 V; $V_{VCI}$ = 0 V; $R_{SLPE}$ = 20 Ω; pin AGC connected to $V_{EE}$; $Z_{line}$ = 600 Ω; f = 1 kHz; measured according to test circuits given in Figs 15, 16 and 17; $T_{amb}$ = 25 °C for TEA1111AT; $T_j$ = 25 °C for TEA1111AUH; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supply (pins LN, $V_{CC}$, SLPE, REG and $V_{DD}$)** | | | | | | |
| THE LINE INTERFACE (PINS LN, SLPE AND REG) | | | | | | |
| $V_{ref}$ | stabilized reference voltage between pins LN and SLPE | | 3.5 | 3.8 | 4.1 | V |
| $V_{LN}$ | DC line voltage | $I_{line}$ = 1 mA | – | 1.5 | – | V |
| | | $I_{line}$ = 4 mA | – | 2.5 | – | V |
| | | $I_{line}$ = 15 mA | 3.7 | 4.0 | 4.3 | V |
| | | $I_{line}$ = 140 mA | – | 6.7 | 7.2 | V |
| $V_{LN(Rext)}$ | DC line voltage with an external resistor $R_{VA}$ | $R_{VA}$ = 90 kΩ (between pins LN and REG) | – | 3.6 | – | V |
| $\Delta V_{LN(T)}$ | DC line voltage variation with temperature referenced to 25 °C | $T_{amb}$ = –25 to +75 °C | – | ±40 | – | mV |
| THE INTERNAL SUPPLY POINT (PIN $V_{CC}$) | | | | | | |
| $I_{CC}$ | internal current consumption | $V_{CC}$ = 3.3 V | – | 1.15 | 1.4 | mA |
| $V_{CC}$ | supply voltage for internal circuitry | $I_P$ = 0 mA | – | 3.3 | – | V |
| THE REGULATED SUPPLY POINT (PIN $V_{DD}$) | | | | | | |
| $I_{SUP}$ | input current of the $V_{DD}$ regulator (current from pin LN not flowing through pin SLPE) | $I_{line}$ = 1 mA | – | 0 | – | mA |
| | | $I_{line}$ = 4 mA | – | 1.2 | – | mA |
| | | $I_{line}$ ≥ 11 mA | – | 4.3 | – | mA |
| $V_{DD}$ | regulated supply voltage in: | | | | | |
| | speech mode | $I_{DD}$ = –3 mA; $V_{LN}$ > 3.6 V + 0.28 V (typ.); $I_{line}$ ≥ 11 mA | 2.95 | 3.25 | 3.55 | V |
| | speech mode at reduced performance | $I_{line}$ = 4 mA | – | $V_{LN}$ – 0.35 | – | V |
| | ringer mode | $I_{line}$ = 0 mA; $I_{DD}$ = 75 mA | 3.0 | 3.3 | 3.6 | V |
| $I_{DD}$ | regulated supply current available in: | | | | | |
| | speech mode | $I_{line}$ ≥ 11 mA | – | – | –3 | mA |
| | speech mode at reduced performance | $I_{line}$ = 4 mA | – | –1 | – | mA |
| | trickle mode | $I_{line}$ = 0 mA; $V_{CC}$ discharging; $V_{DD}$ = 1.2 V | – | – | 100 | nA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **LED control (pin LEDC)** | | | | | | |
| $I_{line(h)}$ | highest line current for $I_{LEDC} < 5\ \mu A$ | | – | 13 | – | mA |
| $I_{line(l)}$ | lowest line current for maximum $I_{LEDC}$ | | – | 82 | – | mA |
| $I_{LEDC(max)}$ | maximum available output current from pin LEDC | | – | 470 | – | μA |
| **Transmit stage (pins MIC+, MIC– and DTMF)** | | | | | | |
| MICROPHONE AMPLIFIER (PINS MIC+ AND MIC–) | | | | | | |
| $\lvert Z_i \rvert$ | input impedance | | | | | |
| | differential between pins MIC+ and MIC– | | – | 68 | – | kΩ |
| | single-ended between pins MIC+/MIC– and $V_{EE}$ | | – | 34 | – | kΩ |
| $G_{v(TX)}$ | voltage gain from pins MIC+/MIC– to pin LN | $V_{MIC}$ = 4 mV (RMS) | 43.2 | 44.2 | 45.2 | dB |
| $\Delta G_{v(TX)(f)}$ | voltage gain variation with frequency referenced to 1 kHz | f = 300 to 3400 Hz | – | ±0.2 | – | dB |
| $\Delta G_{v(TX)(T)}$ | voltage gain variation with temperature referenced to 25 °C | $T_{amb}$ = –25 to +75 °C | – | ±0.3 | – | dB |
| CMRR | common mode rejection ratio | | – | 80 | – | dB |
| $V_{LN(max)(rms)}$ | maximum sending signal (RMS value) | $I_{line}$ = 15 mA; THD = 2% | 1.8 | 2 | – | V |
| | | $I_{line}$ = 4 mA; THD = 10% | – | 0.45 | – | V |
| $V_{no(LN)}$ | noise output voltage at pin LN | psophometrically weighted (P53 curve); pins MIC+/MIC– short circuited through 200 Ω | – | –77 | – | dBmp |
| DTMF AMPLIFIER (PIN DTMF) | | | | | | |
| $\lvert Z_i \rvert$ | input impedance | | – | 20 | – | kΩ |
| $G_{v(DTMF)}$ | voltage gain from pin DTMF to pin LN | $V_{DTMF}$ = 20 mV (RMS); $\overline{MUTE}$ = LOW | 24.9 | 25.9 | 26.9 | dB |
| $\Delta G_{v(DTMF)(f)}$ | voltage gain variation with frequency referenced to 1 kHz | f = 300 to 3400 Hz | – | ±0.2 | – | dB |
| $\Delta G_{v(DTMF)(T)}$ | voltage gain variation with temperature referenced to 25 °C | $T_{amb}$ = –25 to +75 °C | – | ±0.4 | – | dB |
| $G_{v(ct)}$ | voltage gain from pin DTMF to pin QR (confidence tone) | $V_{DTMF}$ = 20 mV (RMS); $R_L$ = 150 Ω; $\overline{MUTE}$ = LOW; $V_{VCI}$ = 0 V | – | –15.6 | – | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Receive stage (pins IR, GAR, QR and VCI)** | | | | | | |
| THE EARPIECE AMPLIFIER (PINS IR AND QR) | | | | | | |
| $\lvert Z_i \rvert$ | input impedance | | – | 22 | – | kΩ |
| $G_{v(QR)}$ | voltage gain from pin IR to pin QR | $V_{IR}$ = 4 mV (RMS); $V_{VCI}$ = 0 V | 26.4 | 27.4 | 28.4 | dB |
| $\Delta G_{v(QR)(f)}$ | voltage gain variation with frequency referenced to 1 kHz | f = 300 to 3400 Hz | – | ±0.2 | – | dB |
| $\Delta G_{v(QR)(T)}$ | voltage gain variation with temperature referenced to 25 °C | $T_{amb}$ = –25 to +75 °C | – | ±0.3 | – | dB |
| $\Delta G_{v(QR)}$ | voltage gain reduction range | external resistor connected between pins GAR and QR | – | – | 6 | dB |
| $V_{QR(max)(rms)}$ | maximum receiving signal on pin QR (RMS value) | $I_P$ = 0 mA; sine wave drive; $R_L$ = 150 Ω; THD = 2%; $V_{VCI}$ = $V_{DD}$ | 0.5 | 0.6 | – | V |
| | | $I_P$ = 0 mA; sine wave drive; $R_L$ = 450 Ω; THD = 2%; $V_{VCI}$ = $V_{DD}$ | 0.8 | 0.9 | – | V |
| $V_{no(QR)(rms)}$ | noise output voltage at pin QR (RMS value) | IR open circuit; $R_L$ = 150 Ω; $V_{VCI}$ = 0 V; psophometrically weighted (P53 curve) | – | –90 | – | dBVp |
| | | $V_{VCI}$ = $V_{DD}$ | – | –75 | – | dBVp |
| VOLUME CONTROL (PIN VCI) | | | | | | |
| $\Delta G_{v(QR)max}$ | maximum increase in voltage gain | $V_{IR}$ = 4 mV (RMS); $V_{VCI}$ = $V_{DD}$ | 12 | 14.5 | 17 | dB |
| $\Delta G_{v(QR)step}$ | step voltage gain | $V_{IR}$ = 4 mV (RMS) | 3.85 | 4.85 | 5.85 | dB |
| **Automatic gain control (pin AGC)** | | | | | | |
| $\Delta G_{v(trx)}$ | voltage gain control range for microphone and earpiece amplifiers w.r.t. $I_{line}$ = 15 mA | $I_{line}$ = 85 mA | – | 6.0 | – | dB |
| $I_{start}$ | highest line current for maximum gain | | – | 23 | – | mA |
| $I_{stop}$ | lowest line current for min. gain | | – | 59 | – | mA |
| **Mute function (pin $\overline{MUTE}$)** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | $V_{EE}$ – 0.4 | – | $V_{EE}$ + 0.3 | V |
| $V_{IH}$ | HIGH-level input voltage | | $V_{EE}$ + 1.5 | – | $V_{DD}$ + 0.4 | V |
| $I_{MUTE}$ | input current | | –10 | –2 | – | μA |
| $\Delta G_{v(trx)(m)}$ | voltage gain reduction for: | | | | | |
| | microphone amplifier | $\overline{MUTE}$ = LOW | – | 80 | – | dB |
| | earpiece amplifier | $\overline{MUTE}$ = LOW | – | 80 | – | dB |
| | DTMF amplifier | $\overline{MUTE}$ = HIGH | – | 80 | – | dB |

## TEST AND APPLICATION INFORMATION

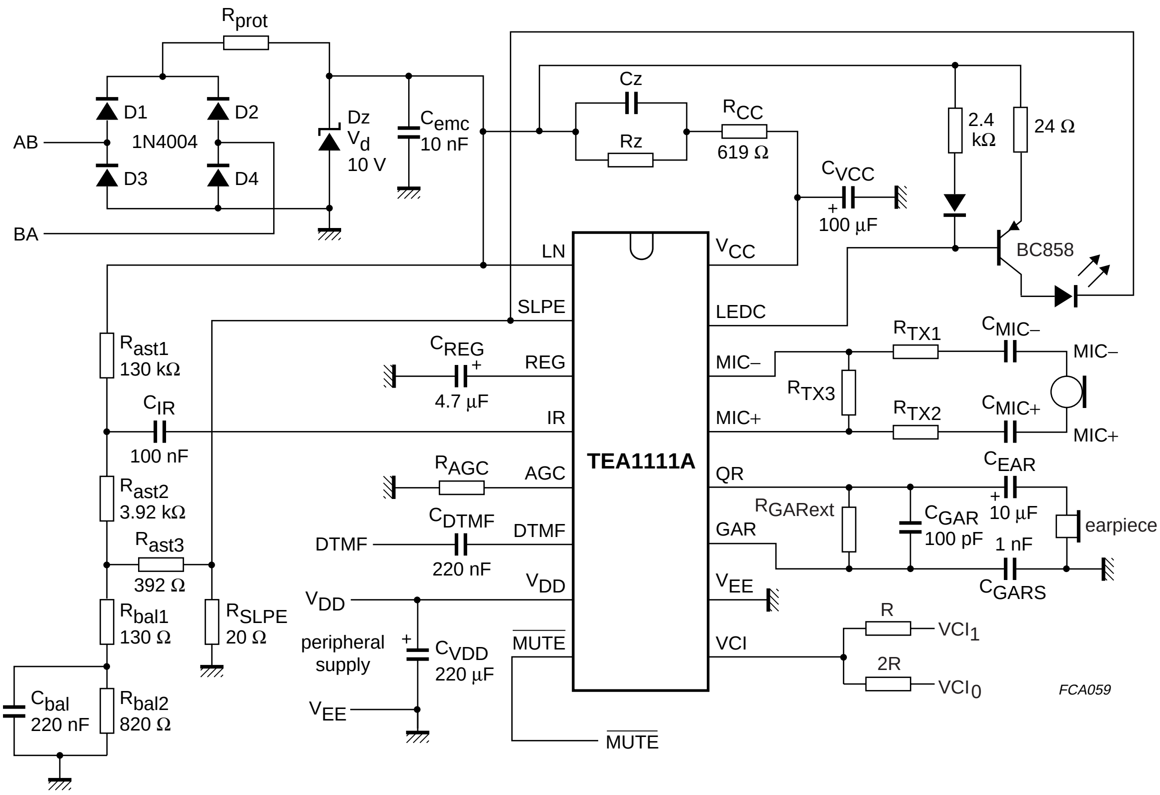
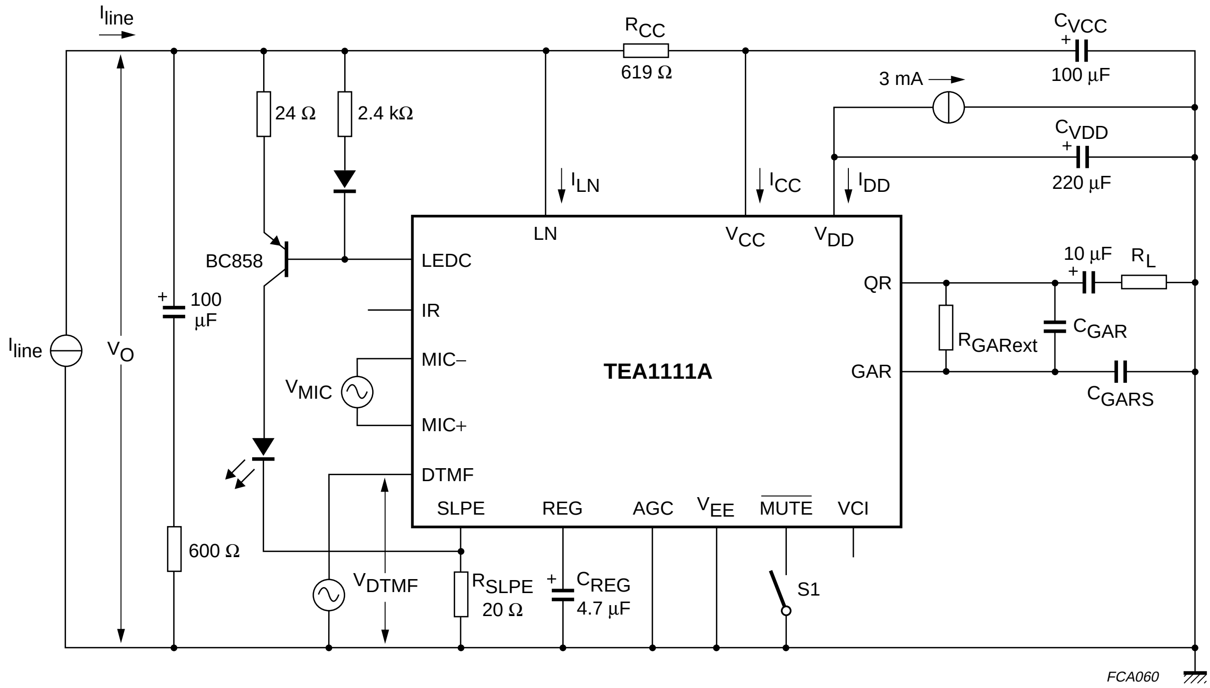



Fig.14 Basic application diagram.



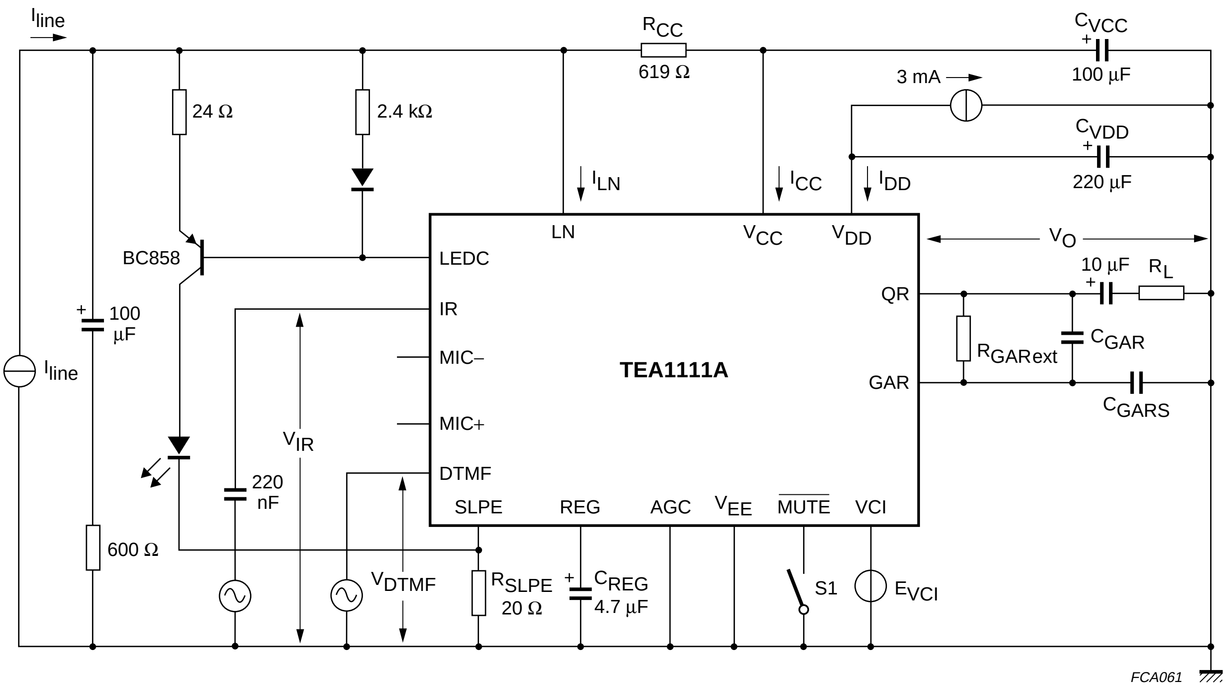

Voltage gain defined as $G_v = 20 \log \left|\frac{V_O}{V_I}\right|$; $V_I = V_{MIC}$ or $V_{DTMF}$.

Microphone gain: S1 = open.

DTMF gain: S1 = closed.

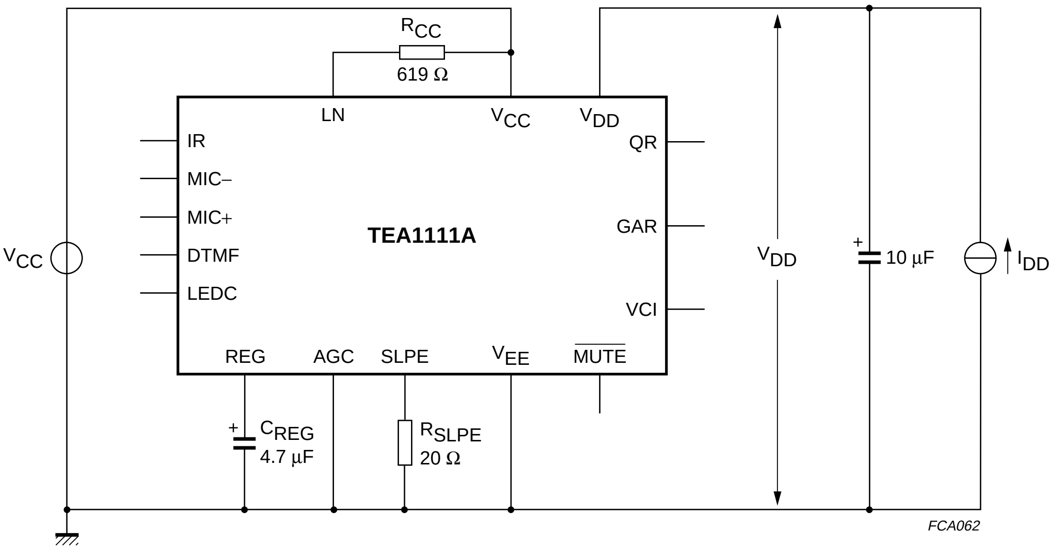
Inputs not being tested should be open circuit.

Fig.15 Test circuit for defining transmit gains.




Voltage gain defined as $G_v = 20 \log \left|\frac{V_O}{V_I}\right|$; $V_I = V_{IR}$ or $V_{DTMF}$.
Earpiece gain: S1 = open.
Confidence tone: S1 = closed.
Inputs not being tested should be open circuit.

Fig.16 Test circuit for defining earpiece gains.




Inputs not being tested should be open circuit.

Fig.17 Test circuit for defining regulated supply ($V_{DD}$) performance in ringer and trickle modes.

### BONDING PAD LOCATIONS FOR TEA1111AUH

All x/y coordinates represent the position of the centre of the pad (in µm) with respect to the origin (x/y = 0/0) of the die (see Fig.18). The size of all pads is 80 µm × 80 µm.

| SYMBOL | PAD | COORDINATES | |
|---|---|---|---|
| | | x | y |
| LN | 1 | 110 | 578.5 |
| SLPE | 2 | 110 | 260 |
| REG | 3 | 155 | 110 |
| IR | 4 | 432 | 110 |
| AGC | 5 | 967.2 | 110 |
| DTMF | 6 | 1203.2 | 110 |
| $V_{DD}$ | 7 | 1394.5 | 115.5 |
| $\overline{MUTE}$ | 8 | 1400 | 350.8 |
| n.c. | 9 | 1400 | 537.8 |
| VCI | 10 | 1400 | 1013 |
| $V_{EE}$ | 11 | 1398.5 | 1249 |
| $V_{EE}$ | 12 | 1397.8 | 1360 |
| QR | 13 | 1238.2 | 1360 |
| GAR | 14 | 1032.5 | 1360 |
| MIC+ | 15 | 370.8 | 1360 |
| MIC- | 16 | 150.5 | 1360 |
| LEDC | 17 | 110.8 | 1211.2 |
| $V_{CC}$ | 18 | 110 | 980.5 |

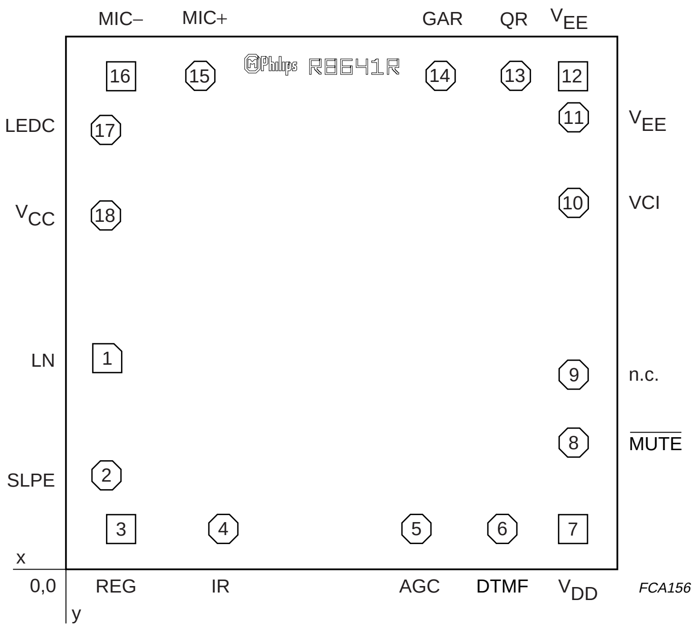
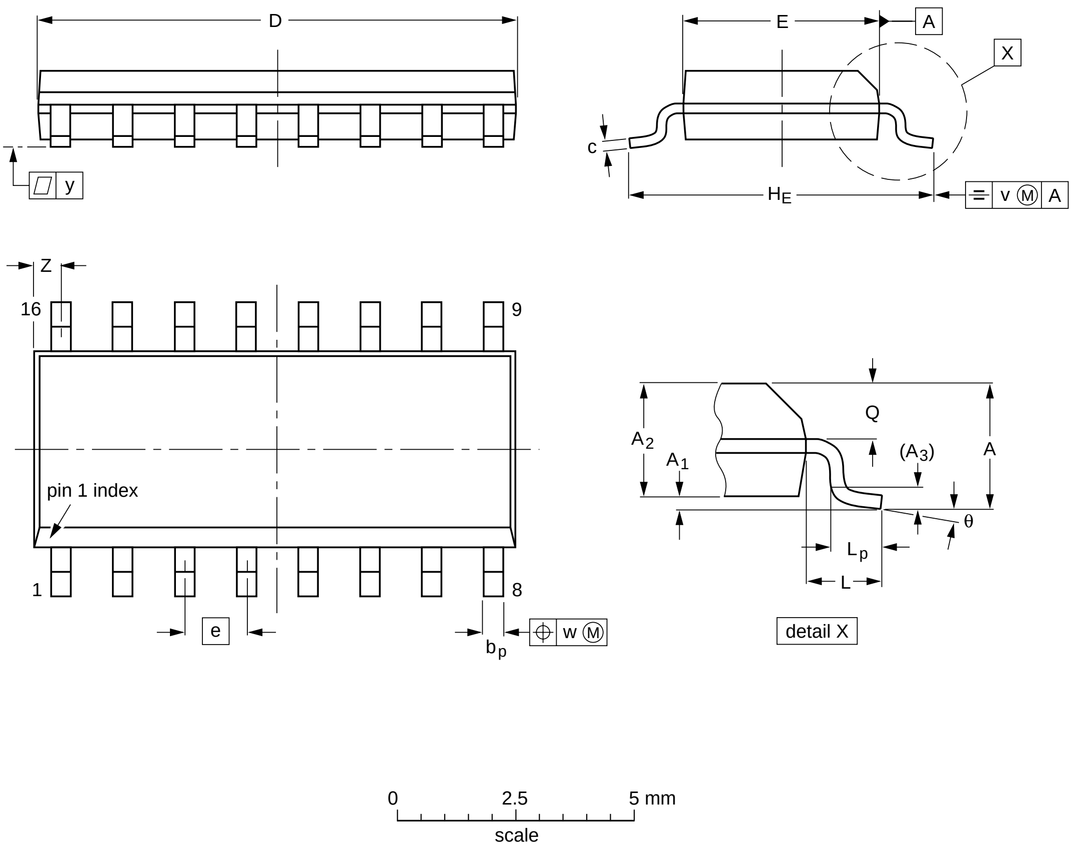



Fig.18 TEA1111AUH bonding pad locations.

## PACKAGE OUTLINE

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~97-05-22~~<br>99-12-27 |

## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Suitability of surface mount IC packages for wave and reflow soldering methods**

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW[1] |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS | not suitable[2] | suitable |
| PLCC[3], SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended[3][4] | suitable |
| SSOP, TSSOP, VSO | not recommended[5] | suitable |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

| | |
|---|---|
| **Data sheet status** | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
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| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
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**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

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**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

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**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V, Tel. +45 33 29 3333, Fax. +45 33 29 3905

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**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 2353 60, Fax. +49 40 2353 6300

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**India:** Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

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**Poland**: Al.Jerozolimskie 195 B, 02-222 WARSAW, Tel. +48 22 5710 000, Fax. +48 22 5710 001

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**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381, Fax. +1 800 943 0087

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