24AA65/24LC65/24C65

64K I²C™ Smart Serial™ EEPROM

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
24AA65	1.8-6.0V	64 Bytes	C	P, SM
24LC65	2.5-6.0V	64 Bytes	C, I	P, SM
24C65	4.5-6.0V	64 Bytes	C, I, E	P, SM

Features

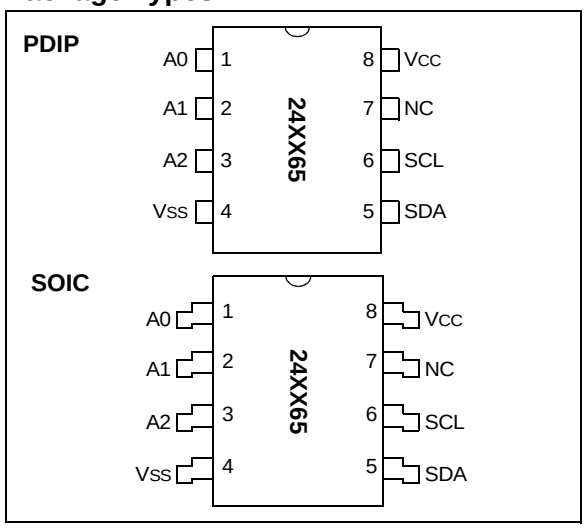
- Voltage operating range: 1.8V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 μA at 6.0V
  - Standby current 1 μA typical
- Industry standard two-wire bus protocol I²C™ compatible
- 8-byte page, or byte modes available
- 2 ms typical write cycle time, byte or page
- 64-byte input cache for fast write loads
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory
- Including 100 kHz (1.8V ≤ Vcc < 4.5V) and 400 kHz (4.5V ≤ VCC ≤ 6.0V) compatibility
- Programmable block security options
- Programmable endurance options
- Schmitt Trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed erase and write cycles
- Power-on/off data protection circuitry
- Endurance:
  - 10,000,000 E/W cycles for a High Endurance Block
  - 1,000,000 E/W cycles for a Standard Endurance Block
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I) -40°C to +85°C
  - Automotive (E) -40°C to +125°C

*24XX65 is used in this document as a generic part number for the 24AA65/24LC65/24C65 devices.

Description

The Microchip Technology Inc. 24AA65/24LC65/24C65 (24XX65)* is a “smart” 8K x 8 Serial Electrically Erasable PROM. This device has been developed for advanced, low-power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24XX65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 1,000,000 erase/write (E/W) cycles ensured. The 24XX65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional address lines allow the connection of up to eight 24XX65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power nonvolatile code and data applications. The 24XX65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

Package Types



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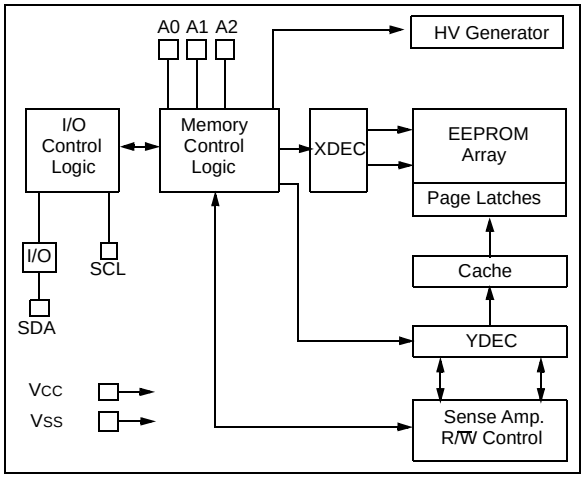
Block Diagram



Pin Function Table

Name	Function
A0, A1, A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data/I/O
SCL	Serial Clock
VCC	+1.8V to 6.0V Power Supply
NC	**No Internal Connection**

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....7.0V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-65°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS	VCC = +1.8V to +6.0V Commercial (C): TA = 0°C to +70°C Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C				
Parameter	**Sym**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High-level input voltage	VIH	.7 VCC	—	V	
Low-level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	**(Note 1)**
Low-level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	—	±1	µA	VIN = .1V to VCC
Output leakage current	ILO	—	±1	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V **(Note 1)** TA = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 6.0V, SCL = 400 kHz
	ICC Read	—	150	µA	VCC = 6.0V, SCL = 400 kHz
Standby current	ICCS	—	5	µA	VCC = 5.0V, SCL = SDA = VCC A0, A1, A2 = VSS

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

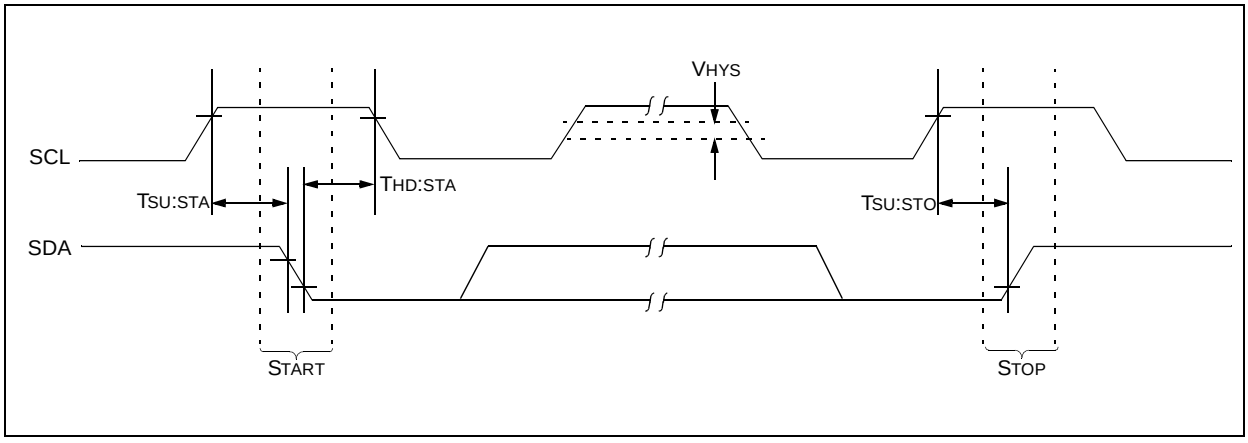


TABLE 1-2: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 1.8V-6.0V STD. Mode		Vcc = 4.5-6.0V FAST Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	**(Note 1)**
SDA and SCL fall time	TF	—	300	—	300	ns	**(Note 1)**
Start condition setup time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
Start condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated Start condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
Stop condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	**(Note 2)**
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	**(Note 1)**, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	50	—	50	—	ns	**(Note 3)**
Write cycle time	TWR	—	5	—	5	ms/page	**(Note 4)**
Endurance High Endurance Block Rest of Array		 10M 1M	 — —	 10M 1M	 — —	cycles	25°C, **(Note 5)**

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.

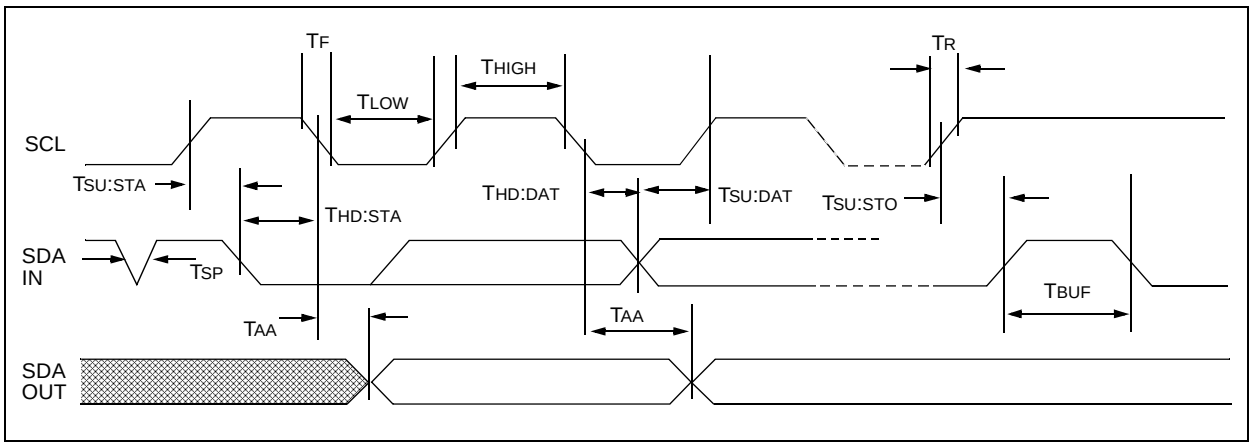
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

5: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be downloaded at www.microchip.com.

FIGURE 1-2: BUS TIMING DATA



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2.0 FUNCTIONAL DESCRIPTION

The 24XX65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX65 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain high.

3.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

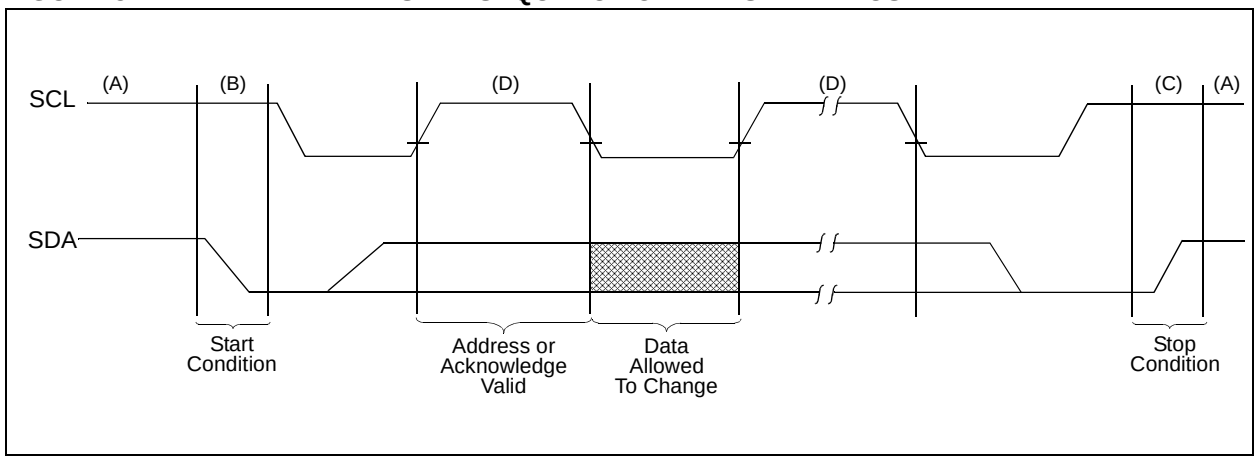
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24XX65 does not generate any Acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX65) must leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

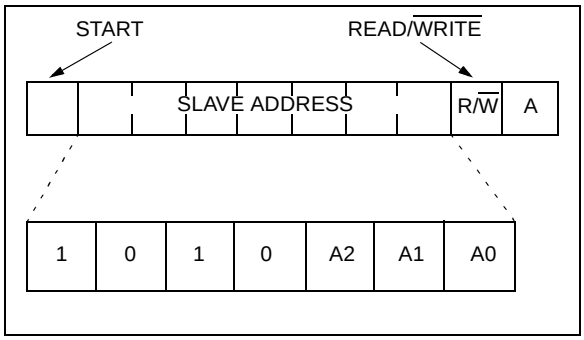


3.6 Device Addressing

A control byte is the first byte received following the Start condition from the master device. The control byte consists of a four-bit control code, for the 24XX65 this is set as '1010' binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three Most Significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 4-1). Because only A12..A0 are used, the upper three address bits must be zeros. The Most Significant bit of the Most Significant Byte is transferred first. Following the Start condition, the 24XX65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a '1010' code and appropriate device select bits, the slave device (24XX65) outputs an Acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24XX65 will select a read or write operation.

Operation	Control Code	Device Select	R/W
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the Start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24XX65) that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24XX65. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX65, the master device will transmit the data word to be written into the addressed memory location. The 24XX65 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and during this time the 24XX65 will not generate Acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX65 in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total), which are temporarily stored in the on-chip page cache of the 24XX65. They will be written from the cache into the EEPROM array after the master has transmitted a Stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the Stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a Stop condition should be generated by the master. If a Stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The Stop condition can be sent at any time during the transfer. As with the byte write operation, once the Stop condition is received an internal write cycle will begin. The 64-byte cache will continue to capture data until a Stop condition occurs or the operation is aborted (Figure 4-2).

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FIGURE 4-1: BYTE WRITE

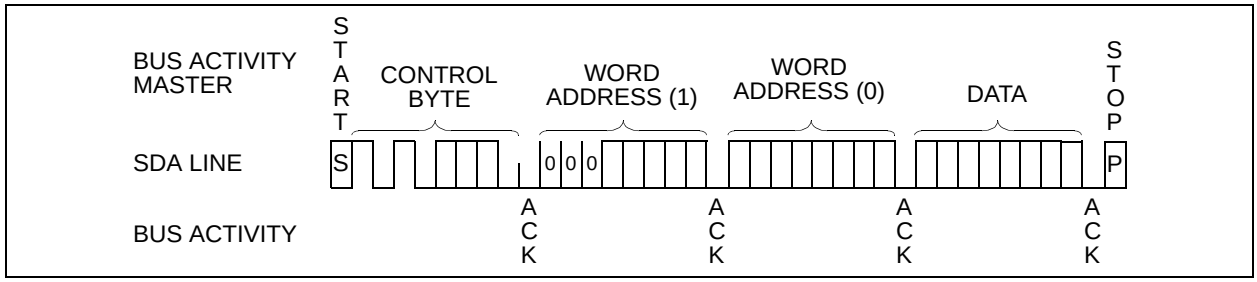


FIGURE 4-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 8-2)

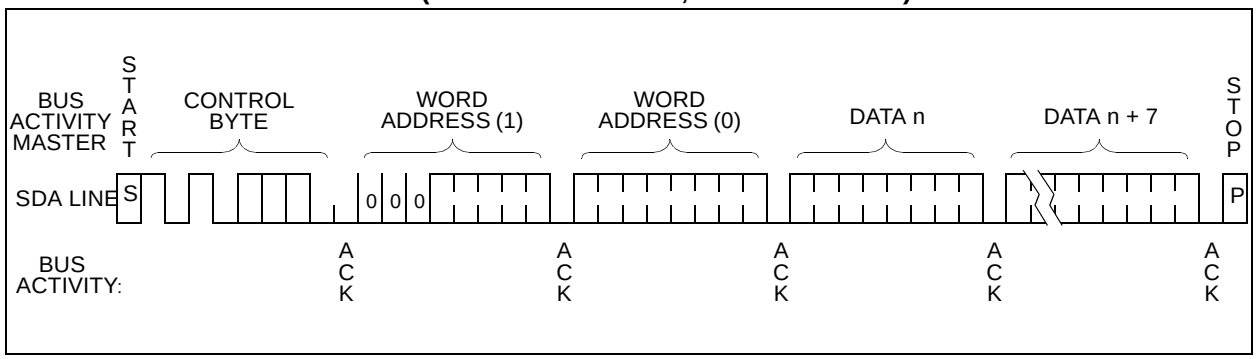


FIGURE 4-3: CURRENT ADDRESS READ

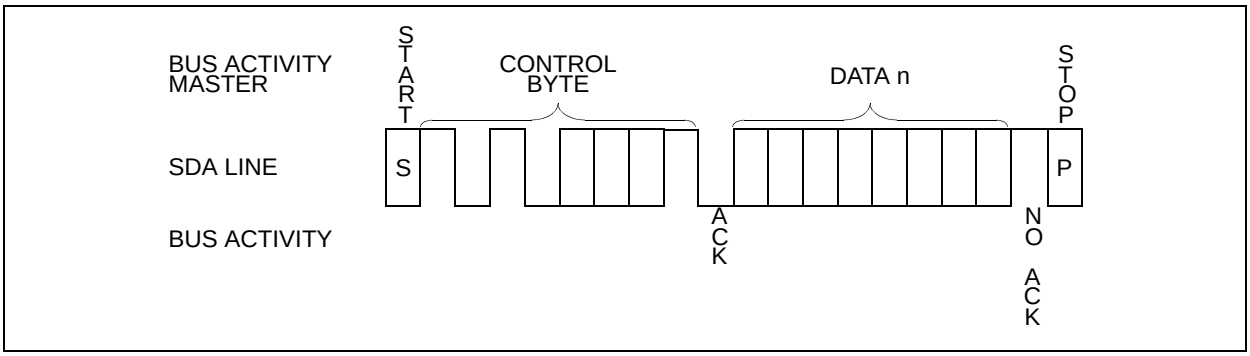


FIGURE 4-4: RANDOM READ

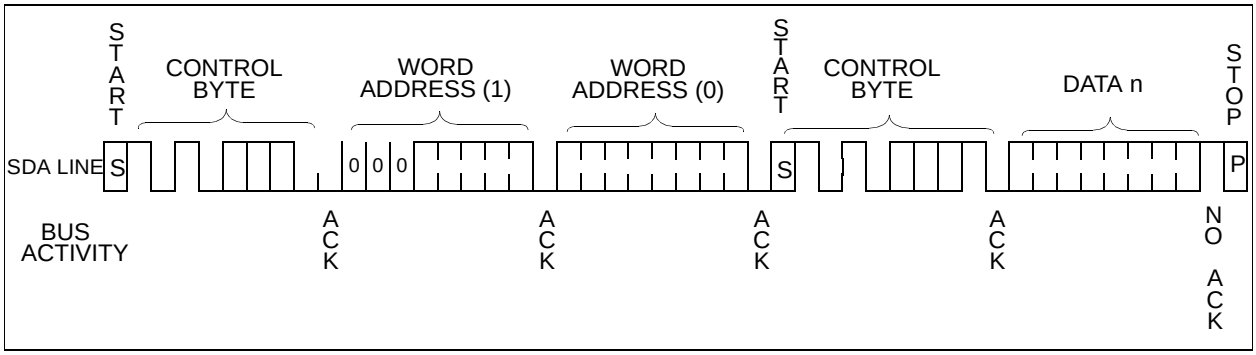
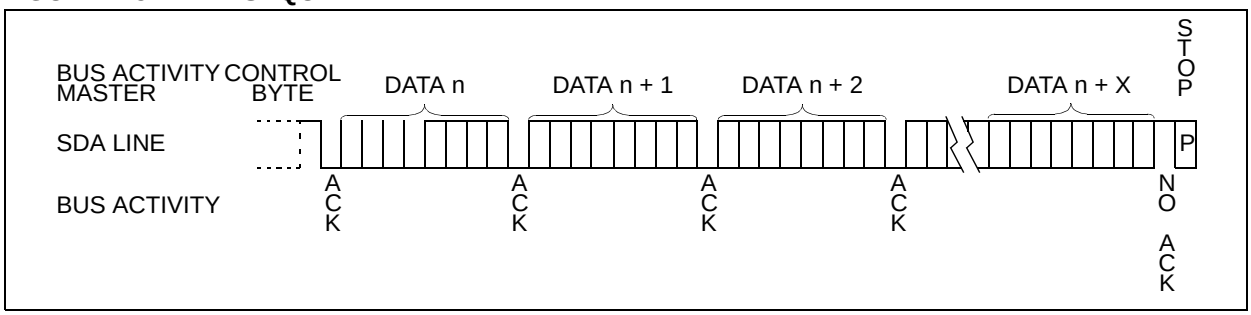


FIGURE 4-5: SEQUENTIAL READ



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5.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

5.1 Current Address Read

The 24XX65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24XX65 issues an acknowledge and transmits the eight-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24XX65 discontinues transmission (Figure 4-3).

5.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24XX65 as part of a write operation (R/$\overline{W}$ bit set to '0'). After the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again, but with the R/$\overline{W}$ bit set to a one. The 24XX65 will then issue an acknowledge and transmit the eight-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition which causes the 24XX65 to discontinue transmission (Figure 4-4).

5.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX65 transmits the first data byte, the master issues an acknowledge as opposed to the Stop condition used in a random read. This acknowledge directs the 24XX65 to transmit the next sequentially addressed 8-bit word (Figure 4-5). Following the final byte transmitted to the master, the master will NOT generate an acknowledge, but will generate a Stop condition.

To provide sequential reads the 24XX65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

5.4 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24XX65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14 and A2 as address bit A15.

5.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt Triggers for 400 kHz (Fast mode) compatibility.

5.6 High Endurance Block

The location of the high endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to '0'. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance. This block will be capable of 10,000,000 erase/write cycles typical (Figure 8-1).

The high endurance block will retain its value as the high endurance block even if it resides within the security block range. The high endurance setting always takes precedence to the security setting.

Note:	The high endurance block cannot be changed after the security option has been set with a length greater than zero. If the H.E. block is not programmed by the user, the default location is the highest block of memory which starts at location 0x1E00 and ends at 0x1FFF.

5.7 Security Options

The 24XX65 has a sophisticated mechanism for write protecting portions of the array. This write-protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE WITH A LENGTH GREATER THAN ZERO.

To invoke the security option, a Write command is sent to the device with the leading bit (bit 7) of the first address byte set to a '1' (Figure 8-1). Bits 1-4 of the first address byte define the starting block number for the protected region.

For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/HE) set high and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write-protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a Stop bit is then sent by the master to complete the command.

If one of the security blocks coincides with the high endurance block, the high endurance setting will take precedence. Also, if the range of the security blocks encompass the high endurance block when the security option is set, the security block range will be set accordingly, but the high endurance block will continue to retain the high endurance setting. As a result, the memory blocks preceding the high endurance block will be set as secure sections.

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a Write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

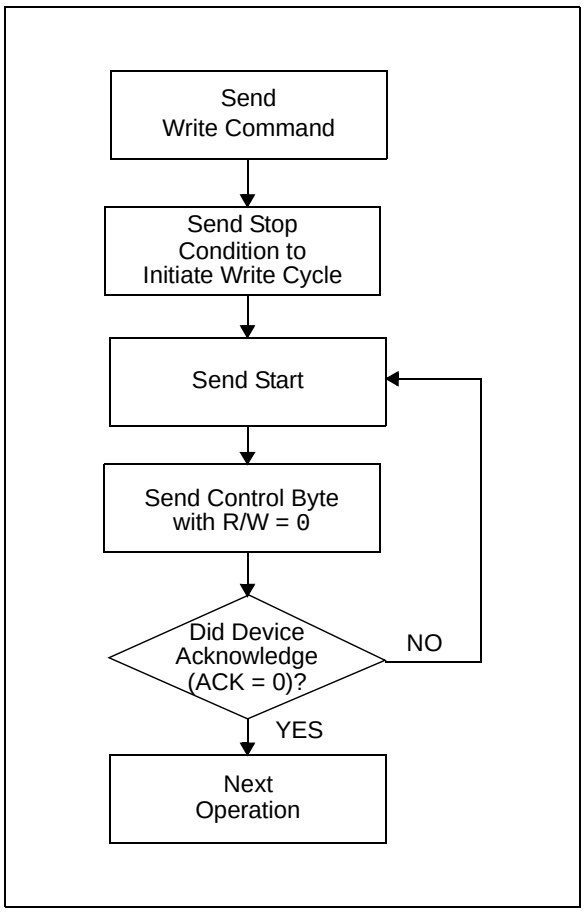
5.8 Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the read bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a Stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (Figure 8-1).

6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command ($R/\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



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7.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64-byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a Write command is initiated, the cache starts loading and will continue to load until a Stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the Stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the Stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.1 Cache Write Starting at a Page Boundary

If a Write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 8-2) a Write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.2 Cache Write Starting at a Non-Page Boundary

When a Write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a Write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three Least Significant Address bits (A2, A1, A0) that were sent as part of the Write command. If the Write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 8-3, a Write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the Stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the Stop bit is sent, only the bytes that have been loaded will be written to the array.

7.3 Power Management

The design incorporates a power Standby mode when not in use and automatically powers off after the normal termination of any operation when a Stop bit is received and all internal functions are complete. This includes any error conditions (i.e., not receiving an Acknowledge or Stop condition per the two-wire bus specification). The device also incorporates V_{DD} monitor circuitry to prevent inadvertent writes (data corruption) during low voltage conditions. The V_{DD} monitor circuitry is powered off when the device is in Standby mode in order to further reduce power consumption.

8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24XX65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-2 and Figure 8-1).

8.2 SDA Serial Address/Data Input/ Output

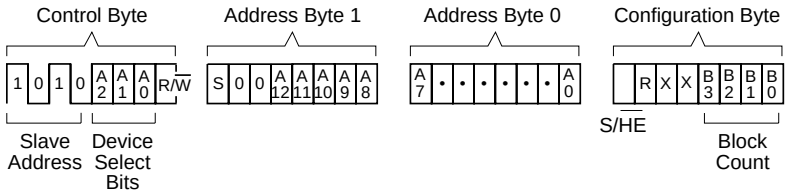
This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to V_{CC} (typical 10 KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

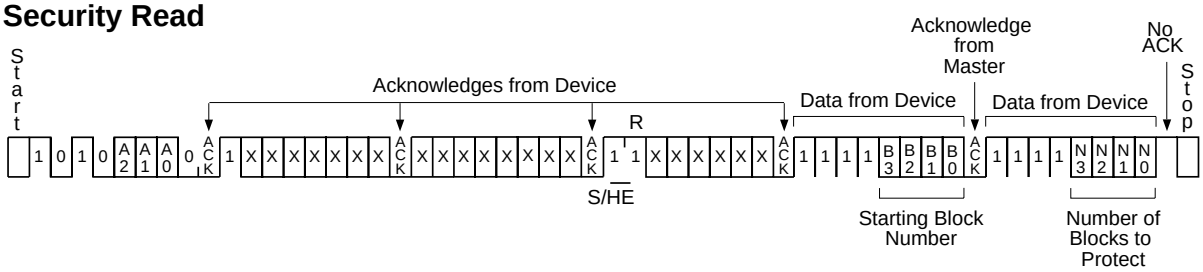
8.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

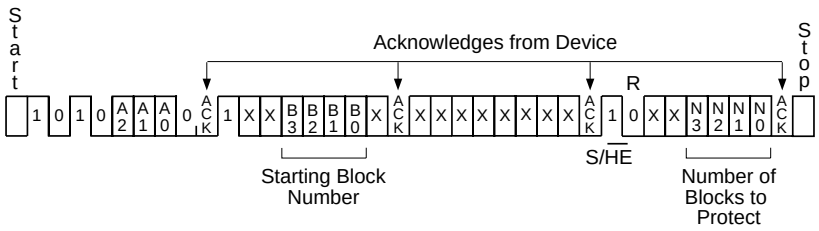
FIGURE 8-1: CONTROL SEQUENCE BIT ASSIGNMENTS



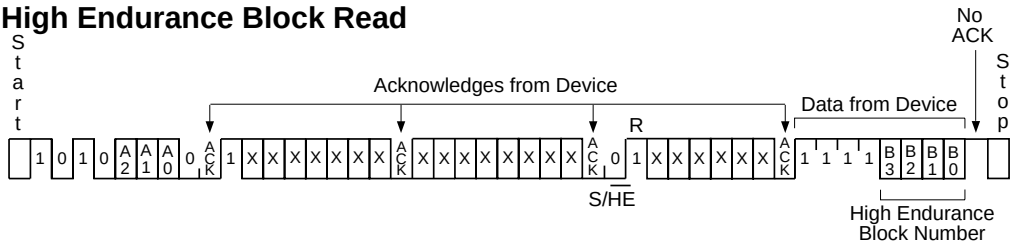
Security Read



Security Write



High Endurance Block Read



High Endurance Block Write

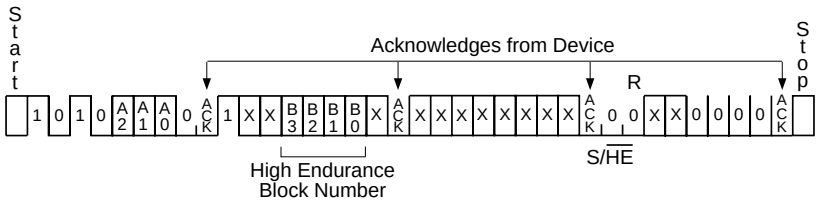


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FIGURE 8-2: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

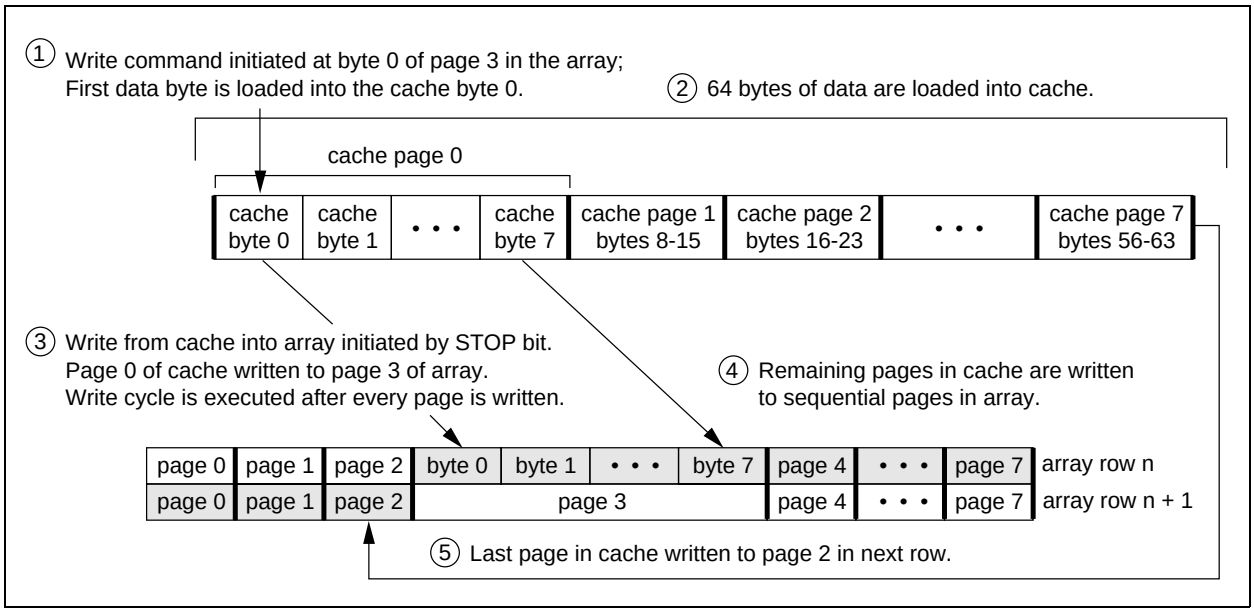
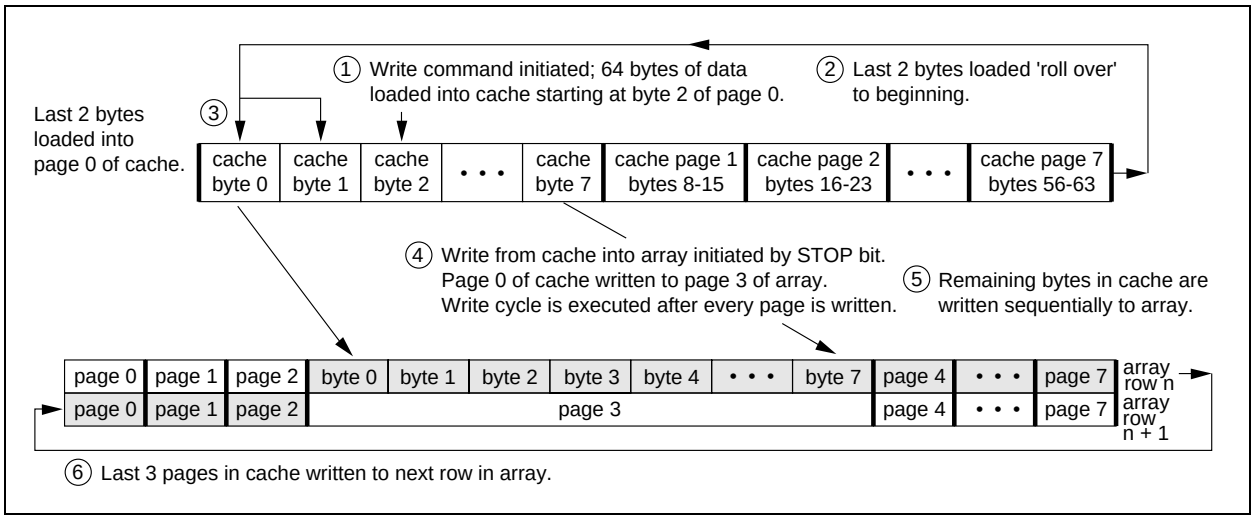


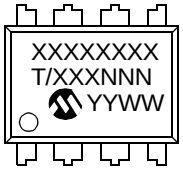
FIGURE 8-3: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



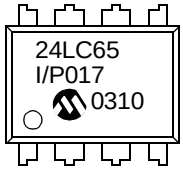
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

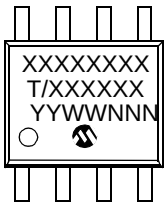
8-Lead PDIP (300 mil)



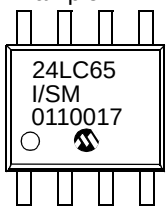
Example:



8-Lead SOIC (208 mil)



Example:



Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	T	Temperature grade (Blank = Commercial, I = Industrial, E = Automotive)

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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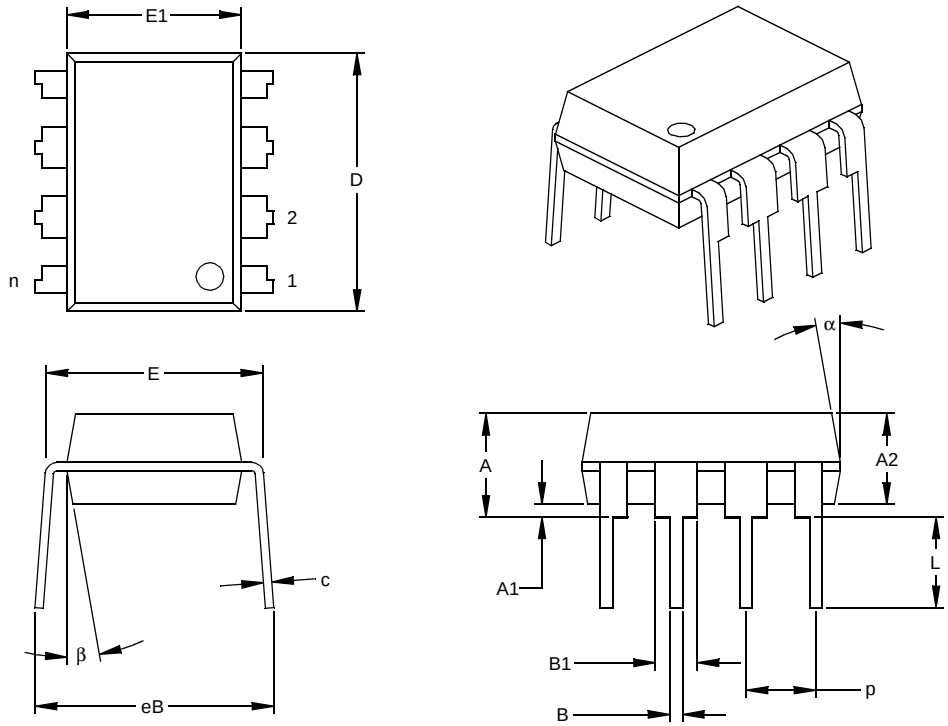
8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

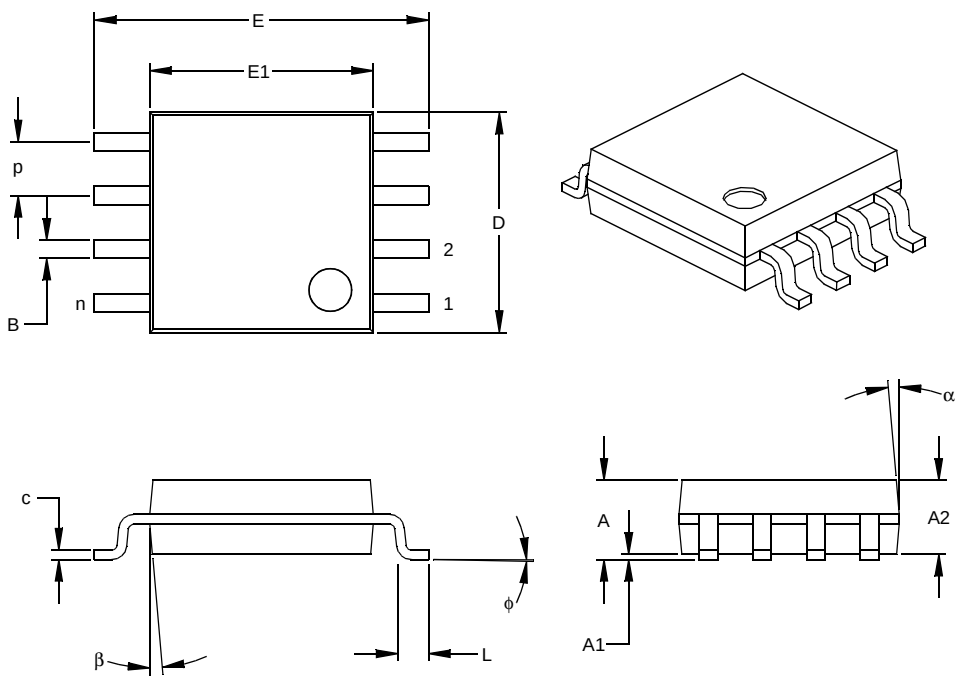


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SM) – Medium, 208 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.070	.075	.080	1.78	1.97	2.03
Molded Package Thickness	A2	.069	.074	.078	1.75	1.88	1.98
Standoff §	A1	.002	.005	.010	0.05	0.13	0.25
Overall Width	E	.300	.313	.325	7.62	7.95	8.26
Molded Package Width	E1	.201	.208	.212	5.11	5.28	5.38
Overall Length	D	.202	.205	.210	5.13	5.21	5.33
Foot Length	L	.020	.025	.030	0.51	0.64	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
Drawing No. C04-056

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APPENDIX A: REVISION HISTORY

Revision J

Corrections to Section 1.0, Electrical Characteristics.

NOTES:

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Device	Temperature Range	Package	Pattern

Device	24AA65 - 64K I^2C 1.8V Serial EEPROM (100 kHz) 24AA65T - 64K I^2C 1.8V Serial EEPROM (100 kHz) 24LC65 - 64K I^2C Serial EEPROM (100 kHz/400 kHz) 24LC65T - 64K I^2C Serial EEPROM (Tape and Reel) 24C65 - 64K I^2C 4.5V Serial EEPROM (400 kHz) 24C65T - 64K I^2C 4.5V Serial EEPROM (Tape and Reel)
Temperature Range	Blank = 0°C to +70°C I = -40°C to +85°C E = -40°C to +125°C
Package	P = Plastic DIP (300 mil Body) SM = Plastic SOIC (207 mil Body, EIAJ standard)

Examples:

a) 24LC65T-I/SM: 64 Kbit Smart Serial, Tape and Reel, 207 mil SOIC package, Industrial temperature, 2.5V

b) 24LC65-I/P: 64 Kbit Smart Serial, Industrial temperature, PDIP package, 2.5V

c) 24AA65T-/SM: 64 Kbit Smart Serial, Tape and Reel, 207 mil SOIC package, Commercial temperature, 1.8V

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