DC273A Quick Start Guide

Description

The LTC2408, an 8 channel **No Latency ΔΣ™** 24-Bit ADC is featured on the DC273A demonstration board. The LTC2408 features 4-ppm linearity, 4-ppm full-scale accuracy, 1-ppm offset accuracy, and 0.3-ppm RMS noise.
The LTC2408 performs interleaved auto-zero and calibration cycles which are transparent to the user. The device does not require initialization or configuration, other than selecting the multiplexer channel. The board includes a precision 2.5V reference (LT1019-2.5), as well as bypassing capacitors, and jumpers to select line frequency rejection and on board /external reference.

On the DC273A demonstration board CSMUX and /CSADC are tied together, as are SLK and CLK. This allows the ADC to be addressed through a minimum of control lines. When the CSMUX and /CSADC are logic High, address data can be clocked into the MUX. When CSMUX and /CSADC are logic low, conversion data can be clocked out of the ADC.

The demonstration board is designed to be incorporated into a target system, as well as give an example of good placement of bypass and partitioning of an analog and digital ground.

The DC273 incorporates 2 jumpers: JP1, which allows the on-board or an external reference, to be selected; and JP2, which allows selection of 50 Hz/60 Hz line frequency rejection.

All the digital control lines are on a 0.070" header (J17).

All the analog inputs are provided with turrets along one edge of the board, positioned to be compatible with clip leads. Two ground connections (J9 & J10) are provided for interconnection into an analog subsystem or to be used as separate returns for two signal groups.

Power and ground are provided on J15 & J16, and reference in and out are provided on J13 & J14. Interconnection of analog and digital subsystems can be made through these ground connections, or all should return to a star ground at a point in the target system. All ground connections should be as short as possible.

Figure 1, DC273A set-up

The multiplexer output is linked to the ADC through a 5 kohm resistor. Both terminals are available, J11 for MUXOUT, and J12 for ADCIN. As the multiplexer output can be disabled, multiplexer expansion can be brought to either of these terminals. Optionally, an amplifier (buffer) can be used to drive ADCIN, without necessarily removing the 5K resistor. If an amplifier with voltage gain is introduced, it is recommended that the resistor be removed. Depending on the source resistance or drive capabilities of nodes driving the multiplexer inputs, J11 can be tied directly to J12. Please see the LTC2400 data sheet for more information on driving the input of the LTC2408
See timing diagram for MUX, and Data Output operation.

F0 is available on J17 for external conversion clock. See full data sheet for use of this line, otherwise, leave open. Use of external clock requires removal of JP2.
The LTC2408's F0 pin is available on J17 for those applications where an external oscillator controls the conversion time of the ADC. Jp2 must be removed in this case. Please consult the LTC2408 data sheet for more information on the use of F0. If an external oscillator is not required, leave pin 1 on J17 open.

Figure 2, MUX timing & output data timing