Dual Matched 1.3GHz Differential Amplifiers/ADC Drivers

FEATURES

- **Matched Gain ±0.1dB**
- **Matched Phase ±0.2° at 100MHz**
- **Channel Separation 80dB at 100MHz**
- 1.3GHz –3dB Bandwidth; Fixed Gain of 10V/V (20dB)
- IMD_3 = –76dBc at 100MHz, $2V_{P-P}$
- Equivalent OIP_3 = 42dBm at 100MHz
- 1nV/√Hz Internal Op Amp Noise
- 6.2dB Noise Figure
- Differential Inputs and Outputs
- Rail-to-Rail Output Swing
- 40mA Supply Current (120mW) per Amplifier
- 1V to 1.6V Output Common Mode Voltage, Adjustable
- DC- or AC-Coupled Operation
- 20-Lead 3mm × 4mm × 0.75mm QFN Package

APPLICATIONS

- Differential ADC Driver
- Differential Driver/Receiver
- Single Ended to Differential Conversion
- IF Sampling (Diversity) Receivers

DESCRIPTION

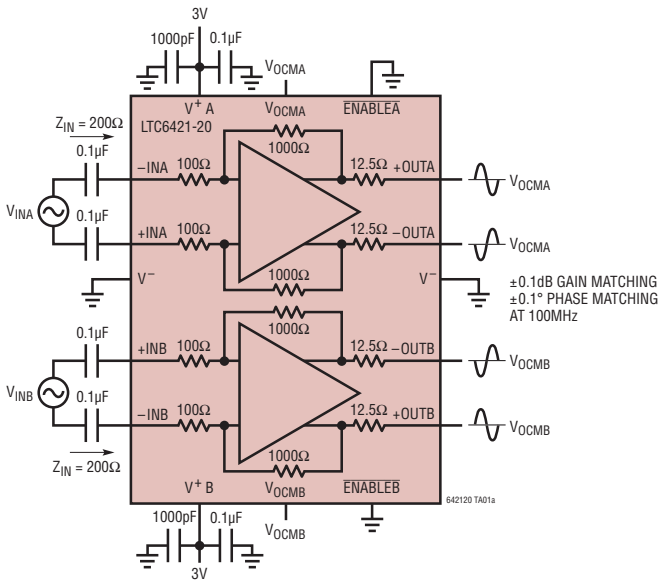
The LTC®6421-20 is a dual high speed differential amplifier targeted at processing signals from DC to 140MHz. The part has been specifically designed to drive 12-, 14- and 16-bit ADCs with low noise and low distortion, but can also be used as a general-purpose broadband gain block.

The LTC6421-20 is easy to use, with minimal support circuitry required. The output common mode voltage is set using an external pin, independent of the inputs, which eliminates the need for transformers or AC-coupling capacitors in many applications. The gain is internally fixed at 20dB (10V/V).

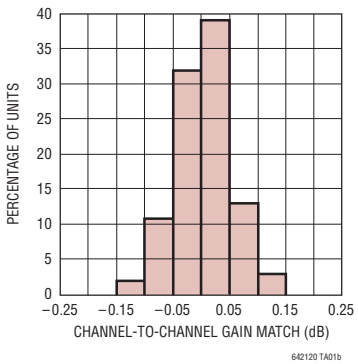
The LTC6421-20 saves space and power compared to alternative solutions using IF gain blocks and transformers. The LTC6421-20 is packaged in a compact 20-lead 3mm × 4mm QFN package and operates over the –40°C to 85°C temperature range.

TYPICAL APPLICATION

Matched Dual Amplifiers with Output Common Mode Biasing



Distribution of Gain Match

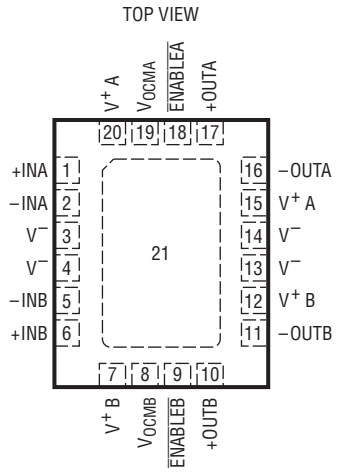


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ($V^+ – V^–$).....3.6V
Input Current (Note 2).....±10mA
Operating Temperature Range (Note 3)....–40°C to 85°C
Specified Temperature Range (Note 4) ....–40°C to 85°C
Storage Temperature Range.....–65°C to 150°C
Maximum Junction Temperature..... 150°C
Output Short-Circuit Duration ..... Indefinite

PIN CONFIGURATION



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 21) IS $V^–$, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6421CUDC-20#PBF	LTC6421CUDC-20#TRPBF	LDDN	20-Lead (3mm × 4mm) Plastic QFN	0°C to 70°C
LTC6421IUDC-20#PBF	LTC6421IUDC-20#TRPBF	LDDN	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

SELECTOR GUIDE

PART NUMBER SINGLE	PART NUMBER DUAL	GAIN (dB)	GAIN (V/V)	Z_{IN} (DIFFERENTIAL) (Ω)	COMMENT
LTC6400-8		8	2.5	400	Lowest Distortion
LTC6400-14		14	5	200	Lowest Distortion
LTC6400-20	LTC6420-20	20	10	200	Lowest Distortion
LTC6400-26		26	20	50	Lowest Distortion
LTC6401-8		8	2.5	400	Lowest Power
LTC6401-14		14	5	200	Lowest Power
LTC6401-20	LTC6421-20	20	10	200	Lowest Power
LTC6401-26		26	20	50	Lowest Power

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, +IN = –IN = V_{OCM} = 1.25V, $\overline{ENABLE}$ = 0V, No R_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input/Output Characteristic							
G_{DIFF}	Gain	V_{IN} = ±100mV Differential	●	19.6	20	20.4	dB
ΔG	Gain Matching	Channel-to-Channel	●		±0.1	±0.25	dB
TC_{GAIN}	Gain Temperature Drift	V_{IN} = ±100mV Differential	●		0.0015		dB/°C
$V_{SWINGMIN}$	Output Swing Low (V_{OCM} = 1.5V)	Each Output, V_{IN} = ±400mV Differential	●		0.1	0.25	V
$V_{SWINGMAX}$	Output Swing High (V_{OCM} = 1.5V)	Each Output, V_{IN} = ±400mV Differential	●	2.75	2.9		V
$V_{OUTDIFFMAX}$	Maximum Differential Output Swing		●	5	5.6		V_{P-P}
I_{OUT}	Output Current Drive	$2V_{P-P, OUT}$ (Note 10)	●	10			mA
V_{OS}	Input Offset Voltage	Differential	●	–2	±0.4	2	mV
TCV_{OS}	Input Offset Voltage Drift	Differential	●		1.4		µV/°C
I_{VRMIN}	Input Common Mode Voltage Range, MIN		●			1	V
I_{VRMAX}	Input Common Mode Voltage Range, MAX		●	1.6			V
R_{INDIFF}	Input Resistance (+IN, –IN)	Differential	●	170	200	230	Ω
ΔR_{IN}	Input Impedance Matching	Channel-to-Channel	●		±1	±2.5	%
C_{INDIFF}	Input Capacitance (+IN, –IN)	Differential, Includes Parasitic			1		pF
$R_{OUTDIFF}$	Output Resistance (+OUT, –OUT)	Differential	●	20	25	36	Ω
CMRR	Common Mode Rejection Ratio	Input Common Mode Voltage 1V to 1.6V	●	45	68		dB
Output Common Mode Voltage Control							
G_{CM}	Common Mode Gain	V_{OCM} = 1V to 1.6V			1		V/V
V_{OCMMIN}	Output Common Mode Range, MIN		●			1	V
V_{OCMMAX}	Output Common Mode Range, MAX		●	1.6			V
V_{OSCM}	Common Mode Offset Voltage	V_{OCM} = 1.25V to 1.5V	●	–10	±2	10	mV
TCV_{OSCM}	Common Mode Offset Voltage Drift		●		6		µV/°C
IV_{OCM}	V_{OCM} Input Current		●	–15	–3	0	µA
$\overline{ENABLE}$x Pins (x = A, B)							
V_{IL}	$\overline{ENABLE}$x Input Low Voltage		●			0.8	V
V_{IH}	$\overline{ENABLE}$x Input High Voltage		●	2.4			V
	$\overline{ENABLE}$x Input Current	ENABLEx ≤ 0.8V ENABLEx ≥ 2.4V	● ●		 1.5	±0.5 3	µA µA
Power Supply							
V_S	Operating Supply Range		●	2.85	3	3.5	V
I_S	Supply Current	$\overline{ENABLE}$x ≤ 0.8V; per Amplifier	●		40	50	mA
I_{SHDN}	Shutdown Supply Current	$\overline{ENABLE}$x ≥ 2.4V; per Amplifier, Inputs Floating	●		1	3	mA
PSRR	Power Supply Rejection Ratio (Differential Outputs)	V^+ = 2.85V to 3.5V	●	55	86		dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{OCM} = 1.25V, $\overline{ENABLE}$ = 0V, No R_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔG	Gain Matching	f = 100MHz (Note 9)	●		±0.1	±0.25	dB
ΔP	Phase Matching	f = 100MHz			±0.2		deg
	Channel Separation (Note 8)	f = 100MHz			80		dB
–3dBBW	–3dB Bandwidth	200mV$_{P-P, OUT}$ (Note 6)			1.3		GHz
0.5dBBW	Bandwidth for 0.5dB Flatness	200mV$_{P-P, OUT}$ (Note 6)			250		MHz
0.1dBBW	Bandwidth for 0.1dB Flatness	200mV$_{P-P, OUT}$ (Note 6)			130		MHz
NF	Noise Figure	R_L = 375Ω (Note 5), f = 100MHz			6.2		dB
e_{IN}	Input Referred Voltage Noise Density	Includes Resistors (Short Inputs), f = 100MHz			2.2		nV/√Hz
e_{ON}	Output Referred Voltage Noise Density	Includes Resistors (Short Inputs), f = 100MHz			22		nV/√Hz
1/f	1/f Noise Corner				12.5		kHz
SR	Slew Rate	Differential (Note 6)			4500		V/µs
$t_{S1\%}$	1% Settling Time	2V$_{P-P, OUT}$ (Note 6)			2		ns
t_{OVDR}	Overdrive Recovery Time	1.9V$_{P-P, OUT}$ (Note 6) Single Ended			7		ns
P_{1dB}	1dB Compression Point	R_L = 375Ω (Notes 5, 7), f = 100MHz			18		dBm
t_{ON}	Turn-On Time	+OUT, –OUT Within 10% of Final Values			80		ns
t_{OFF}	Turn-Off Time	I_{CC} Falls to 10% of Nominal			150		ns
–3dBBW$_{VOCM}$	V_{OCM} Pin Small Signal –3dB BW	0.1V$_{P-P}$ at V_{OCM}, Measured Single-Ended at Output (Note 6)			15		MHz
IMD_3	3rd Order Intermodulation Distortion	f = 100MHz (1MHz Spacing), V_{OUT} = 2V$_{P-P}$ Composite			–76		dBc
OIP_3	3rd Order Output Intercept	f = 100MHz (Note 7)			42		dBc
IIP_3	3rd Order Input Intercept	f = 100MHz (Z_{IN} = 50Ω) f = 100MHz (Z_{IN} = 200Ω)			22 16		dBc dBc
HD_2	2nd Order Harmonic Distortion	f = 100MHz, V_{OUT} = 2V$_{P-P}$			–74		dBc
HD_3	3rd Order Harmonic Distortion	f = 100MHz, V_{OUT} = 2V$_{P-P}$			–78		dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input pins (+IN, –IN) are protected by steering diodes to either supply. If the inputs go beyond either supply rail, the input current should be limited to less than 10mA.

Note 3: The LTC6421C and LTC6421I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 4: The LTC6421C is guaranteed to meet specified performance from 0°C to 70°C. It is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6421I is guaranteed to meet specified performance from –40°C to 85°C.

Note 5: Input and output baluns used. See Test Circuit A.

Note 6: Measured using Test Circuit B. R_L = 87.5Ω on each output.

Note 7: Since the LTC6421-20 is a feedback amplifier with low output impedance, a resistive load is not required when driving an AD converter. Therefore, typical output power is very small. In order to compare the LTC6421-20 with amplifiers that require 50Ω output load, the output voltage swing driving a given R_L is converted to OIP_3 and P_{1dB} as if it were driving a 50Ω load. Using this modified convention, 2V$_{P-P}$ is by definition equal to 10dBm, regardless of actual R_L.

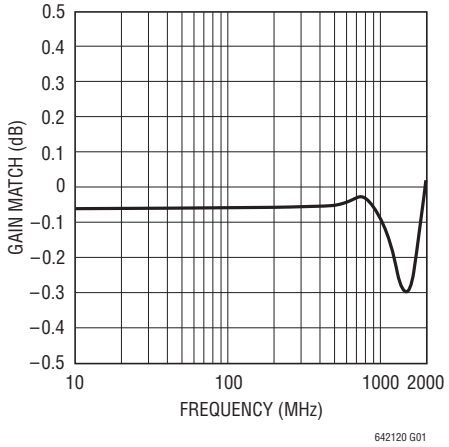
Note 8: Channel separation (the inverse of crosstalk) is measured by driving a signal into one input, while terminating the other input. Channel separation is the ratio of the resulting output signal at the driven channel to the channel that is not driven.

Note 9: Not production tested. Guaranteed by design and by correlation to production tested parameters.

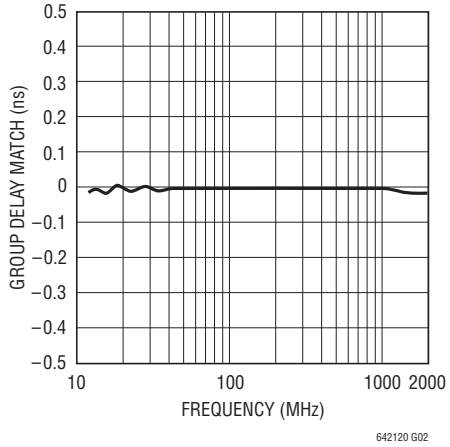
Note 10: The output swing range is at least 2V$_{P-P}$ differential even when sourcing or sinking 20mA. Tested at V_{OCM} = 1.5V.

TYPICAL PERFORMANCE CHARACTERISTICS

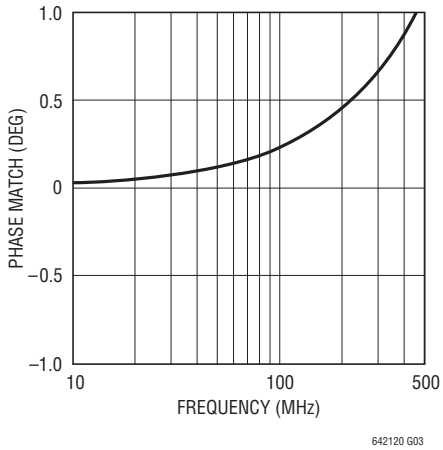
Channel-to-Channel Gain Match vs Frequency



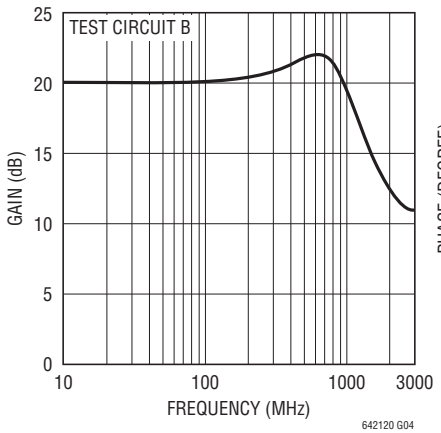
Channel-to-Channel Group Delay Match vs Frequency



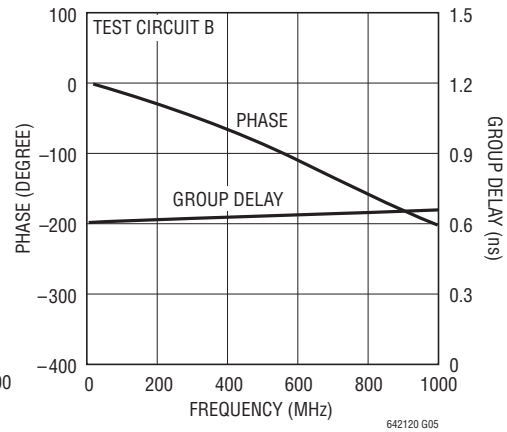
Channel-to-Channel Phase Match vs Frequency



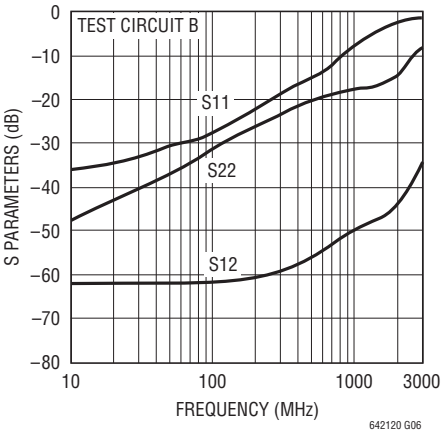
Frequency Response



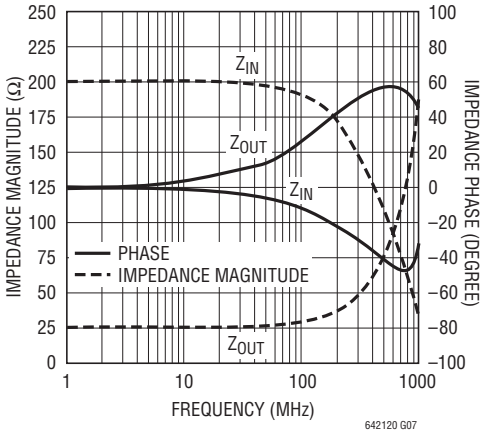
S21 Phase and Group Delay vs Frequency



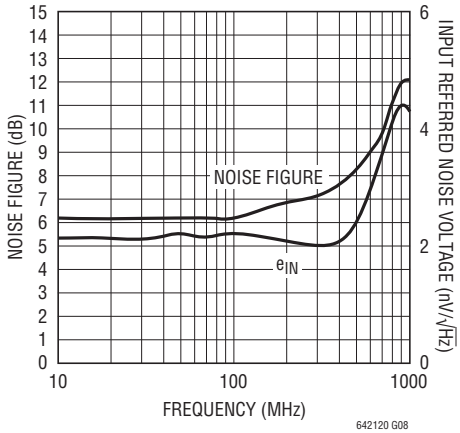
Input and Output Reflection and Reverse Isolation vs Frequency



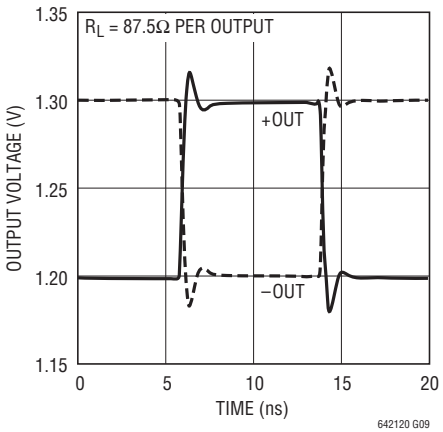
Input and Output Impedance vs Frequency



Noise Figure and Input Referred Noise Voltage vs Frequency

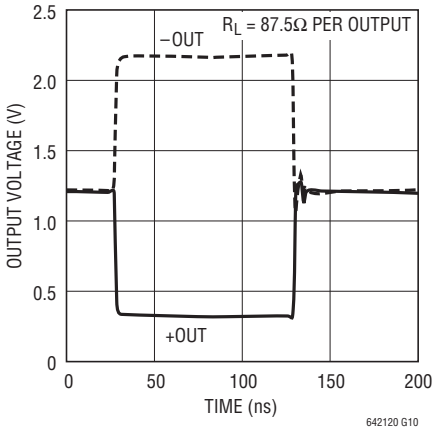


Small-Signal Transient Response

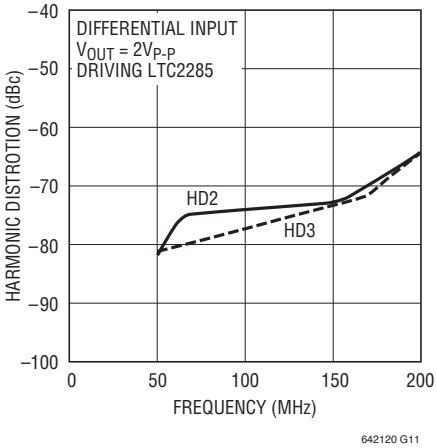


TYPICAL PERFORMANCE CHARACTERISTICS

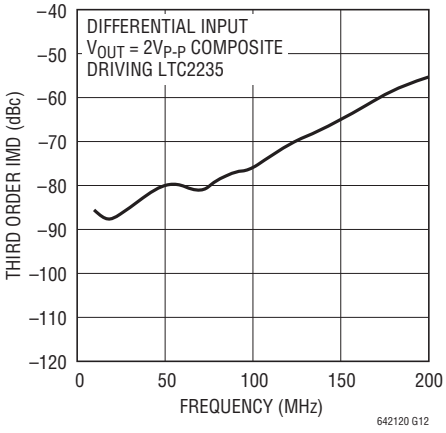
Overdrive Transient Response



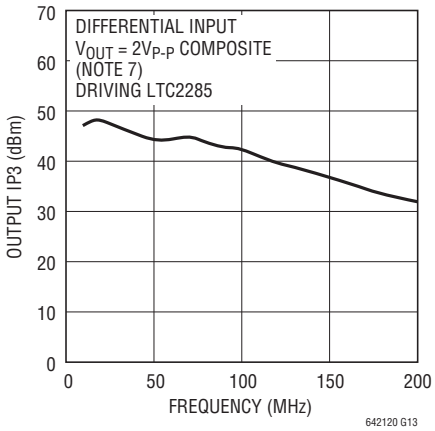
Harmonic Distortion vs Frequency



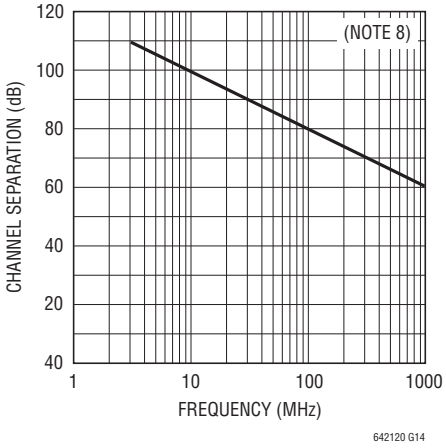
Third Order Intermodulation Distortion vs Frequency



Equivalent Output Third Order Intercept vs Frequency



Channel Separation vs Frequency



PIN FUNCTIONS

+INA, –INA, –INB, +INB (Pins 1, 2, 5, 6): Differential Inputs of A and B channel respectively.

V^- (Pins 3, 4, 13, 14, 21): Negative Power Supply. All four pins, as well as the exposed back, must be connected to same voltage/ground.

$\overline{ENABLEA}$, $\overline{ENABLEB}$ (Pins 9, 18): Logic inputs. If low, the amplifier is enabled. If high, the amplifier is disabled and placed in a low-power shutdown mode, making the amplifier outputs high impedance. These pins are internally separate. These pins should not be left floating.

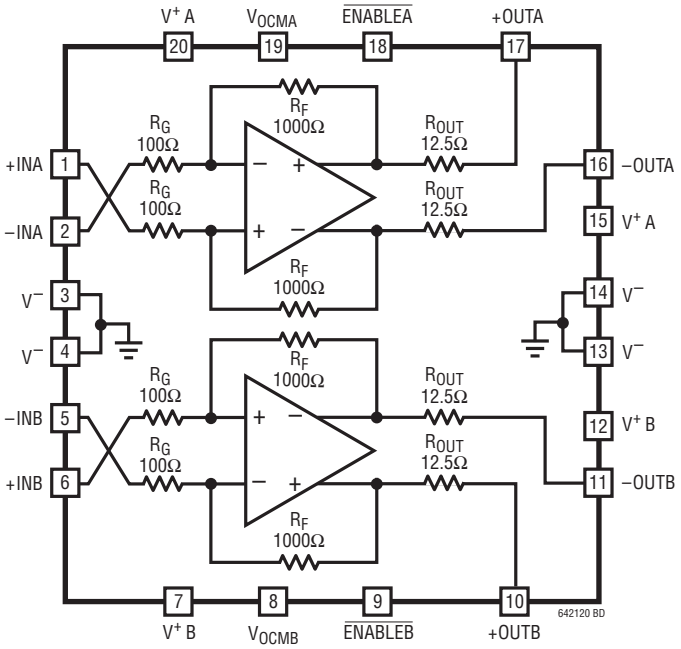
V^+A , V^+B (Pins 15, 20, 7, 12): Positive Power Supply (Normally tied to 3V or 3.3V). Supply pins of A and B channels are internally separate. Bypass each pin with 1000pF and 0.1µF capacitors as close to the pins as possible.

–OUTA, +OUTA, –OUTB, +OUTB (Pins 16, 17, 11, 10): Differential Outputs of channels A and B respectively.

V_{OCMA}, V_{OCMB} (Pins 19, 8): These pins set the output common mode voltage for the respective channel. They are internally separate. A 0.1µF external bypass capacitor is recommended.

Exposed Pad (Pin 21): V^-. The Exposed Pad must be connected to same voltage/ground as pins 3, 4, 13, 14.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Circuit Operation

Each of the two channels of the LTC6421-20 is composed of a fully differential amplifier with on chip feedback and output common mode voltage control circuitry. Differential gain and input impedance are set by 100Ω/1000Ω resistors in the feedback network. Small output resistors of 12.5Ω improve the circuit stability over various load conditions.

The LTC6421-20 is very flexible in terms of I/O coupling. It can be AC- or DC-coupled at the inputs, the outputs or both. If the inputs are AC-coupled, the input common mode voltage is automatically biased close to V_{OCM} and thus no external circuitry is needed for bias. The LTC6421-20 provides an output common mode voltage set by V_{OCM}, which allows driving an ADC directly without external components such as a transformer or AC coupling capacitors. The input signal can be either single-ended or differential with only minor differences in distortion performance.

Input Impedance and Matching

The differential input impedance of the LTC6421-20 is 200Ω. If a 200Ω source impedance is unavailable, then the differential inputs may need to be terminated to a lower value impedance, e.g. 50Ω, in order to provide an impedance match for the source. Several choices are available. One approach is to use a differential shunt resistor (Figure 1). Another approach is to employ a wide band transformer (Figure 2). Both methods provide a wide band impedance match. The termination resistor or the transformer must be placed close to the input pins in order to minimize the reflection due to input mismatch. Alternatively, one could apply a narrowband impedance match at the inputs of the LTC6421-20 for frequency selection and/or noise reduction.

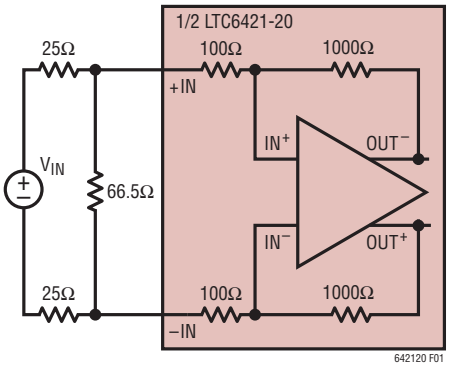


Figure 1. Input Termination for Differential 50Ω Input Impedance Using Shunt Resistor

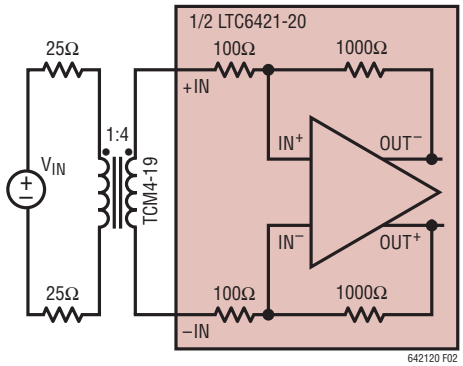


Figure 2. Input Termination for Differential 50Ω Input Impedance Using a 1:4 Balun

APPLICATIONS INFORMATION

Referring to Figure 3, LTC6421-20 can be easily configured for single-ended input and differential output without a balun. The signal is fed to one of the inputs through a matching network while the other input is connected to the same matching network and a source resistor. Because the return ratios of the two feedback paths are equal, the two outputs have the same gain and thus symmetrical swing. In general, the single-ended input impedance and termination resistor R_T are determined by the combination of R_S, R_G and R_F. For example, when R_S is 50Ω, it is found that the single-ended input impedance is 202Ω and R_T is 66.5Ω in order to match to a 50Ω source impedance.

The LTC6421-20 is unconditionally stable. However, the overall differential gain is affected by both source impedance and load impedance as follows:

$$A_V = \left|\frac{V_{OUT}}{V_{IN}}\right| = \frac{2000}{R_S + 200} \bullet \frac{R_L}{25 + R_L}$$

Output Impedance Match

The LTC6421-20 can drive an ADC directly without external output impedance matching. Alternatively, the differential output impedance of 25Ω can be matched to a higher value impedance, e.g. 50Ω, by series resistors or an LC network.

Output Common Mode Adjustment

The output common mode voltage is set by the V_{OCM} pin, which is a high impedance input. The output common mode voltage is capable of tracking V_{OCM} in a range from 1V to 1.6V. The bandwidth of V_{OCM} control is typically 15MHz, which is dominated by a low pass filter connected to the V_{OCM} pin and is aimed to reduce common mode noise generation at the outputs. The internal common mode feedback loop has a –3dB bandwidth of 300MHz, allowing fast rejection of any common mode output voltage disturbance. The V_{OCM} pin should be tied to a DC bias

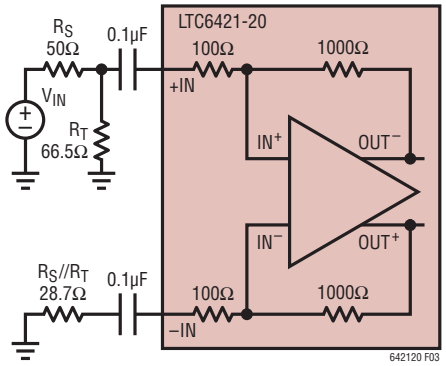


Figure 3. Input Termination for Single-Ended 50Ω Input Impedance

APPLICATIONS INFORMATION

voltage with a 0.1µF bypass capacitor. When interfacing with A/D converters such as the LTC22xx families, the V_{OCM} pin can be connected to the V_{CM} pin of the ADC.

Driving A/D Converters

The LTC6421-20 has been specifically designed to interface directly with high speed A/D converters. The back page of this data sheet shows the LTC6421-20 driving an LTC2285, which is a dual 14-bit, 125Msps ADC.

The V_{OCM} pins of the LTC6421-20 are connected to the V_{CM} pins of the LTC2285, which provide a DC voltage level of 1.5V. Both ICs are powered from the same 3V supply voltage.

The inputs to the LTC6421-20 can be configured in various ways, as described in the Input Impedance and Matching section of this datasheet. The outputs of the LTC6421-20 may be connected directly to the analog inputs of an ADC, or a simple lowpass or bandpass filter network may be inserted to reduce out-of-band noise.

Test Circuits

Due to the fully-differential design of the LTC6421 and its usefulness in applications with differing characteristic specifications, two test circuits are used to generate the information in this datasheet. Test Circuit A is DC1299, a two-port demonstration circuit for the LTC6420/LTC6421 family. The schematic and silkscreen are shown in Figure 4. This circuit includes input and output transformers (baluns) for single-ended-to-differential conversion and impedance transformation, allowing direct hook-up to a 2-port network analyzer. There are also series resistors at the output to avoid loading the amplifier directly with a 50Ω load. Due to the input and output transformers, the –3dB bandwidth is reduced from 1.3GHz to approximately 1.1GHz.

Test Circuit B uses a 4-port network analyzer to measure S-parameters and gain/phase response. This removes the effects of the wideband baluns and associated circuitry, for a true picture of the >1GHz S-parameters and AC characteristics.

APPLICATIONS INFORMATION

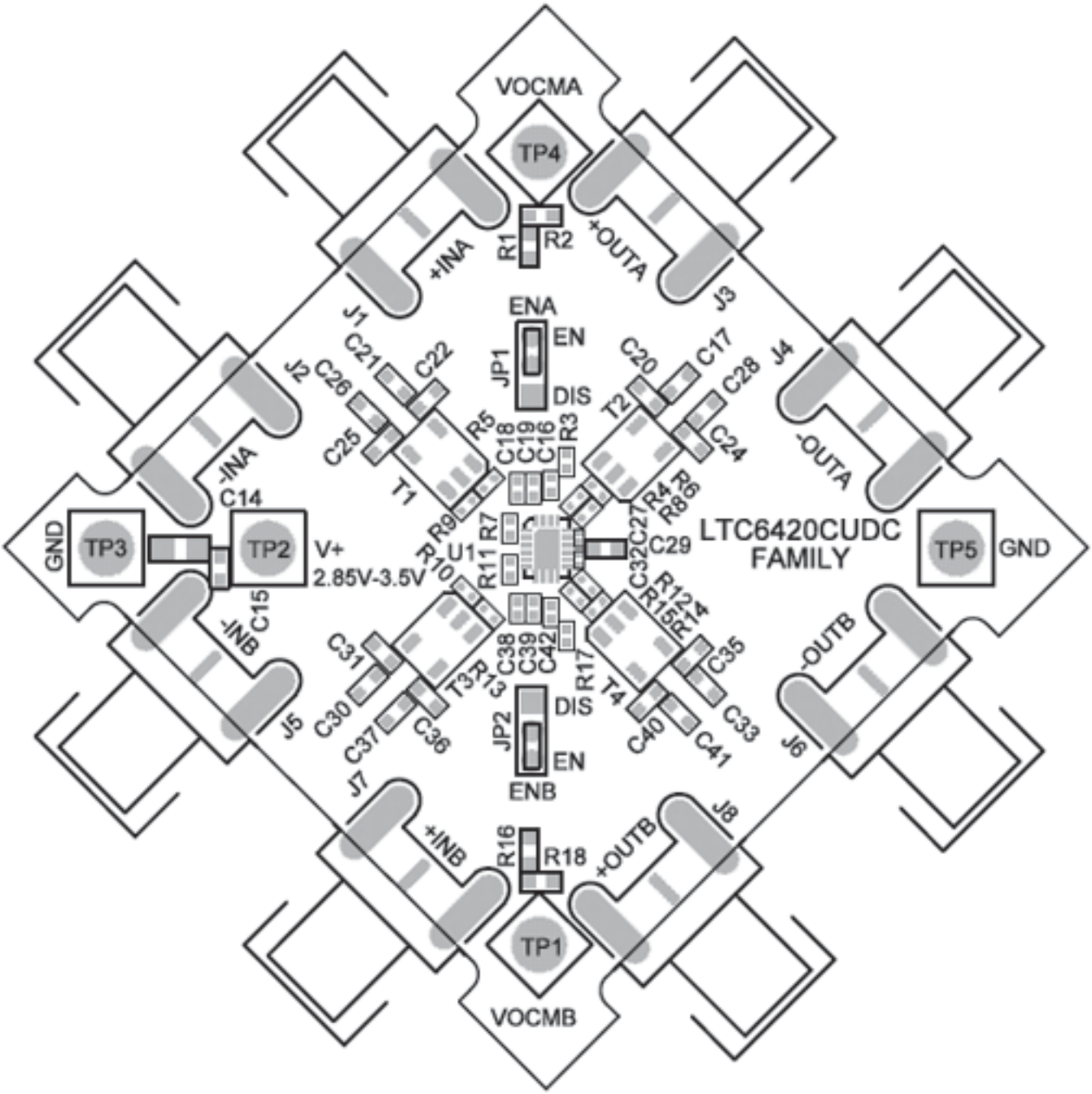


Figure 4a. Top Silkscreen of DC1299 (Test Circuit A)

APPLICATIONS INFORMATION

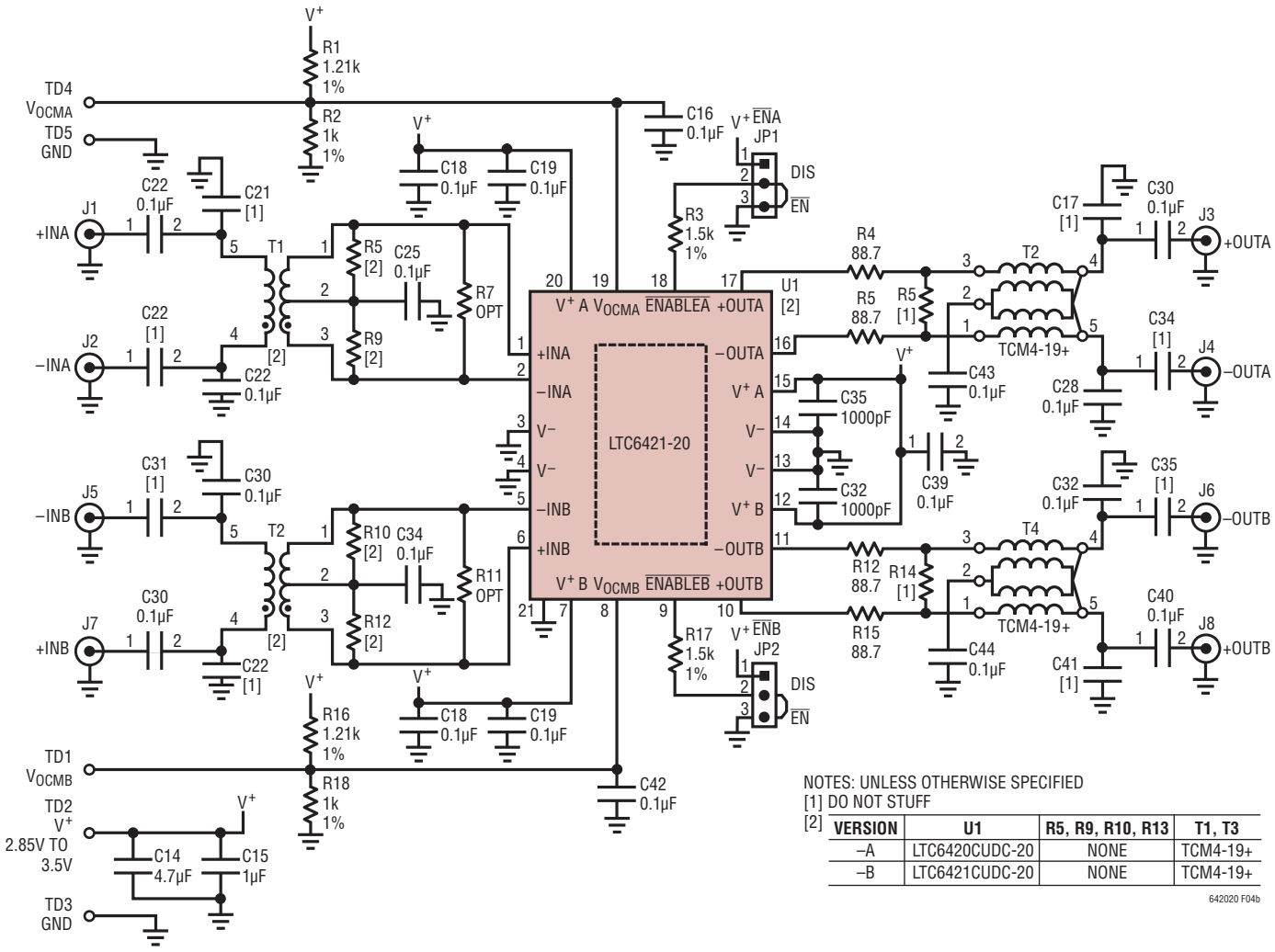
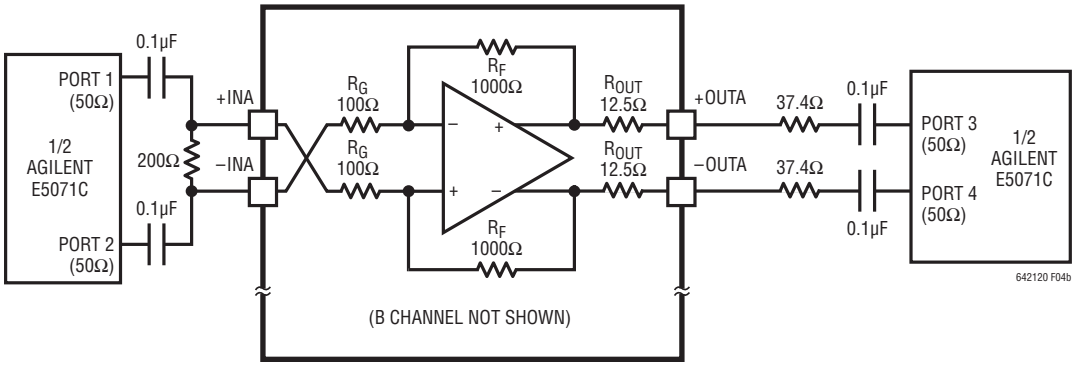


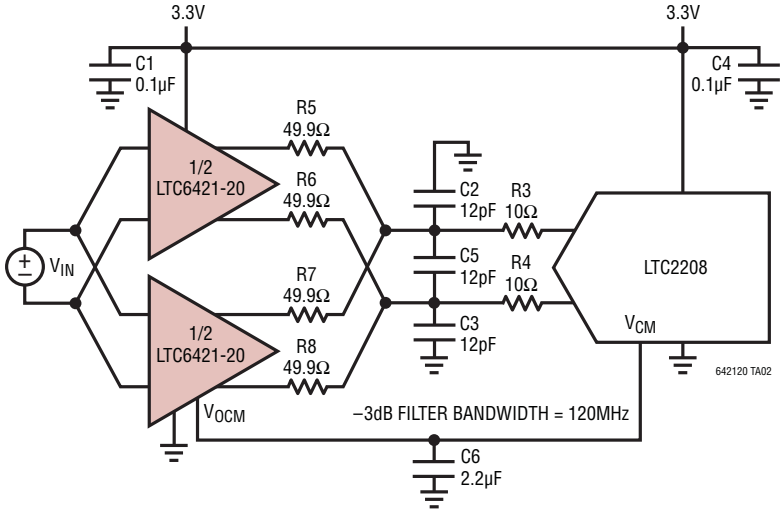
Figure 4b. Demo Circuit 1299 Schematic (Test Circuit A)

TYPICAL APPLICATIONS

Test Circuit B, 4-Port Measurements
(Only the Signal-Path Connections Are Shown)

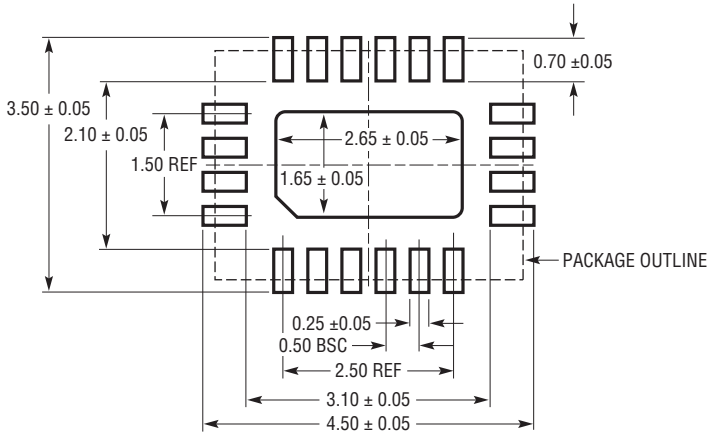


Parallel ADC Drivers to Reduce Wideband Noise

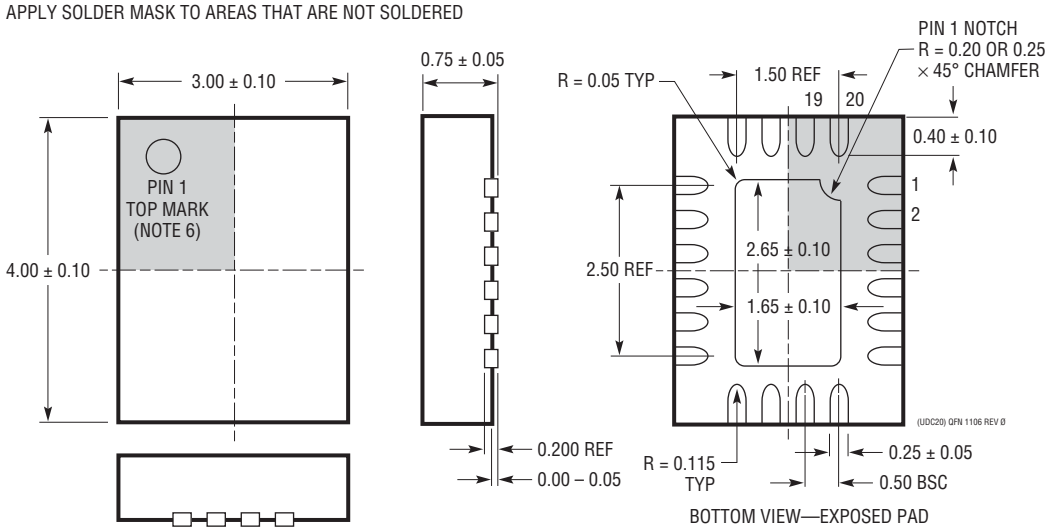


PACKAGE DESCRIPTION

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

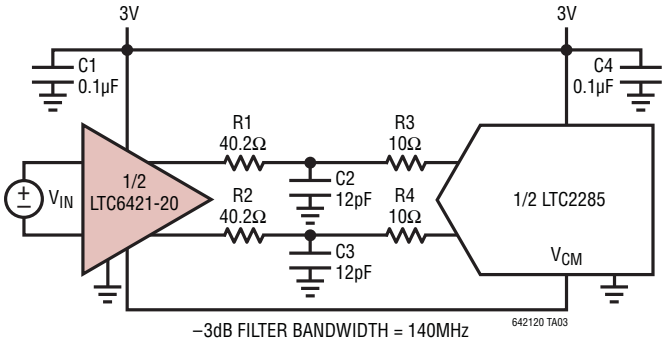


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Dual ADC Driver for Wideband Direct-Conversion Receivers



–3dB FILTER BANDWIDTH = 140MHz

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
High-Speed Differential Amplifiers/Differential Op Amps		
LT®1993-2	800MHz Differential Amplifier/ADC Driver	A_V = 2V/V, OIP3 = 38dBm at 70MHz
LT1993-4	900MHz Differential Amplifier/ADC Driver	A_V = 4V/V, OIP3 = 40dBm at 70MHz
LT1993-10	700MHz Differential Amplifier/ADC Driver	A_V = 10V/V, OIP3 = 40dBm at 70MHz
LT1994	Low Noise, Low Distortion Differential Op Amp	16-Bit SNR and SFDR at 1MHz, Rail-to-Rail Outputs
LT5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 47dBm at 100MHz, Gain Control Range 10.5dB to 33dB
LT5524	Low Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	OIP3 = 40dBm at 100MHz, Gain Control Range 4.5dB to 37dB
LTC6400-14/ LTC6400-20/ LTC6400-26	Low Noise, Low Distortion, Differential ADC Drivers	A_V = 14dB/20dB/26dB, Single Amplifier per IC, High Performance
LTC6401-8/ LTC6401-14/ LTC6401-20/ LTC6401-26	Low Noise, Low Distortion, Differential ADC Drivers	A_V = 8dB/14dB/20dB/26dB, Single Amplifier per IC, Low Power
LTC6402-6	300MHz Differential Amplifier/ADC Driver	A_V = 6dB, Distortion < –80dBc at 25MHz
LTC6402-12	300MHz Differential Amplifier/ADC Driver	A_V = 12dB, Distortion < –80dBc at 25MHz
LTC6402-20	300MHz Differential Amplifier/ADC Driver	A_V = 20dB, Distortion < –80dBc at 25MHz
LTC6404-1	600MHz, Low Noise, AC Precision, Fully Differential Input/Output Amplifier/Driver	A_V = Unity Gain, e_n = 1.5nV/Hz, Distortion < –90dBc at 10MHz
LTC6404-2	900MHz, Low Noise, AC Precision, Fully Differential Input/Output Amplifier/Driver	A_V = 2V/V, e_n = 1.5nV/Hz, Distortion < –95dBc at 10MHz
LTC6404-4	1800MHz, Low Noise, AC Precision, Fully Differential Input/Output Amplifier/Driver	A_V = 4V/V, e_n = 1.5nV/Hz, Distortion < –98dBc at 10MHz
LTC6406	3GHz Rail-to-Rail Input Differential Op Amp	1.6nV/$\sqrt{Hz}$ Noise, –72dBc Distortion at 50MHz, 18mA
LT6411	Low Power Differential ADC Driver/Dual Selectable Gain Amplifier	16mA Supply Current, IMD3 = –83dBc at 70MHz, A_V = 1, –1 or 2

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