

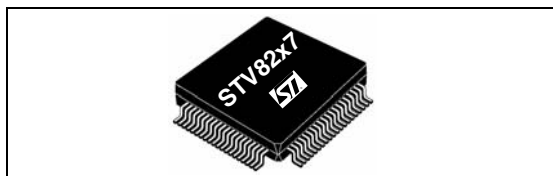


# STV8247, STV8257, STV8277, STV8287

Digital audio decoder/processors  
for A2 and NICAM television/video recorders

## Features

- Full-automatic multi-standard demodulation
  - B / G / I / L / M / N / D / K standards
  - Mono AM and FM
  - FM 2-carrier (German and Korean Zweiton) and NICAM
- Multi-channel capability
  - 3 I<sup>2</sup>S digital inputs, S/PDIF (pass-thru/out)
  - 1 I<sup>2</sup>S digital output (shared with one of the I<sup>2</sup>S digital inputs)
  - 5.1 analog outputs
  - Dolby<sup>®</sup> Pro Logic<sup>®</sup> and Dolby<sup>®</sup> Pro Logic II<sup>®</sup>
- Sound processing: Loudspeaker
  - ST royalty-free processing: ST WideSurround<sup>™</sup>, ST OmniSurround<sup>™</sup> (Virtual Dolby<sup>®</sup>, Surround and Virtual Dolby<sup>®</sup>, Digital compliant) and ST Dynamic Bass<sup>™</sup>
  - SRS<sup>®</sup>, WOW<sup>™</sup>, SRS<sup>®</sup>, TruSurround XT<sup>™</sup> (Virtual Dolby<sup>®</sup>, Surround and Virtual Dolby<sup>®</sup>, Digital compliant)
  - Independent volume/balance
  - SVC (smart volume control), 5-band equalizer and loudness
- Sound processing: Headphone
  - SVC (smart volume control), bass-treble, loudness and SRS<sup>®</sup>, TruBass<sup>™</sup>
  - Independent volume/balance
- Analog audio matrix
  - 4 stereo inputs and 3 stereo outputs
  - THRU mode
  - 2 V<sub>RMS</sub> capability
- Audio delay for audio video synchronization
  - Embedded stereo delay up to 90 ms when processing at 32KHz (demodulator input mode) and up to 60 ms when processing at 48KHz (SCART only input mode)
  - Independent delay on headphone and loudspeaker channels



## Description

The STV82x7 family, based on audio DSPs (digital signal processors), performs high quality and advanced dedicated digital audio processing. The STV82x7 devices provide all of the necessary resources for automatic detection and demodulation of analog audio transmissions for European and Asian terrestrial TV broadcasts.

Virtual or true, multi-channel capabilities and easy digital links make them ideal for digital audio low cost consumer applications. Starting from enhanced stereo up to independent control of 5 loudspeakers and a subwoofer (5.1 channels), the STV82x7 family offers standard and advanced features plus sound enhancements, spatial and virtual effects to enhance television viewer comfort and entertainment.

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# 1 General description

The STV82x7 is a multi-standard TV sound demodulator and audio processor which integrates SRS<sup>®</sup>, WOW<sup>™</sup>, SRS<sup>®</sup>, TruSurround XT<sup>™</sup>, Dolby<sup>®</sup>, Pro Logic<sup>®</sup>, Dolby<sup>®</sup>, Pro Logic II<sup>®</sup>, Virtual Dolby<sup>®</sup>, Surround (VDS) and Virtual Dolby<sup>®</sup>, Digital (VDD) capability.

ST advanced algorithms such as ST OmniSurround<sup>™</sup>, ST WideSurround<sup>™</sup>, ST Dynamic Bass<sup>™</sup> are also available in this audio sound processor. ST OmniSurround<sup>™</sup> is a certified Dolby<sup>®</sup>, algorithm for the Virtual Dolby<sup>®</sup>, Digital (VDD) and the Virtual Dolby<sup>®</sup>, Surround (VDS). When using VDD or VDS, either a Dolby<sup>®</sup>, Digital or a Pro Logic<sup>®</sup>, (or Pro Logic II<sup>®</sup>) decoder is mandatory respectively.

This chip performs automatic multi-standard analog TV stereo sound identification and demodulation (no specific I<sup>2</sup>C programming is required). It offers various audio processing functions such as equalization, loudness, beeper, volume, balance, and surround effects. It provides a cost-effective solution for analog and digital TV designs.

The STV82x7 is perfectly suited to current and future digital TV platforms, based on audio/video digital chips (STD2000, DTV100 platform) which include an internal digital decoder (MPEG, Dolby<sup>®</sup>, Digital...). In the case where a Dolby<sup>®</sup>, Digital decoder is embedded in the audio/video digital chip, Virtual Dolby<sup>®</sup>, Digital can be obtained.

For the CTV100/120 platforms, this device is offered as an alternative solution to the first-generation chassis that uses the STV82x6

**Table 1. STV82x7 version list**

	STV8247		STV8257			STV8277		STV8287
	S T V 8 2 4 7 D D	S T V 8 2 4 7 D S X	S T V 8 2 5 7 D	S T V 8 2 5 7 D S X	S T V 8 2 5 7 S X	S T V 8 2 7 7 D S X	S T V 8 2 7 7 D S X	S T V 8 2 8 7 D
<b>Demodulation</b>								
FM 2 Carrier and NICAM	X	X	X	X	X	X	X	X
<b>Multi-channel capabilities</b>								
Analog loudspeakers output number	2.1	2.1	2.1	2.1	2.1	5.1	5.1	5.1
I <sup>2</sup> S In ( <i>exclusive</i> with I <sup>2</sup> S Out)	1	1	3	3	3	3	3	3
S/PDIF (pass-thru or output)	1	1	1	1	1	1	1	1
Virtual Dolby, Surround	X	X	X	X		X	X	VDS PLII
Virtual Dolby <sup>®</sup> , Digital capability <sup>(1)</sup>			X	X	X	X	X	X

Table 1. STV82x7 version list (continued)

	STV8247		STV8257			STV8277		STV8287
	S T V 8 2 4 7 D	S T V 8 2 4 7 D S X	S T V 8 2 5 7 D	S T V 8 2 5 7 D S X	S T V 8 2 5 7 S X	S T V 8 2 7 7 D	S T V 8 2 7 7 D S X	S T V 8 2 8 7 D
Dolby <sup>®</sup> , Pro Logic <sup>®</sup> , (DPLI) or Dolby <sup>®</sup> , Pro Logic II <sup>®</sup> , (DPLII)	DPLI (internal)	DPLI (internal)	DPLI (internal)	DPLI (internal)		DPLI	DPLI	DPLII
<b>Audio processing</b>								
SRS <sup>®</sup> , WOW <sup>™</sup> (WOW)								
SRS <sup>®</sup> , TruSurround XT <sup>™</sup>		X		X	X		X	
ST Voice <sup>™</sup> , ST Dynamic Bass <sup>™</sup>	X	X	X	X	X	X	X	X
ST WideSurround <sup>™</sup> , ST OmniSurround <sup>™</sup> (2)	X	X	X	X	X	X	X	X

1. Dolby<sup>®</sup>, Digital Bypass capability or Virtual Dolby<sup>®</sup>, Digital are obtained with the use of an external Dolby<sup>®</sup>, Digital decoder (for example STD2000).
2. When using Virtual Dolby<sup>®</sup>, Digital or Virtual Dolby<sup>®</sup>, Surround with ST OmniSurround<sup>™</sup> or SRS, TruSurround XT<sup>™</sup> a Dolby<sup>®</sup>, Digital or a Pro Logic<sup>®</sup>, (or Pro LogicII<sup>®</sup>) decoder is mandatory.

## 1.1 STV82x7 overview

### 1.1.1 Core features

- Single audio source processing:
  - IF source and/or analog stereo input (SCART)
  - one digital source with a maximum of 6 synchronous channels (5.1 is obtained across three I<sup>2</sup>S)
- SIF input signal with AGC (automatic gain control)
- Digital demodulator with automatic standard detection and demodulation for AM, FM mono, FM 2 carriers (German or Korean FM 2-carrier) and NICAM
- Audio processor working at 32 kHz, 44.1 kHz or 48 kHz with specific features:
  - For loudspeakers (L, R, L<sub>S</sub>, R<sub>S</sub>, SubW, C):
    - Dolby<sup>®</sup> Pro Logic II<sup>®</sup> Decoder with bass management
    - SRS<sup>®</sup> WOW<sup>™</sup> or TruSurround XT<sup>™</sup> including Virtual Dolby<sup>®</sup> Surround and Virtual Dolby<sup>®</sup> Digital
    - ST WideSurround<sup>™</sup>
    - ST OmniSurround<sup>™</sup>
    - ST Dynamic Bass<sup>™</sup>
    - 5-band equalizer or bass-treble

- Loudness
  - SVC (smart volume control)
  - Volume/Balance/Soft-mute
  - Beeper
  - Video processing delay compensation
- For headphone:
  - SRS® TruBass™
  - SVC (smart volume control)
  - Bass-Treble
  - Loudness
  - Volume/Balance/Soft-mute
  - Beeper
  - Video processing delay compensation
- Shared outputs for headphone and loudspeakers surround channels:
- Analog matrix with:
  - five external inputs:
    - four SCART inputs (2 V<sub>RMS</sub> capable)
    - one analog mono input (0.5 V<sub>RMS</sub>)
  - one internal input from a digital matrix via a DAC
  - three external outputs (2 V<sub>RMS</sub> capable)
  - one internal output for the digital matrix (using an internal ADC)
- Digital matrix with:
  - three input modes (demodulator/SCART, SCART only and I<sup>2</sup>S)
  - three stereo outputs (loudspeakers, headphone and SCART)
- High-end audio DAC
- S/PDIF pass-thru/output for connection with an external amplifier/decoder
- Internal multiplexer for the S/PDIF output (to share the internal S/PDIF output and the S/PDIF output generated by the external decoder of the digital broadcast)
- Specific stand-by mode (Loop-through)
- Control by I<sup>2</sup>C bus (two I<sup>2</sup>C addresses)
- System PLL and clock generation using either a single quartz oscillator or a differential clock input

## 1.2 Software information

The different software combinations are listed in [Table 2](#)

**Table 2. Input/Output software configurations**

Input (number of channels)	Output (number of channels)		
	2 (+1)	4 (+1)	5 (+1)
1	ST WideSurround™ or SRS®, WOW™		



**Table 2. Input/Output software configurations (continued)**

Input (number of channels)	Output (number of channels)		
	2 (+1)	4 (+1)	5 (+1)
2 (L and R)	ST WideSurround or SRS <sup>®</sup> , WOW <sup>™</sup>		
2 (L <sub>T</sub> and R <sub>T</sub> )	ST WideSurround <sup>™</sup> or SRS <sup>®</sup> , TruSurround XT <sup>™</sup> or ST OmniSurround <sup>™</sup> or Dolby <sup>®</sup> , Pro Logic <sup>®</sup> , + SRS <sup>®</sup> , TruSurround XT <sup>™</sup> or Dolby <sup>®</sup> , Pro Logic <sup>®</sup> , + ST OmniSurround <sup>™</sup>	Dolby <sup>®</sup> , Pro Logic <sup>®</sup>	
4 (+1)	SRS <sup>®</sup> , TruSurround XT <sup>™</sup> or ST OmniSurround <sup>™</sup> or DownMix	No processing	
5 (+1)	SRS <sup>®</sup> , TruSurround XT <sup>™</sup> or ST OmniSurround <sup>™</sup> or DownMix	DownMix	No processing

Note: 1 In addition to the above sound processing, it is always possible to add ST Voice and also ST Dynamic Bass algorithms.

2 The SRS<sup>®</sup> TruSurround<sup>®</sup> and ST OmniSurround<sup>™</sup> are approved by Dolby<sup>®</sup> as Virtual Dolby<sup>®</sup> Surround (VDS) and Virtual Dolby<sup>®</sup> Digital (VDD).

The SRS<sup>®</sup>, TruSurround XT<sup>™</sup> system is composed of:

- SRS<sup>®</sup>, TruSurround
- SRS<sup>®</sup>, WOW<sup>™</sup>
- The SRS<sup>®</sup>, WOW<sup>™</sup> system includes:
  - SRS<sup>®</sup>, 3D Mono/Stereo<sup>™</sup>
  - SRS<sup>®</sup>, Dialog Clarity<sup>™</sup>
  - SRS<sup>®</sup>, TruBass<sup>™</sup>

### 1.2.1 Device input modes

- Demodulator only mode (with output  $f_S = 32$  kHz)
- Demodulator and SCART mode (with output  $f_S = 32$  kHz)
- SCART only mode (with output  $f_S = 48$  kHz)
- I<sup>2</sup>S mode (with output  $f_S = 32, 44.1$  or  $48$  kHz)
- External audio input interface using 3 x I<sup>2</sup>S (for decoded streams such as Dolby, Digital and/or standard stereo streams)

### 1.2.2 Electrical features

Multi power supply: 1.8 V, 3.3 V and 8 V.

Power consumption:

- lower than 1 W in functional mode (full features)
- 200 mW in loop-through mode corresponding to switch-off of all digital blocks

### 1.3 Typical applications

The STV82x7 is specified to enable flexible, analog and digital TV chassis design (refer to [Figure 1](#), [Figure 2](#) and [Figure 3](#)).

The main considerations are:

- all necessary connections between devices can be provided through the TV set,
- pseudo stand-by mode used to copy to VCR or the DVD sources when the TV set is OFF,
- possible application compatibility with STV82x6 (TQFP80 package) TV design,
- pin-to-pin compatibility with STV82x8 (TQFP80 package) TV design.

The STV82x7 is used to process a single audio source (analog or digital). However, it is possible to process two audio sources simultaneously using an STV82x7 interconnection (two chips can be easily connected).

In the case of a single audio source, it is possible to hear and record in the same time: the same audio stream can be simultaneously output on headphone, loudspeakers, S/PDIF and the SCART connectors.

*Note: Headphone and loudspeakers can be used simultaneously for dual-language purposes or for different sound settings (for example, volume). In this case, certain restrictions occur (see [Section 5.2: Audio processing](#)).*

For more connections, the SCART-to-SCART path can be used. The use of these full analog paths implies that the sound is not digitally processed.

Figure 1. STV8247 typical application (analog virtual sound)

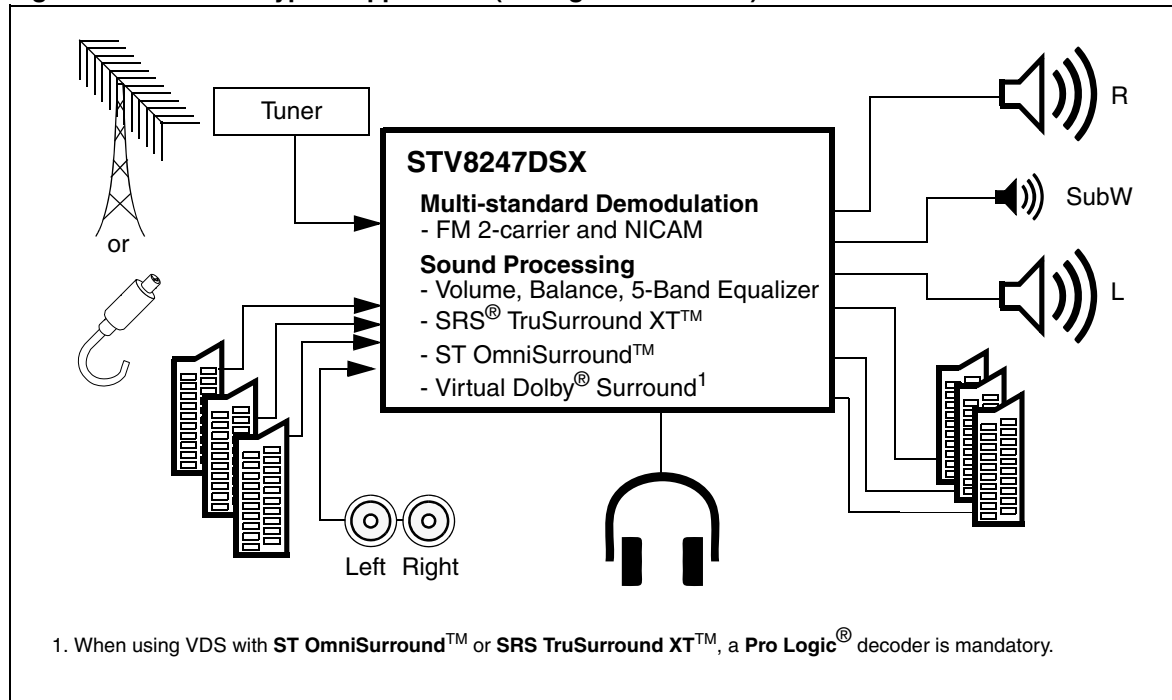


Figure 2. STV8257 typical application (digital: virtual sound)

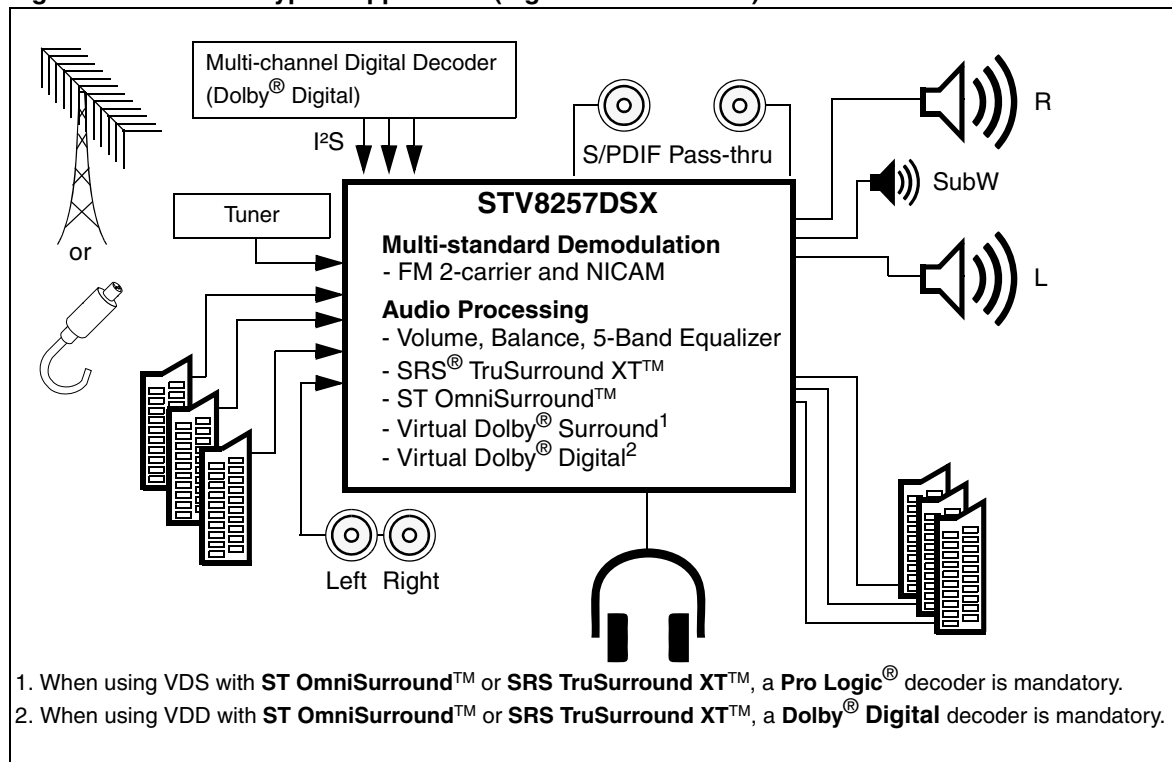
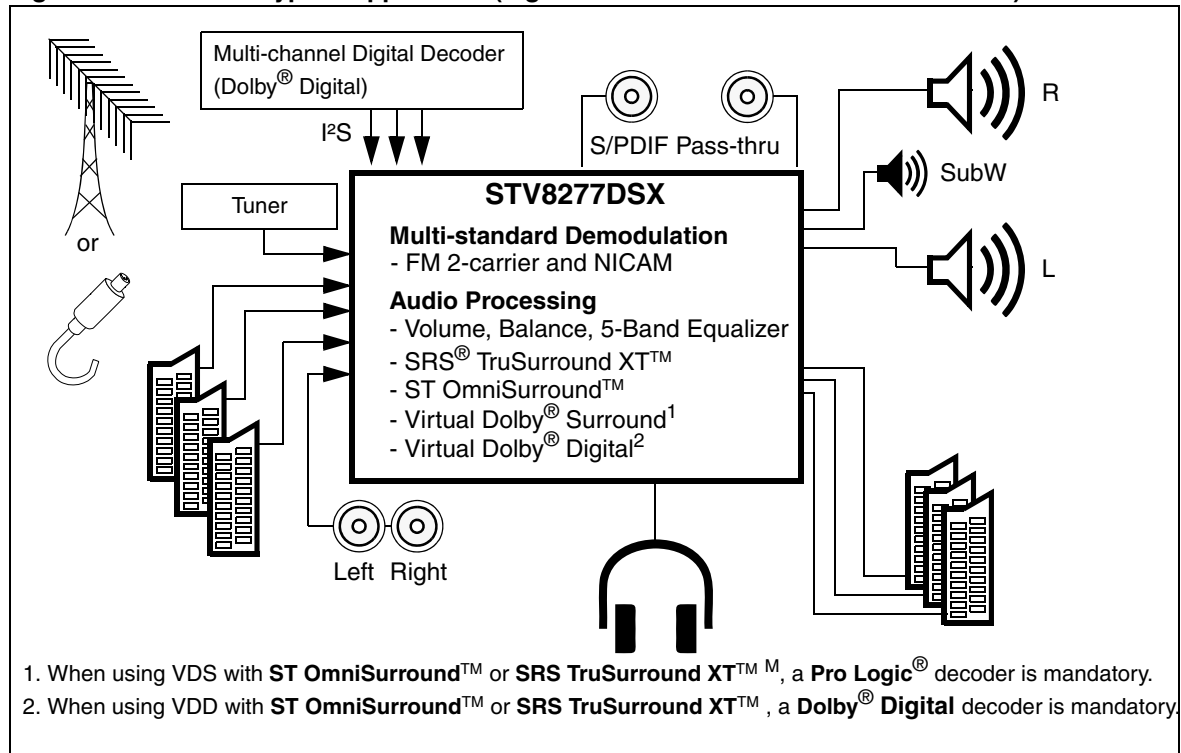


Figure 3. STV8277 typical application (digital TV: multi-channel and virtual sound)



## 2 System clock

The system clock integrates 2 independent frequency synthesizers.

The first frequency synthesizer can be used in one of two modes:

- In Mode 1, it is used by the demodulator, and the frequency is 49.152 MHz.
- In Mode 2, it is used by the I<sup>2</sup>S input and is synchronous with the input frequency ( $f_S = 32, 44.1$  or  $48$  kHz) and the frequency is 49.152 MHz (for  $f_S = 32$  or  $48$  kHz) or 45.1584 MHz (for  $f_S = 44.1$  kHz).

The second frequency synthesizer is used by the DSP core and can be adjusted between 100 and 150 MHz depending on the application (around 106 MHz at reset value).

In I<sup>2</sup>S output mode, clocks are generated by synthesizer 1.

The default values are designed for a **standard 27 MHz reference frequency** provided by a stable single crystal or an external differential clock signal (for example, from the STV35x0) depending on the CLK\_SEL pin configuration (CLK\_SEL = 1 means a single crystal, 0 means an external differential clock). The 27 MHz value is the recommended frequency for minimizing potential RF interference in the application. The sinusoidal clock frequency, and any harmonic products, remain outside the TV picture and sound IFs (PIF/SIF) and Band-I RF.

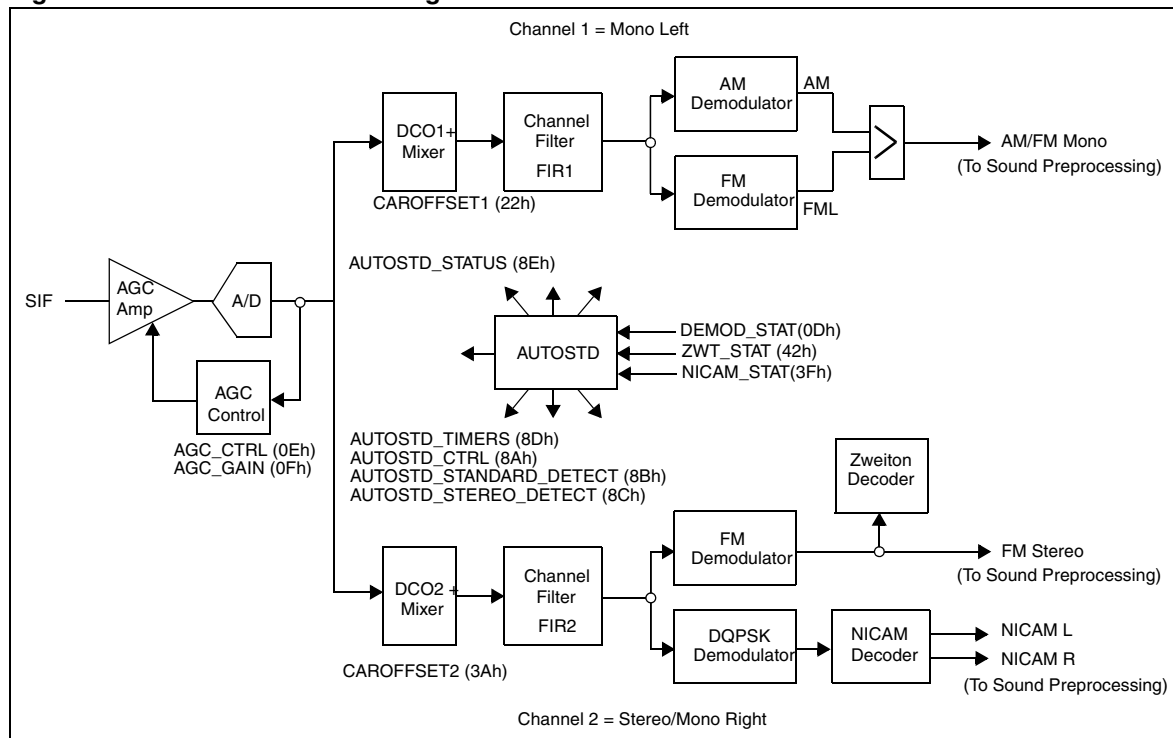
*Note: A change in the reference frequency is compatible with other default I<sup>2</sup>C programming values, including those of the built-in Automatic Standard Recognition System.*

### 3 Digital demodulator

The digital demodulator (see [Figure 4](#)) is composed of two channels. The first channel demodulates an FM or an AM signal. The second channel demodulates FM 2-carrier or NICAM signals (stereo demodulation).

All channel parameters are programmed automatically by the **built-in Automatic Standard Recognition System (Autostandard)** in order to find the correct sound standard. Channels can also be programmed manually via the I<sup>2</sup>C interface for very specific standards not included among the known standards.

**Figure 4. Demodulator block diagram**



#### 3.1 Sound IF signal

The analog sound carrier IF is connected to the STV82x7 via the SIF pin. Before ADC (analog-to-digital conversion), an AGC (automatic gain control) is performed to adjust the incoming IF signal to the full scale of the ADC. A preliminary video rejection is recommended to optimize conversion and demodulation performances. The AGC system provides a gain value allowing for a wide range of SIF input levels and is activated for all standards, except L/L'. In this particular case, the sound carrier is AM-modulated and an automatic level adjustment would only damage the transmitted audio signal. A preset I<sup>2</sup>C parameter is provided to define the gain of the AGC used in manual mode (Registers [AGC\\_CTRL](#) and [AGC\\_GAIN](#)).

*Note:* For optimum AM demodulation performance, it is recommended to use the MONO Input.

## 3.2 Demodulation

The demodulation system operates by default in Automatic mode. In this mode, the STV82x7 is able to **identify and demodulate any TV sound standard including NICAM and A2 systems** (see [Table 3](#)) without any external control via the I<sup>2</sup>C interface. It consists of the two demodulation channels (Channel 1 = Mono Left and Channel 2 = Mono Right/Stereo) to simultaneously process two sound carriers in order to handle all transmission modes (stereo and up to three mono languages). The **built-in Automatic Standard Recognition System** (Autostandard) automatically programs the appropriate bits in the I<sup>2</sup>C registers which are forced to Read-only mode for users (see [Section 12.1](#)). The programming is optimized for each standard to be identified and demodulated.

Each mono and stereo standard can be removed (or added) from the List of Standards to be recognized by programming registers [AUTOSTD\\_STANDARD\\_DETECT](#) and [AUTOSTD\\_STEREO\\_DETECT](#), respectively. The identified standard is displayed in register [AUTOSTD\\_STATUS](#) and any change to standard is flagged to the host system via pin IRQ. This flag must be reset by re-programming the MSBs of register [AUTOSTD\\_CTRL](#) while checking the detected standard status by reading registers [AUTOSTD\\_STATUS](#), [NICAM\\_STAT](#) and [ZWT\\_STAT](#). Moreover, the detection of Stereo mode during demodulation is also flagged in register [AUTOSTD\\_STATUS](#).

**Important:** L/L' and D/K standards cannot be automatically processed because the same frequency is used for the MONO carrier. An exclusive L/DK selection must be programmed in register [AUTOSTD\\_CTRL](#). This may be externally controlled by detecting the RF modulation sign, which is negative for all TV standards except L/L'.

To recover out-of standard FM deviations or the Sound Carrier Frequency Offset, additional I<sup>2</sup>C controls are provided without interfering with the Automatic Standard Recognition System (Autostandard).

**DK-NICAM overmodulation recovery:** Four different FM deviation ranges can be selected (via register [AUTOSTD\\_CTRL](#)) for the DK standard while the Autostandard system remains active. The maximum FM deviation is 500 kHz in DK Mono mode and 350 kHz in DK NICAM mode (limited by overlapping FM and NICAM spectrum values). The demodulated signal peak level (proportional to the FM deviation) is detected by the Peak Detector and written to registers [PEAK\\_DET\\_L](#) and [PEAK\\_DET\\_R](#). This value is used to implement automatic overmodulation detection via an external I<sup>2</sup>C control.

**Important:** Only the selection of the 50 kHz FM deviation standard is compatible with the other DK-A2\* standards (DK1, DK2 or DK3). These standards must be removed from the list of standards (registers [AUTOSTD\\_STANDARD\\_DETECT](#) and [AUTOSTD\\_STANDARD\\_DETECT](#)) when programming larger FM deviations reserved only for DK-NICAM standards.

**Table 3. Recognized standards**

System	Sound type	Type name	Carrier 1 (MHz)	Carrier 2 (MHz)	FM deviation			De-emphasises	Roll-off (%)	Pilot freq. (kHz)
					Nom.	Max.	Over			
B/G	FM mono		5.5							
	FM/NICAM		5.5	5.850	27	50	80	J17	40	
	FM 2-carrier	A2	5.5	5.742	27	50	80	50 µs		54.6875

Table 3. Recognized standards (continued)

System	Sound type	Type name	Carrier 1 (MHz)	Carrier 2 (MHz)	FM deviation			De-emphasiss	Roll-off (%)	Pilot freq. (kHz)
					Nom	Max.	Over			
D/K	FM mono		6.5							
	FM/NICAM		6.5	5.850	27	50	80	J17	40	
D/K1	FM 2-carrier	A2*	6.5	6.258				50 $\mu$ s		54.6875
D/K2	FM 2-carrier	A2*	6.5	6.742				50 $\mu$ s		54.6875
D/K3	FM 2-carrier	A2*	6.5	5.742				50 $\mu$ s		54.6875
I	FM mono		6.0							
	FM/NICAM		6.0	6.552	27	50	80	J17	100	
L	AM/NICAM		6.5	5.850				J17	40	
M/N	FM mono		4.5		15	27	50	75 $\mu$ s		
	FM 2-carrier	A2+	4.5	4.724	15	27	50	75 $\mu$ s		55.069

For Chinese TV transmissions (DK-NICAM) which are subject to overmodulation, different FM deviations are proposed for sound demodulation.

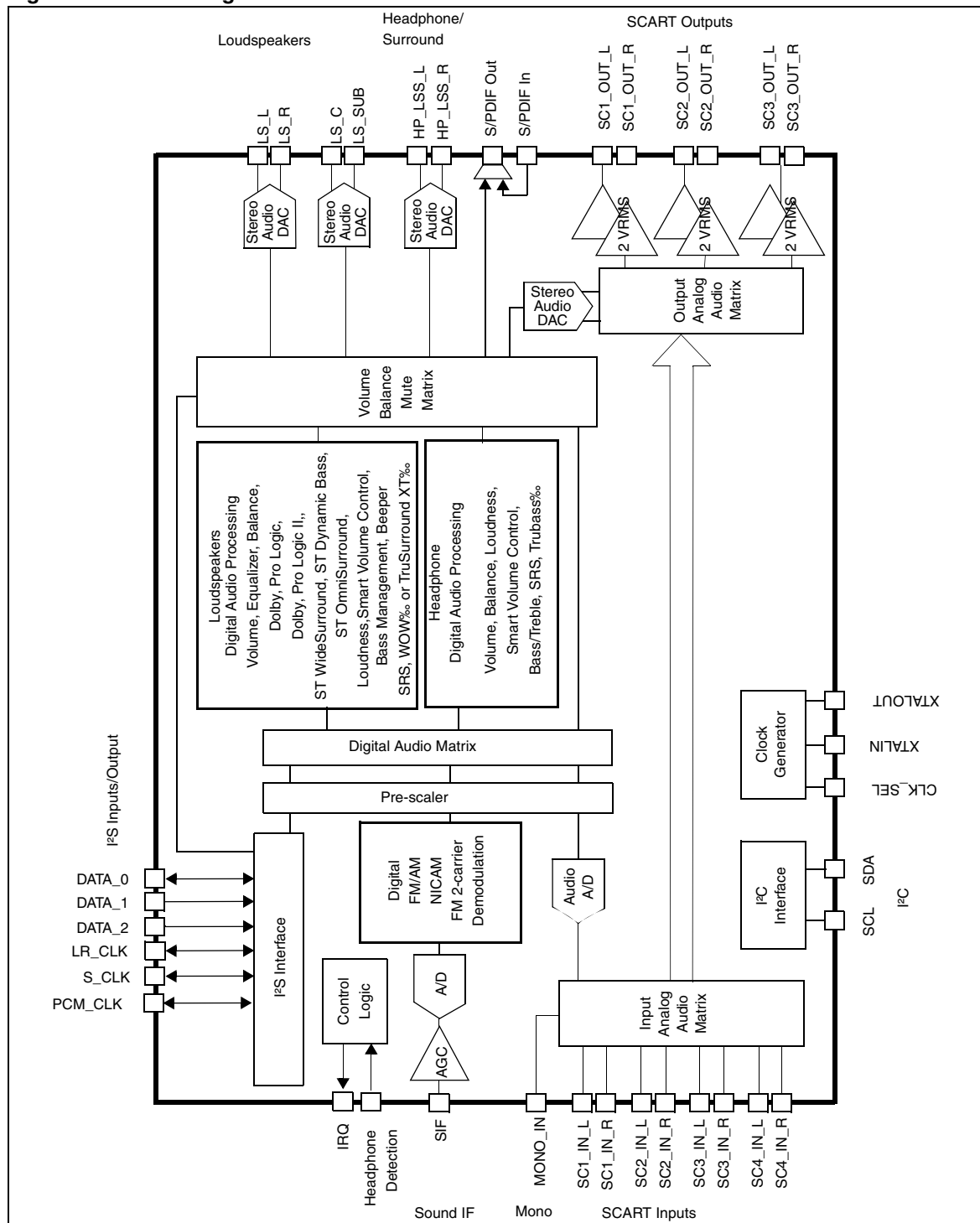
**Sound Carrier Frequency Offset Recovery:** Both Mono and Stereo IF Carrier frequencies can be adjusted independently (registers [CAROFFSET1](#) and [CAROFFSET2](#)) within a large range (up to 120 kHz for standard mono FM deviations) while the Automatic Standard Recognition System remains active. The frequency offset estimation is written in registers [DC\\_REMOVAL\\_L](#) and [DC\\_REMOVAL\\_R](#) (Mono Left / Channel 1 and Mono Right / Channel 2, respectively) and can be used to implement the Automatic Frequency Control (AFC) via an external I<sup>2</sup>C control.

**Manual Mode:** If required, the Automatic Standard Recognition System system can be disabled (Manual mode) and the user can control all registers including those only controlled by the Automatic Standard Recognition System function when active. Manual mode is selected in register [AUTOSTD\\_STANDARD\\_DETECT](#) (bit LDK\_SCK, I\_SCK, BG\_SCK and MN\_SCK set to 0).



# 4 Block diagram

Figure 5. Block diagram



## 5 Digital signal processor

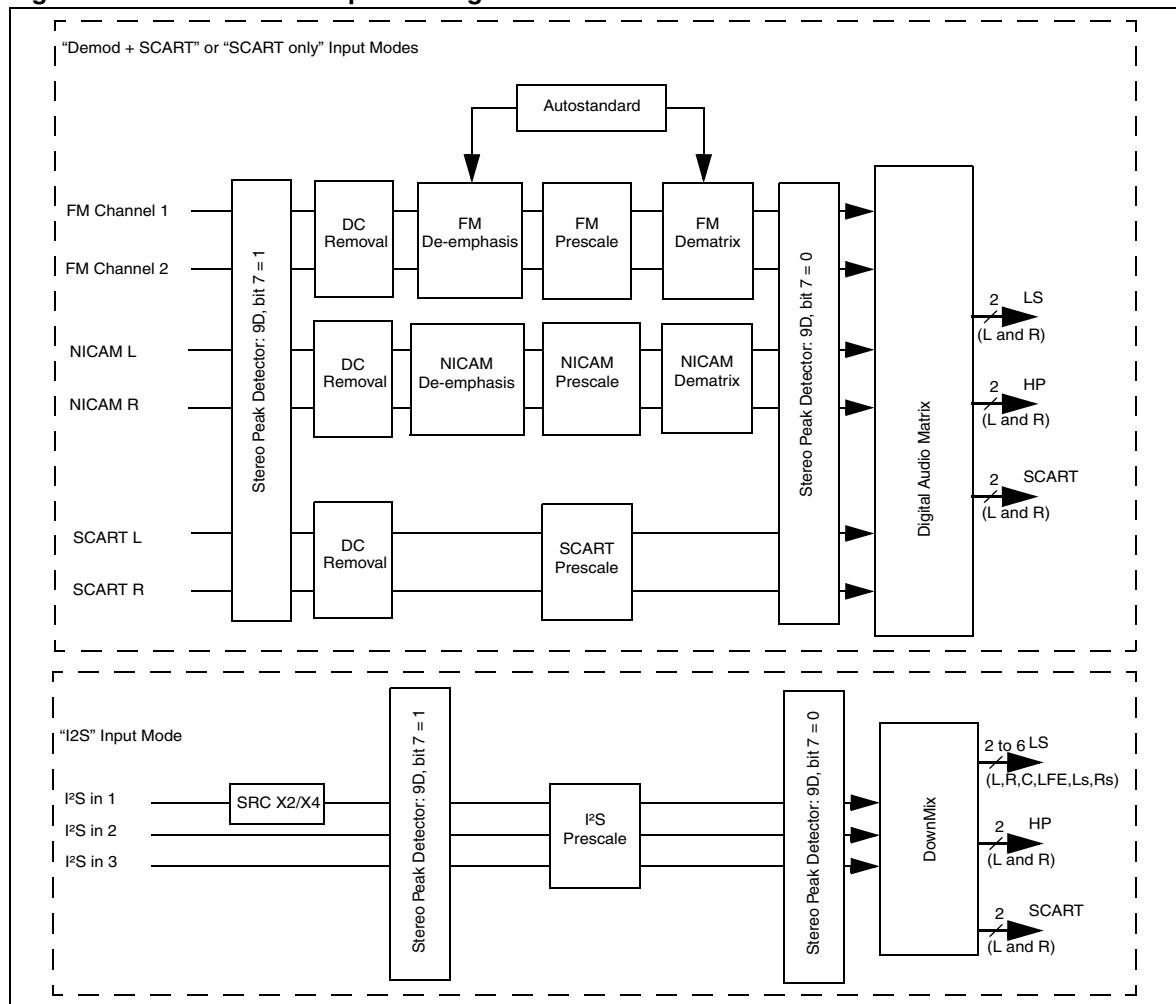
A dedicated DSP (digital signal processor) takes charge of all audio processing features and the low frequency signal processing features of the demodulator. The internal 24-bit architecture will ensure a high quality signal treatment and an excellent dynamic.

### 5.1 Back-end processing

The “back-end” processing corresponds to the low frequency signal processing (32 kHz or higher frequencies) of the demodulator and other inputs (I<sup>2</sup>S, ADC).

Figure 6 shows a flowchart of the back-end processing tasks. However, the figure shows that the processing is only a SINGLE SOURCE PROCESSING flow (no processing is possible with “Demod + SCART” and I<sup>2</sup>S inputs simultaneously) and that the selection of a headphone output restricts the loudspeakers configuration to 2+1 instead of 5+1

Figure 6. Back-end audio processing



The main features depend on the path:

- FM Channel
  - DC removal
  - Prescaling
  - De-emphasis (50 or 75 us)
  - Stereo dematrix
- NICAM channel
  - DC removal
  - Prescaling
  - De-emphasis (J17)
  - Dematrix
- Input SCART channel
  - DC removal
  - Prescaling
- Input I<sup>2</sup>S channel
  - I<sup>2</sup>S prescaling
- Digitalaudio matrix
  - Audio channel multiplexer between the different sources (IF, I<sup>2</sup>S, SCART) towards all outputs (S/PDIF, LS, HP or SCART).
- Autostandard management
  - Device configuration depending on the standard to be detected
  - Freeze the device when a standard is detected
  - Once a standard detected, check that there is no change in the detection status
  - Set the correct action depending on any change in the detection status (mono backup or mute setup and new standard detection)
- SCART
  - Downmixing: L<sub>T</sub> / R<sub>T</sub> or L<sub>0</sub> / R<sub>0</sub> (see AC-3 specification)
  - Soft mute

## 5.2 Audio processing

**The following software is provided for main loudspeakers (L, R, C, L<sub>S</sub>, R<sub>S</sub>, SubW):**

- Downmix
- Dolby® Pro Logic II® decoder (L<sub>T</sub>, R<sub>T</sub> → L, R, C, L<sub>S</sub>, R<sub>S</sub>, SubW) with bass management
- ST WideSurround™, ST OmniSurround™, SRS® WOW™, or SRS® TruSurround XT™, (certified Virtual Dolby® Surround and Virtual Dolby® Digital)
- ST Dynamic Bass™,
- SVC (smart volume control)
- 5-band equalizer or bass-treble
- Loudness
- Volume with independent channels (smooth volume control)
- Master volume control
- Mute/soft-mute
- Balance
- Beeper
- Pink noise generator (used to position the loudspeakers)
- Programmable delay for each loudspeaker
- Adjustable delay for “lip sync” to compensate audio/video latency up to 60 ms in SCART only mode (processing at 48 KHz) and up to 90 ms in demodulator and SCART mode (processing at 32 KHz)

**The following software is provided for the headphone or auxiliary output:**

- Downmix
- SRS® TruBass™,
- SVC (smart volume control)
- Bass/treble
- Loudness
- Independent volume for each channel (smooth volume control)
- Soft mute
- Balance
- Beeper
- Adjustable delay for “lip sync” up to 120 ms (to compensate audio/video latency) in SCART only mode and up to 180 ms in demodulator and SCART mode

**The following software is provided for SCART or S/PDIF outputs:**

- Downmix
- Soft mute

Figure 7. STV82x7 audio processing flowchart (front end)

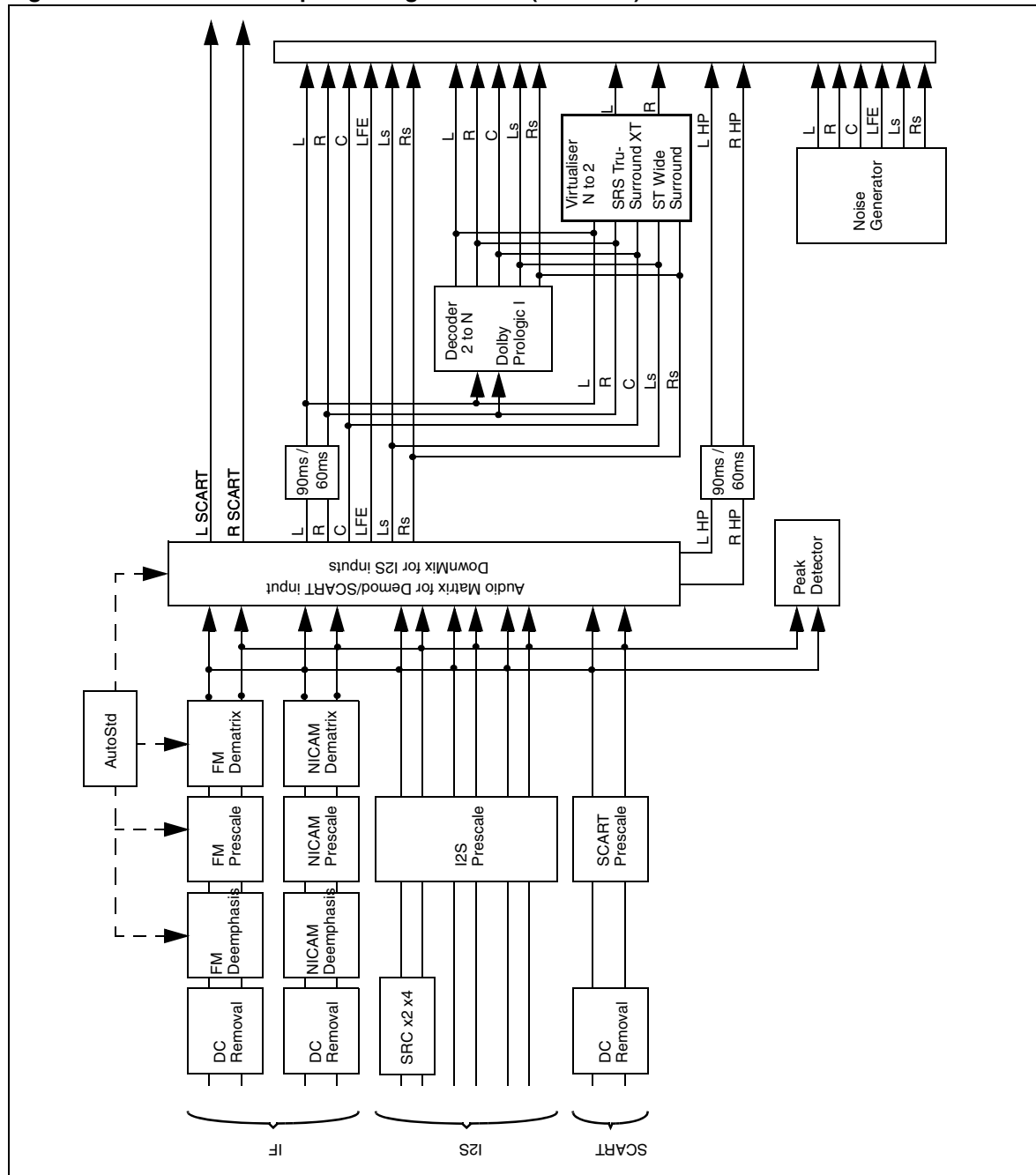
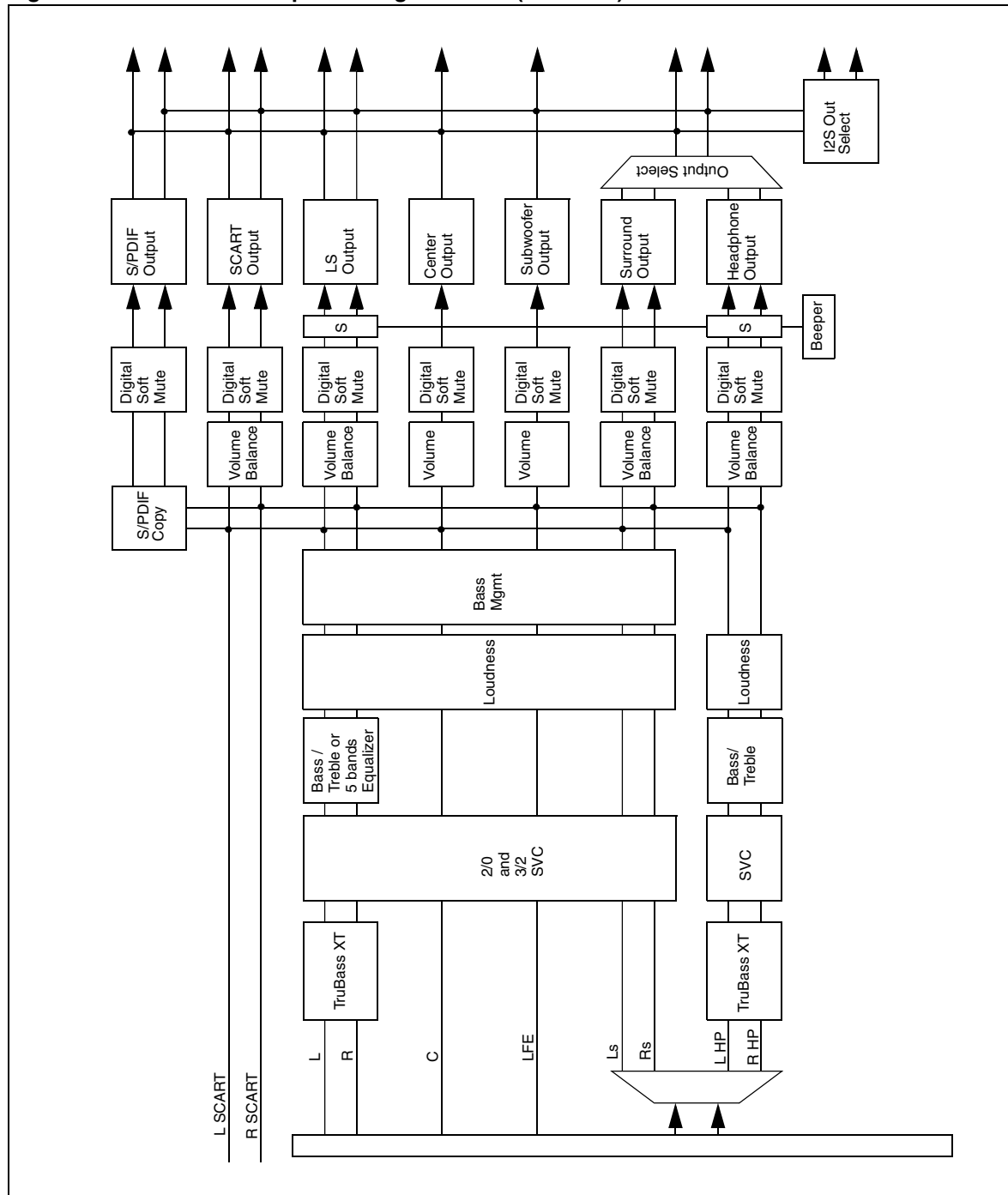


Figure 8. STV82x7 audio processing flowchart (back end)



### 5.3 ST WideSurround

STV82x7 offers three preset ST WideSurround™ sound effects on the loudspeakers path:

- Music, for a concert hall effect
- Movie, for films on TV
- Simulated stereo, which generates a pseudo-stereo effect from mono source

ST WideSurround™ sound is an extension of the conventional stereo concept which improves the spatial characteristics of the sound. This could be done simply by adding more speakers and coding more channels into the source signal as is done in the cinema, but this approach is too costly for normal home use. The ST WideSurround system exploits a method of phase shifting to achieve a similar result using only two speakers. It restores spatiality by adding artificial phase differences.

The surround/pseudo-stereo mode is automatically selected by the Automatic Standard Recognition System (Autostandard) depending on the detected stereo or mono source. By default, “Movie” is selected for surround mode. This value may be changed to “Music” by the STSRND\_MODE bit in the [STSRND\\_CONTROL](#) register.

Additional user controls are provided to better adapt the spatial effect to the source. The ST WideSurround™ gain ([STSRND\\_LEVEL](#)) and ST WideSurround™ frequency ([STSRND\\_FREQ](#)) registers can be used to enhance music predominancy in music mode and theater effect and voice predominancy in movie mode.

### 5.4 ST OmniSurround

STV82x7 offers a spatial virtualizer to output any multi-channel input in stereo on the loudspeakers path:

ST OmniSurround™ will recreate a multi-channel spatial sound environment using only the left and right front speakers. It can be adapted to any input configuration (OMNISRND\_INPUT\_MODE).

ST Voice™ will allow you to enhance the voice content of your program to increase the intellegibility and the presence of the sound.

### 5.5 Dolby Pro Logic II decoder

Dolby® Pro Logic II® is a matrix decoder that decodes the five channels of surround sound that have been encoded onto the stereo sound tracks of Dolby® Surround program material such as DVD movies and TV shows.

It is even possible to decode standard stereo signals like music or non encoded movies. Furthermore, it is an active process designed to enhance sound localization through the use of very high-separation decoding techniques.

The Dolby® Pro Logic II® decoder is also able to emulate the former Dolby® Pro Logic® decoder in a specific mode.

## 5.6 Bass management

This processing will generate the subwoofer signal and adjust all loudspeakers channels gain and bandwidth.

Speakers capable of reproducing the entire frequency range will be referred to as “full range speakers”, then signals sent to full range speaker will be full bandwidth (no filtering).

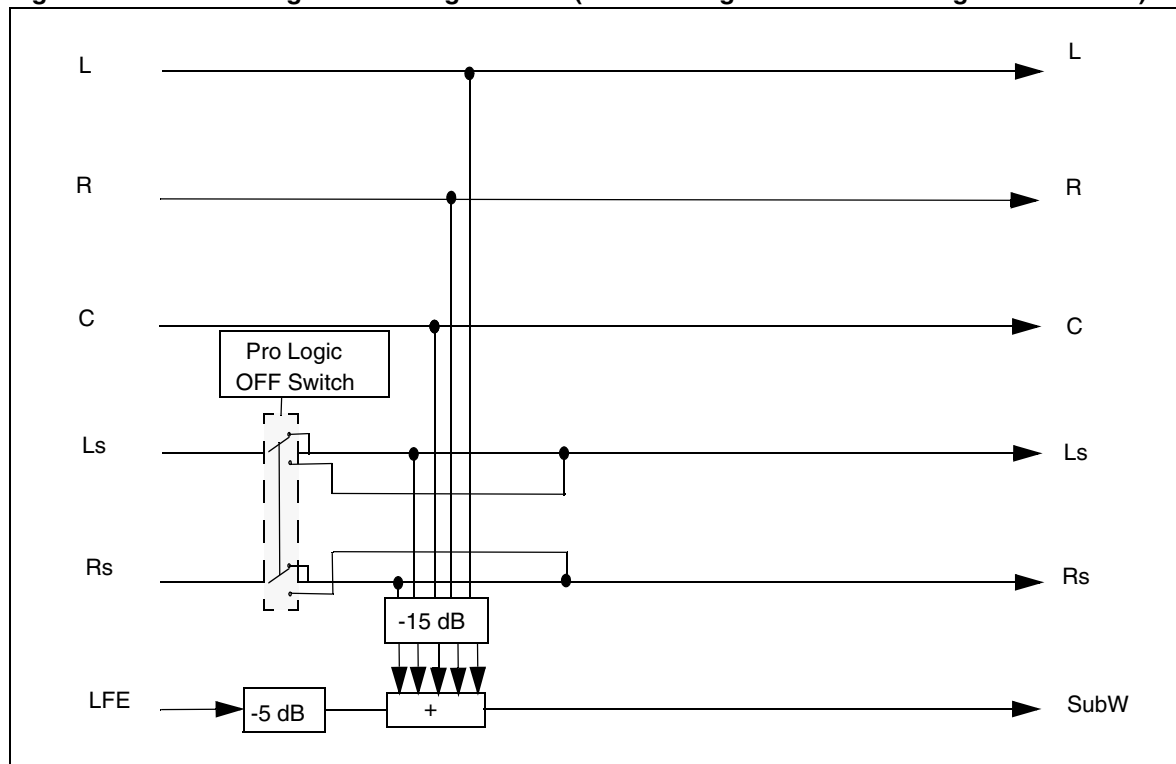
Speakers that have limited bass handling capabilities will be referred to as “satellite speakers”, then signals sent to satellite speaker will be high-pass filtered to remove bass information below 100 Hz.

In the STV82x7, five output configuration modes have been implemented according to “Dolby Digital Consumer Decoder” specifications. They are described below.

## 5.7 Bass management configuration 0

In some cases, the bass management filters are available in the decoder itself, so there is no need to reproduce these filters. The output configuration shown in [Figure 9](#) offers this possibility.

**Figure 9. Bass management configuration 0 (with Pro Logic switch indicating its reset state)**



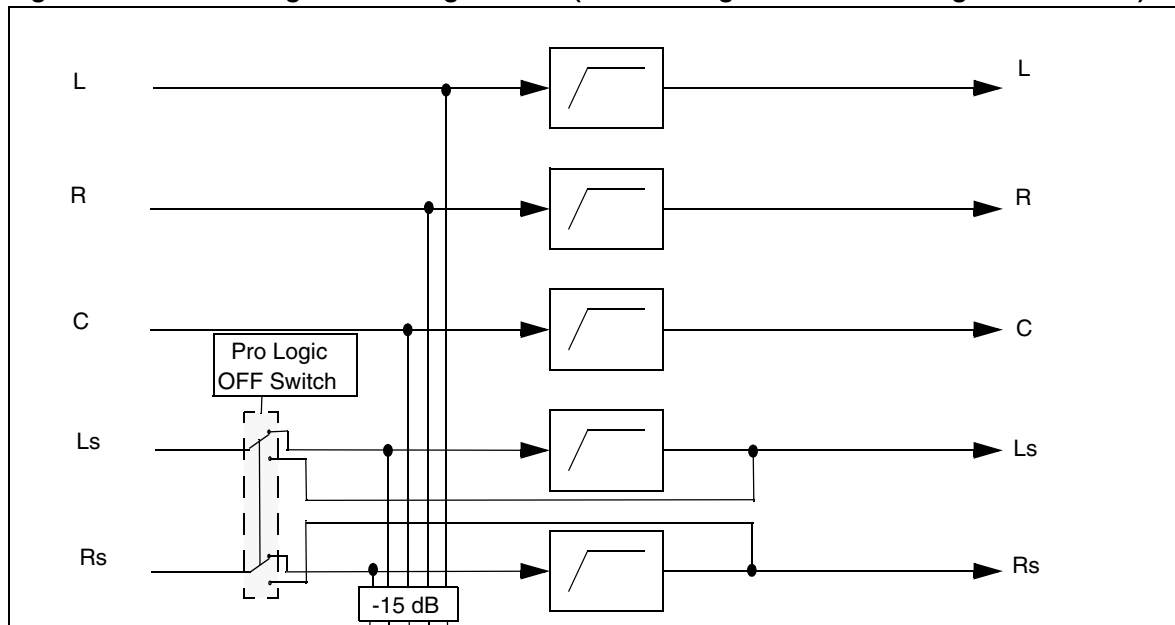


## 5.8 Bass management configuration 1

Configuration 1, shown in [Figure 10](#), assumes that all five speakers are not full range and that all of the bass information will be redirected to and reproduced by a single subwoofer. This configuration is intended for use with 5 satellite speakers.

To prevent signal overload, the five main channels are attenuated by 15 dB, while the LFE channel is attenuated by 5 dB to maintain the proper mixing ratio.

**Figure 10. Bass management configuration 1 (with Pro Logic switch indicating its reset state)**

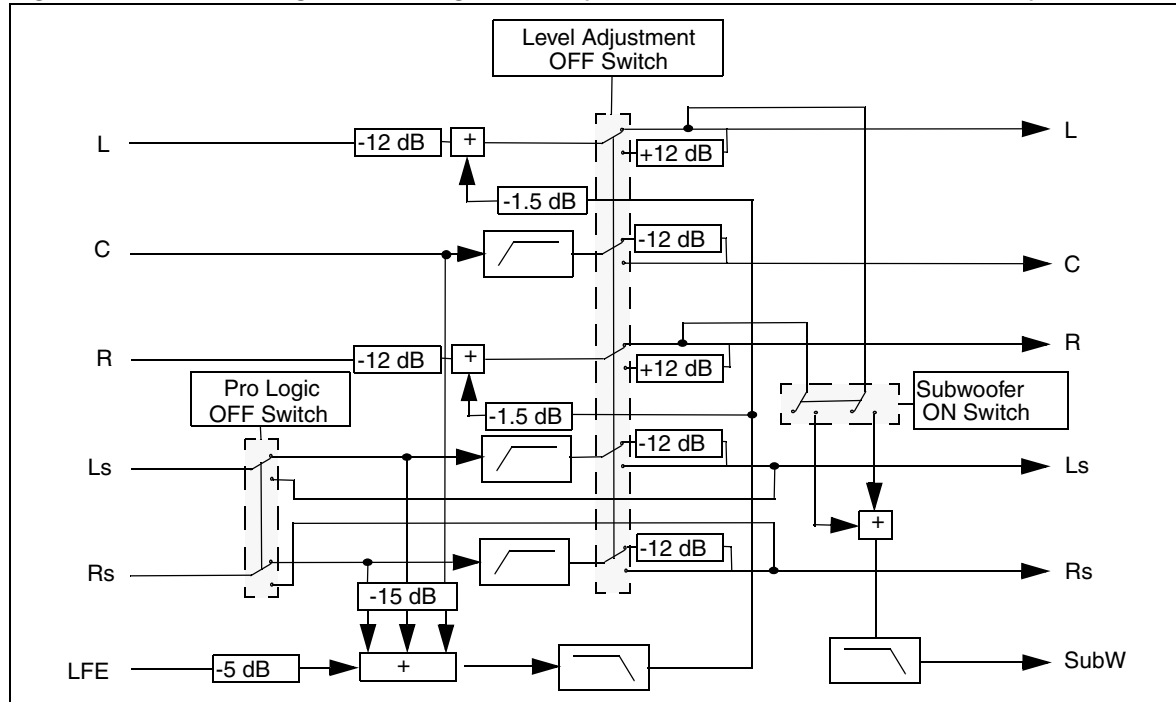


### 5.9 Bass management configuration 2

Configuration 2 assumes that the left and right speakers, are full range while the center and surround speakers are smaller speakers. Also, all bass data is redirected to the left and right speakers.

This configuration include output level adjustment that allows 12 dB attenuation for the 3 smaller speakers (C, Ls, Rs). When the level adjustment will be disabled the decoder boosts by 12 dB the full range speakers (Left, Right).

Figure 11. Bass management configuration 2 (all switches indicate their reset state)

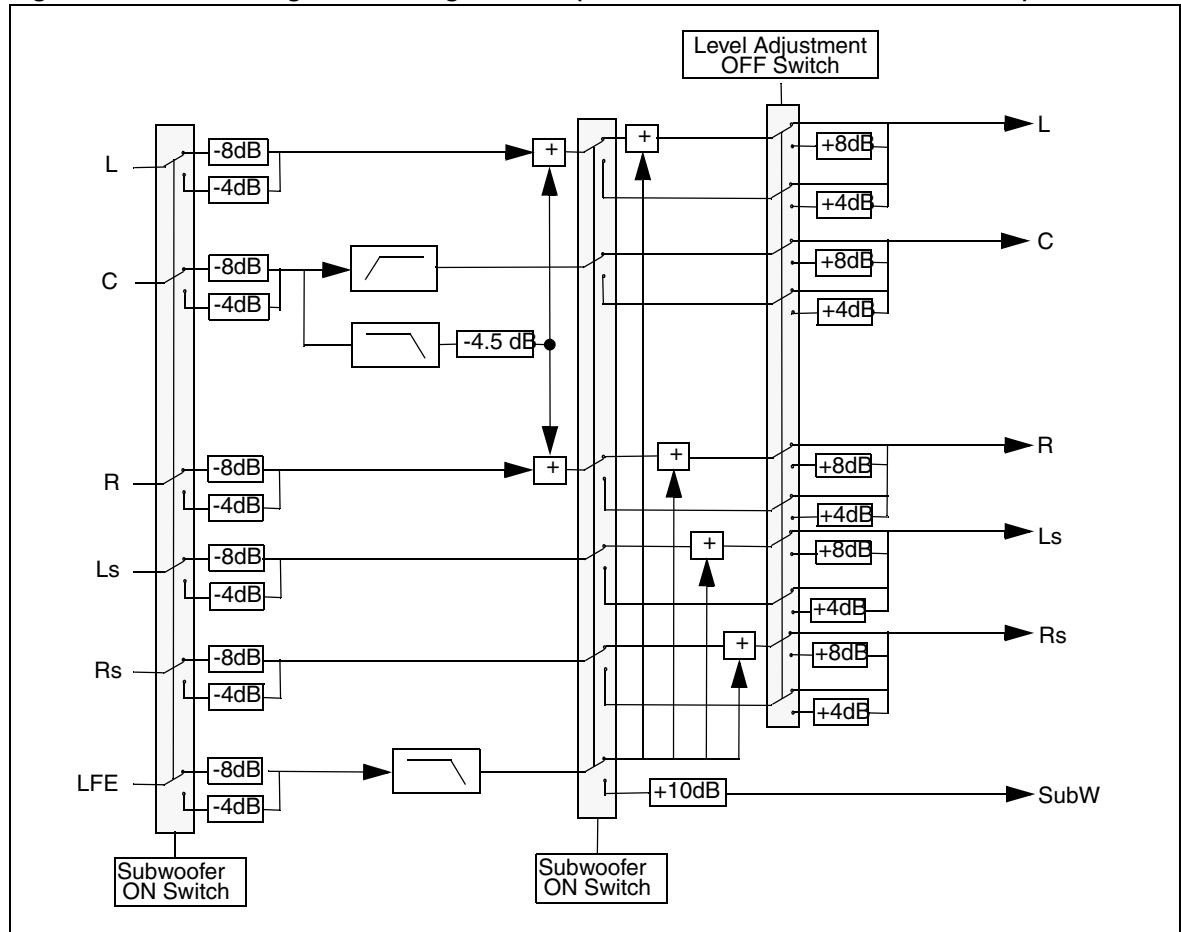


### 5.10 Bass management configuration 3

The third configuration, shown in [Figure 12](#), assumes that all speakers except the center are full range, then all bass information will be directed to and reproduced by the front left and front right and both surround speakers. In order to provide more flexibility to this configuration, a switch will offer an option which will produce a subwoofer channel by the LFE channel.

When the subwoofer switch is OFF, the input channels will be attenuated by 8 dB. Configuration 3 is required in certain high-end products.

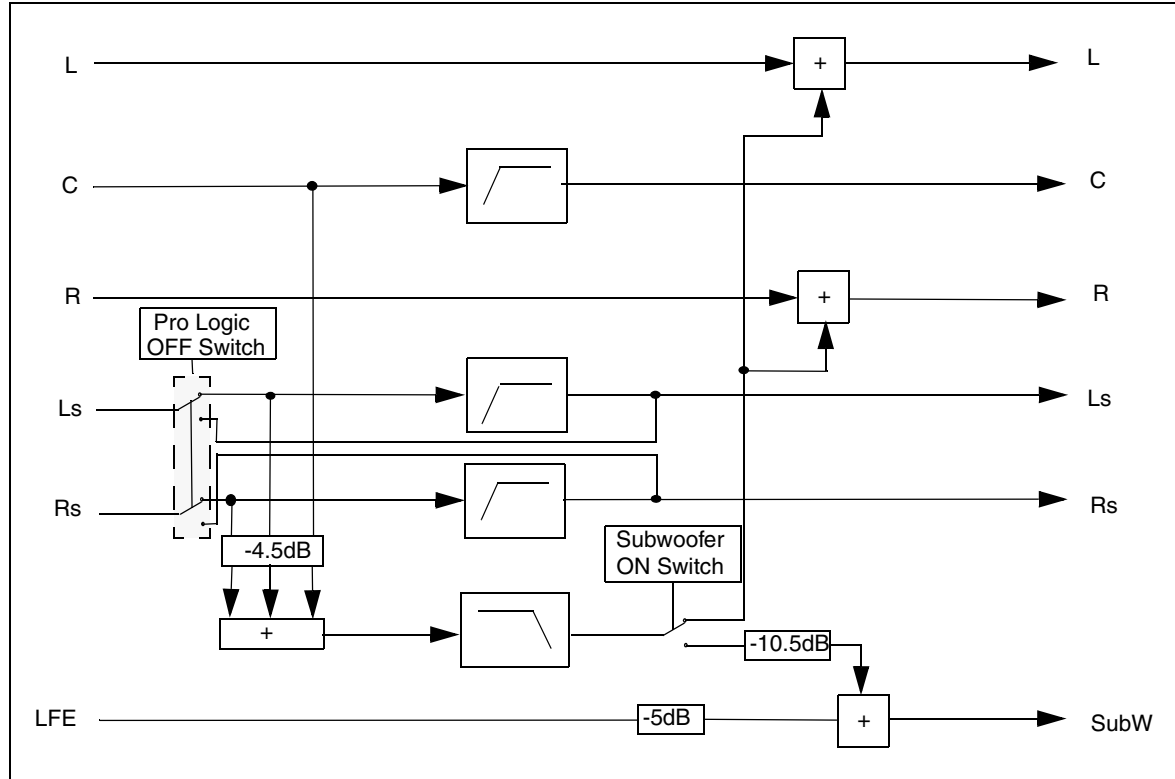
**Figure 12. Bass management configuration 3 (all switches indicate their reset state)**



### 5.11 Bass management configuration 4

This configuration implements the simplified Dolby® configuration. The center, left surround and right surround channels are summed and then filtered by the LPF. The composite bass information is either summed back into the left and right channels or summed with the LFE channel and sent to the subwoofer output, see [Figure 13](#).

**Figure 13. Implementation of the bass management configuration 4 (simplified configuration)**



### 5.12 SRS WOW and TruSurround XT

The SRS® TruSurround XT™ is a processing system that can accept from 1 to 6 channels on input and generate a 2-channel output signal.

This processing system includes the latest SRS® algorithms:

- SRS® WOW™
- SRS® TruSurround® (multi-channel signal virtualizer)

## 5.13 SRS TruSurround

The SRS® TruSurround® is a processing system that can accept from 2 to 5 channels on input and generate a 2-channel output signal.

SRS® TruSurround® uses HRTF (head-related transfer function) -based frequency tailoring of (L/R) difference signals to extend the sound image out past the physical boundaries of the speaker placements to surround channel information. These rear channel HRTF curves have much greater peak to valley differences at center frequencies. These were chosen to cause rear channel difference signals to virtualize farther behind the listener and directed to a different virtual position as compared to front channel signals. Information that is equal (L+R) in the rear surround channels is processed by an identical HRTF curve but mixed in at a much lower amount. This HRTF processing of equal (L/R) signals was again used to virtualize information to the rear of the listener.

The SRS® TruSurround® is certified by Dolby Laboratories to be a Virtual Dolby® Digital and Virtual Dolby® Surround.

## 5.14 SRS WOW

The SRS® WOW™ is an a sound processing system including:

- SRS® 3D Mono/Stereo™
- SRS® Dialog Clarity™
- SRS® TruBass™

### 5.14.1 SRS 3D Mono/Stereo

The SRS® 3D Mono/Stereo™ system is used to create a pseudo-stereo signal for mono inputs or a three-dimensional spatial signal for stereo inputs.

### 5.14.2 SRS Dialog Clarity

The Digital Clarity™ system is used to enhance dialog perception.

### 5.14.3 SRS TruBass

The SRS® TruBass™ audio enhancement technology provides deep, rich bass to small speaker systems without the need for a subwoofer or additional extra physical components. For systems with a subwoofer, SRS® TruBass™ complements and enhances bass performance. Psycho-acoustically, when the human ear is presented with a low frequency sound signal that is missing the fundamental harmonic, it will fill in the fundamental frequency based on the higher harmonics that are present. By accentuating the second and higher frequency harmonics of the bass portion of a signal, SRS® TruBass™ gives the perception of greatly improved bass response.

SRS® TruBass™ is implemented on loudspeakers path, headphone path or on both in parallel.

## 5.15 SVC (smart volume control)

SVC (smart volume control) regulates the audio signal level before audio processing. This regulation is necessary in order for the signal level to be independent from the source (terrestrial channels, I<sup>2</sup>S or SCART), its modulation (AM, FM or NICAM) and annoying volume changes (advertising, etc.). SVC works as an audio compressor/expander; that is, when the input signal exceeds the threshold level, a very rapid attenuation (-2 dB/ms) is applied to rescale the signal down to the threshold value. When the input signal is below the threshold level, the previous attenuation is reduced slowly in order to retrieve the original input level (0 dB gain). If the input signal is too low, an addition gain of 6 dB can be provided.

To personalize the action of the SVC, five parameters are available:

1. Threshold: maximum quasi-peak level that can be expected on output
2. Peak measurement mode: selects the channel on which the peak measurement must be performed (left, right, center...)
3. Release time: applies gain slope to the amplification phase
4. Expander switch: allows a +6dB amplification of small signals in order to reduce the output dynamic range
5. Make up gain: allows compensation of the signal amplitude limitation thanks to a 0 to 24 dB adjustable gain.

The SVC is implemented on the loudspeakers path, headphone path or on both in parallel (independent settings). Also, the SVC can be applied in six-channel mode (L, R, L<sub>S</sub>, R<sub>S</sub>, C and SubW).

## 5.16 ST Dynamic Bass

STV82x7 offers dynamic bass boost processing on the loudspeakers path.

ST Dynamic Bass™ is a bass boost process that can dramatically increase the bass content of any program without any output level saturation.

3 cutoff frequencies (BASS\_FREQ) can be chosen, 100 Hz, 150 Hz and 200 Hz to adapt the effect to your loudspeakers. The amount of bass (BASS\_LEVEL) can also be fine tuned in order to adapt the effect loudness.

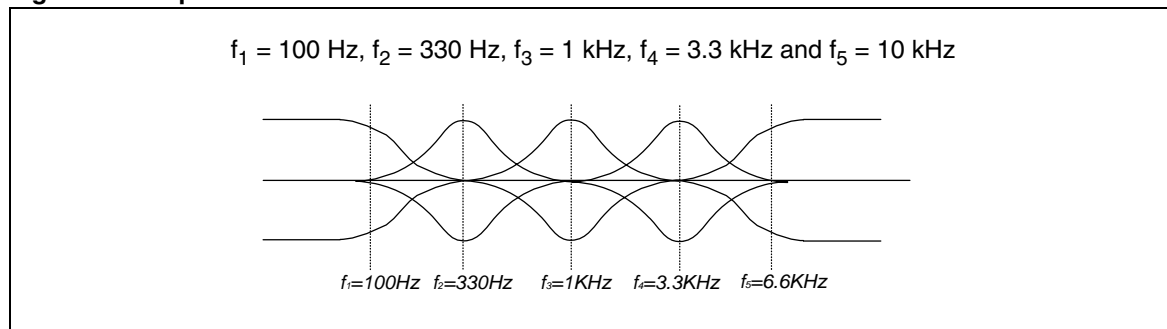
## 5.17 5-band audio equalizer

The loudspeakers audio spectrum is split into 5 frequency bands and the gain of each of band can be adjusted within a range from -12 dB to +12 dB in steps of 0.25 dB. The audio equalizer may be used to pre-define frequency band enhancement features dedicated to various kinds of music or to attenuate frequency resonances of loudspeakers or the listening environment. The equalizer is enabled by the LS\_EQ\_ON bit in the [LS\\_EQ\\_BT\\_CTRL](#) register. The gain value for band X is programmed in register [EQ\\_BANDX\\_GAIN](#).

The 5-band audio equalizer is exclusive with bass-treble control. Bit LS\_EQ\_BT\_SW in register [LS\\_EQ\\_BT\\_CTRL](#) is used to select either the 5-band audio equalizer or the bass-treble control for the Loudspeakers path.

Depending on the LS equalizer or LS bass-treble value, the volume level can be clamped to the LS output to prevent any possible signal clipping from occurring using the ANTICLIP\_LS\_VOL\_CLAMP bit in the [VOLUME\\_MODES](#) (D7h) register.

Figure 14. Equalizer



## 5.18 Bass/Treble control

The gain of bass and treble frequency bands for headphone can be also tuned within a range from -12 dB to +12 dB in steps of 0.25 dB. It may be used to pre-define frequency band enhancement features dedicated to various kinds of music. The Headphone Bass/Treble feature is enabled by setting the HP\_BT\_ON bit in the [HP\\_BT\\_CONTROL](#) register. The Bass and Treble gain values are adjusted in registers [HP\\_BASS\\_GAIN](#) and [HP\\_TREBLE\\_GAIN](#), respectively.

Depending on the HP Bass-Treble value, the volume level can be clamped to the HP output to prevent any possible signal clipping from occurring using the ANTICLIP\_HP\_VOL\_CLAMP bit in the [VOLUME\\_MODES](#) (D7h) register.

## 5.19 Automatic loudness control

As the human ear does not hear the audio frequency range the same way depending on the power of the audio source, the Loudness Control corrects this effect by sensing the volume level and then boosting bass and treble frequencies proportionally to middle frequencies at lower volume.

While maintaining the amplitude of the 1 kHz components at an approximately constant value, the gain values of lower and higher frequencies are automatically progressively amplified up to +18 dB when the audio volume level decreases. The maximum treble amplification can be adjusted from 0 dB (first order loudness) to +18 dB (second order loudness) in steps of 3 dB. As the volume is proportional to the external audio amplification power, the loudness amplification threshold is programmable in order to tune the absolute level. The loudspeakers loudness function is enabled by setting the LS\_LOUD\_ON bit in register [LS\\_LOUDNESS](#). The loudspeakers loudness threshold and maximum treble gain values are also programmed in this register. The headphone loudness function is enabled by setting the HP\_LOUD\_ON bit in register [HP\\_LOUDNESS](#). The headphone loudness threshold and maximum treble gain values are also programmed in this register.

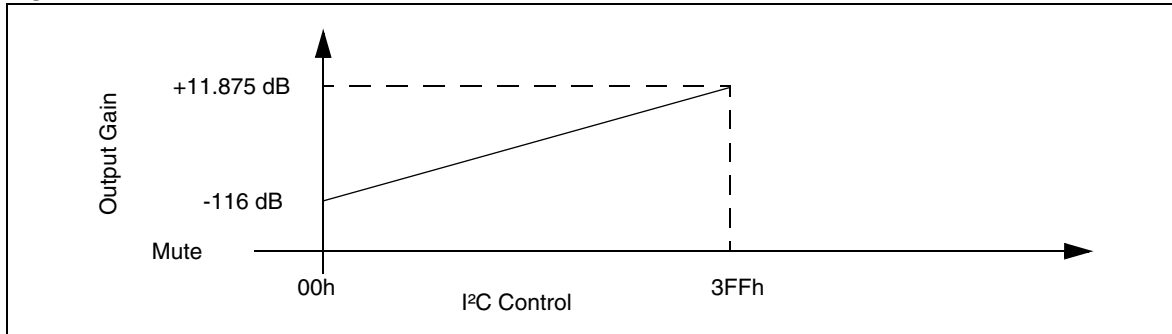
The loudness cut-off frequency is 100 Hz.

## 5.20 Volume/Balance control

The STV82x7 provides a volume/balance control for all output channels configuration (except for S/PDIF) with different volume level per channel (L, R, C, L<sub>S</sub>, R<sub>S</sub>, SubW, SCART).

Its wide range (from +11.875 to -116 dB, in a dB linear scale with a 0.125 dB step) largely covers typical home applications (approx. 60 dB) while maintaining a good S/N ratio.

**Figure 15. Volume control**



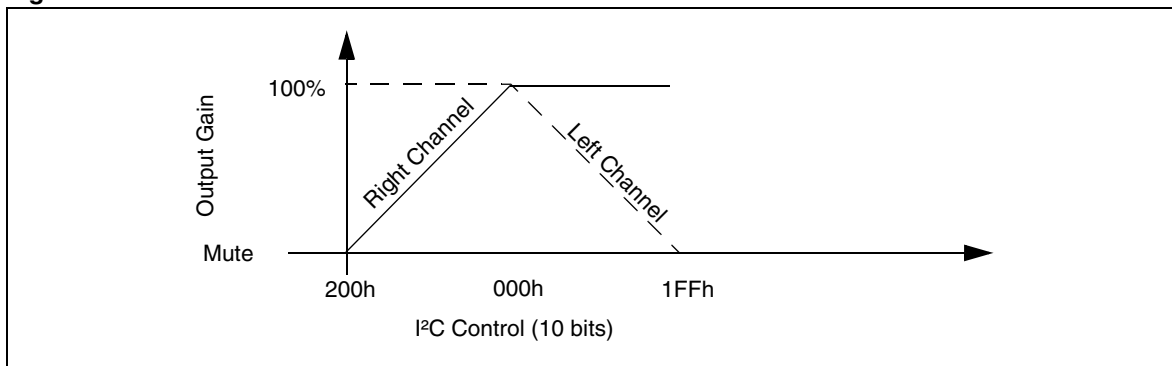
An extra master volume control can apply an extra gain/attenuation on L, R, C, L<sub>S</sub>, R<sub>S</sub> and SubW channels.

The volume/balance control can operate in one of two different modes:

In **Differential mode** (default value), the volume control is a common volume value for both the left and right loudspeakers or headphone channels (see [Figure 15](#)) and complimentary balance control is used (see [Figure 16](#)).

In **Independent mode**, the volume for the left and right channels for loudspeakers or headphone is controlled independently.

**Figure 16. Differential balance**



*Note: Each step is 0.25 dB*



## 5.21 Soft mute control

The digital soft mute is applied smoothly (20 ms for 120 dB range) to avoid any switch noise on output. It is available on all output channels pairs:

- S/PDIF channel (left/right)
- SCART channels (left/right)
- Loudspeakers channels (left/right)
- Center
- Subwoofer
- Headphone/Surround channels (left/right)

Another soft mute (analog) is also available on each DAC output.

## 5.22 Beeper

The beeper is used to generate a tone on the loudspeakers or headphone outputs or both. The beeper sound (square wave) is added to the audio signal which is attenuated by 20 dB. The beep sound amplitude includes a smooth attack and decay to avoid any parasitic noise when starting and stopping.

It can be used for various applications such as beep sounds for remote control, alarm clock or other features.

The beeper operates in one of two modes:

- **Pulse mode** (beep applications): A tone with a programmable short duration (0.1, 0.25, 0.5 and 1.0 s) is generated. Afterwards, the beeper is automatically disabled and the output is switched back to the audio signal, see [Figure 17](#).
- **Continuous mode** (alarm application): A tone with a programmable long duration is generated. Its start and stop controls must be programmed by I<sup>2</sup>C, see [Figure 18](#).

The Beeper function is enabled by setting the BEEPER\_ON bit in register [BEEPER\\_ON](#).

Beeper parameters are controlled in register [BEEPER\\_MODE](#).

The beeper tone level and frequency are programmed in register [BEEPER\\_FREQ\\_VOL](#). The level (or volume) ranges between 0 dB and -93 dB in steps of 3 dB and the tone frequency ranges between 62.5 Hz and 8 kHz in steps of 1 octave.

A beep generator is shared only by the loudspeakers or headphone outputs. Therefore, in the event of simultaneous beeps when in pulse mode, only the first beep will define the effective duration that will be the same for both outputs.

Figure 17. Pulse mode

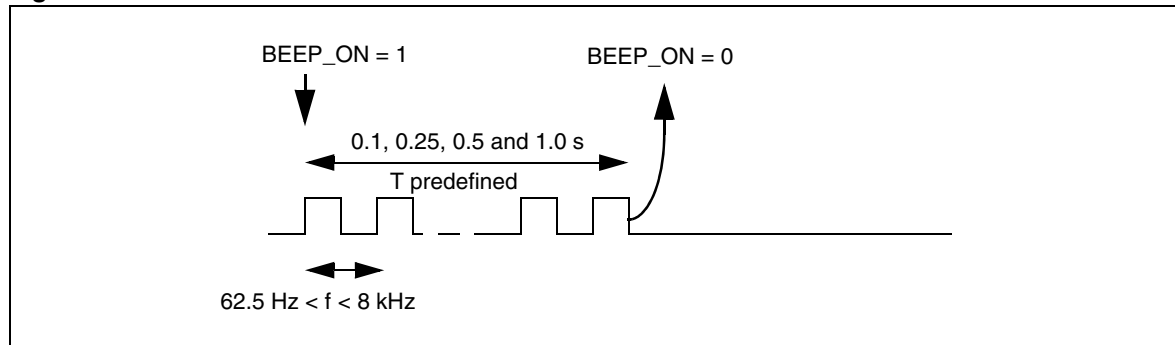
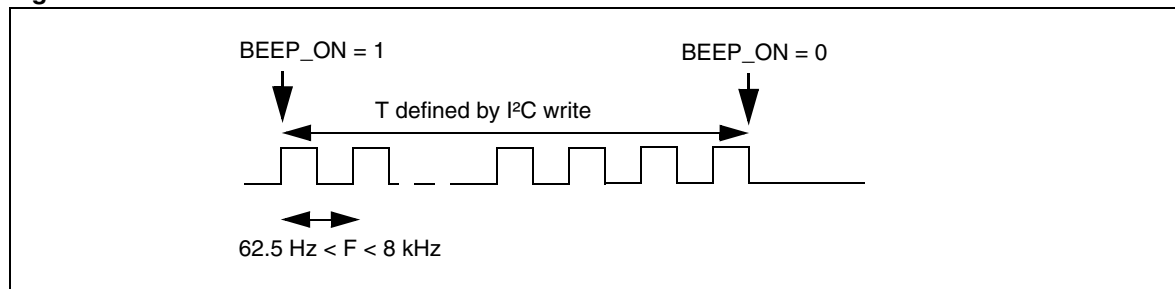


Figure 18. Continuous mode



### 5.23 Internal audio/video delay (lip sync)

Since increasing processing on the video signal implies more delay compared to the audio signal, there is a possibility inside the device of compensating by inserting a delay on the audio path in order to resynchronize the two signals:

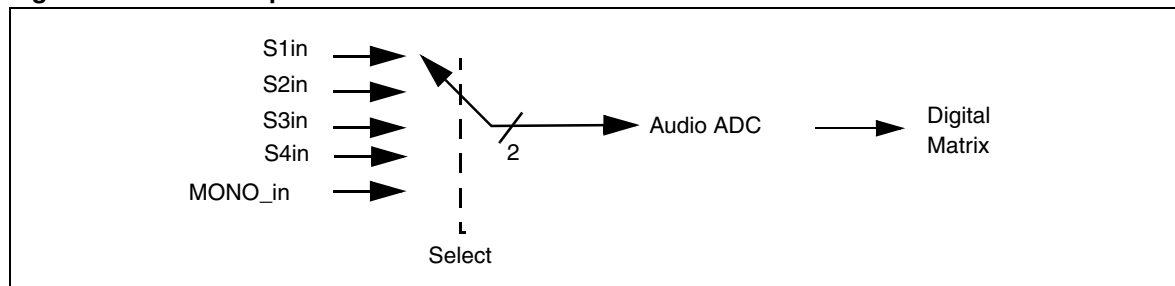
- 60ms with 48 KHz sampling frequency (SCART only input mode)
- 90ms with 32 KHz sampling frequency (demodulator input mode)

The same delay is available for the LS or HP path or both.

### 5.24 Analog audio matrix (input/output)

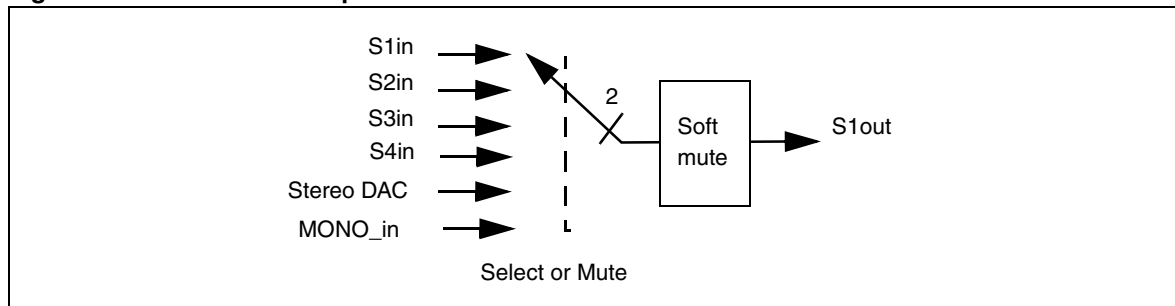
The analog part of the audio matrix can be divided into two parts: the SCART input matrix and the SCART output matrix.

Figure 19. SCART input matrix



The SCART input matrix is an input for the digital matrix (after the ADC) which select which source will be sent to the DSP.

**Figure 20. SCART1/2/3 output matrix**



The SCART output matrix selects the sound to output, which can be directly a SCART input or the output of the DSP. A mute function is provided to switch off the outputs.

A soft-mute function is provided to avoid all spurious sounds when switching from one position to another position.

The SCART 2 and 3 output matrices have the same functions as the SCART 1 output matrix.

The particularity of the matrix is to accept input signal of  $2 V_{RMS}$  and to have the capability to output such level. In this case, the power supply must be 8 V.

*Note: The mono audio input is able to accept signals with a  $0.5 V_{RMS}$  amplitude.*

## 6 I<sup>2</sup>S interface (input/output)

The STV82x7 offers three input/output choices: one I<sup>2</sup>S input, three I<sup>2</sup>S inputs or one I<sup>2</sup>S output.

### 6.1 I<sup>2</sup>S inputs

The STV82x7 can interface with a digital sound decoder. In this case, the digital data can be input at a speed of 0.384 Mbytes/s (3.072 MHz for a 48 kHz sampling frequency with 32 bits of data). In compliance with Dolby<sup>®</sup> specifications, only the sampling frequency is subject to restrictions. All other requirements are extracted from other various specifications

**Table 4. I<sup>2</sup>S characteristics**

Sampling frequency (kHz)	8, 11.025, 12,16, 22.05, 24, 32, 44.1 and 48
Data size	16, 18*, 20*, 24*, 32
PCMCLK	1. $512 \times f_s^{(1) (2)}$

1. Means that the number is the number of effective bits but the transmission is with 32 bits.

2.  $512 \times f_s$  is used by the DACs if  $512 \times f_s$  is present.

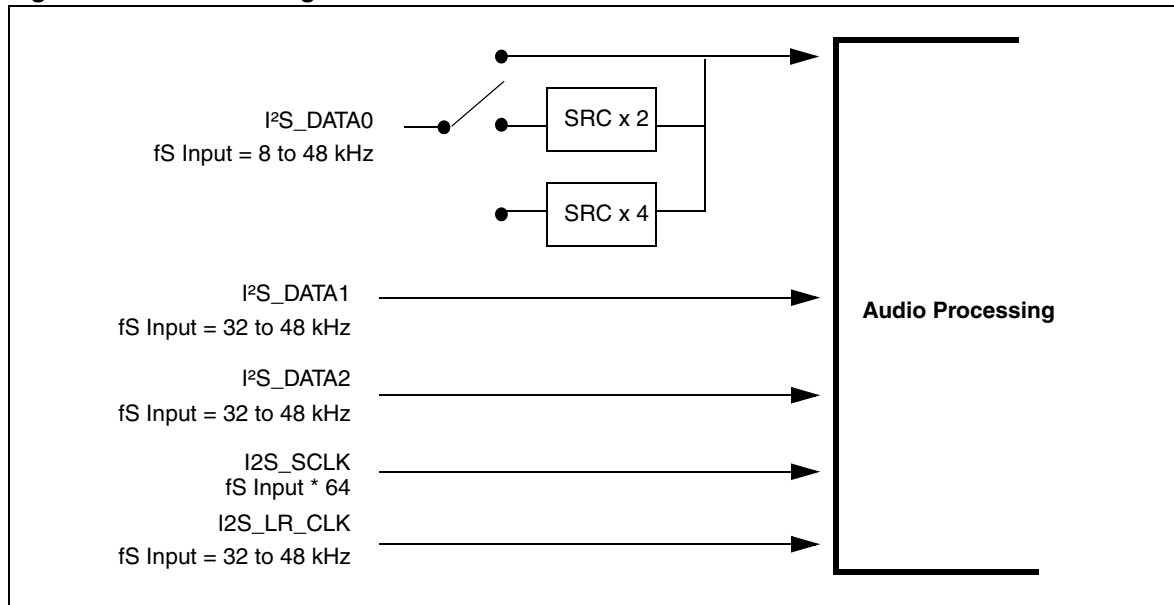
The PCMCLK (possible clock for upsampling) is provided by the master which is the digital sound decoder. A sample rate conversion (SRC) will be necessary in the second case (STV82x7 slave) in order to have a fixed frequency output from this block (either 32 kHz, 44.1 kHz or 48 kHz).

*Note:* The SRC function is only available in single I<sup>2</sup>S input mode.

The I<sup>2</sup>S interface is used in two ways depending on the package:

1. The interface with one I<sup>2</sup>S (I<sup>2</sup>S\_DATA0) connection (only stereo or stereo-coded Dolby<sup>®</sup> Pro Logic<sup>®</sup>);
2. One interface with three I<sup>2</sup>S connections connected to the DSP to allow the processing of a multi-channel signal (maximum of 6 channels).

Figure 21. I<sup>2</sup>S block diagram



- Note:
- 1 The I<sup>2</sup>S input and output modes are exclusive (this means that the I2S\_DATA0 can be used as input or as output).
  - 2 Simultaneous processing of I<sup>2</sup>S inputs and SIF inputs and/or ADC inputs (SCART or MONO inputs) is NOT possible with the device.
  - 3 I2S\_PCM\_CLK is not needed for the device

Table 5. I<sup>2</sup>S frequency configuration

I <sup>2</sup> S (max. number of channels)	f <sub>S</sub> input (kHz)	f <sub>S</sub> output (kHz) after SRC	SRC use
1 (I <sup>2</sup> S_DATA0)	8	32.0	x 4
1 (I <sup>2</sup> S_DATA0)	16	32.0	x 2
3	32	32.0	No
1 (I <sup>2</sup> S_DATA0)	11.025	44.1	x 4
1 (I <sup>2</sup> S_DATA0)	22.05	44.1	x 2
3	44.1	44.1	No
1 (I <sup>2</sup> S_DATA0)	12	48.0	x 4
1 (I <sup>2</sup> S_DATA0)	24	48.0	x 2
3	48	48.0	No

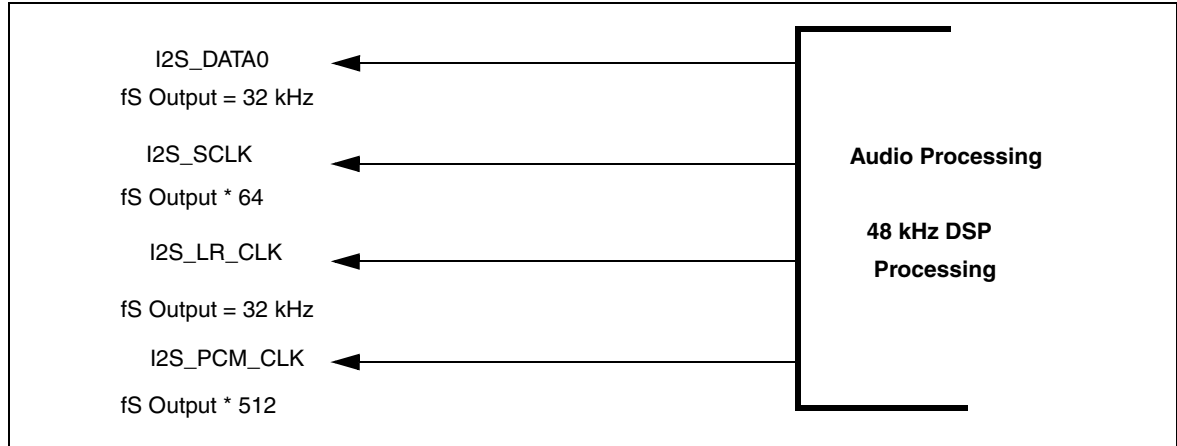
Both standard and non-standard modes are available, see [Figure 24](#)

## 6.2 I<sup>2</sup>S output

A digital stereo output (I<sup>2</sup>S compatible) is also available for routing the demodulated signal or a converted input audio signal to an external device. In this case, the I2S\_DATA0 signal and all clock signals are set as outputs by setting bit D6 in register RESET to 1.

The STV82x7 I<sup>2</sup>S drives the serial bus (SCLK, LR\_CLK, I<sup>2</sup>S\_DATA0) in master mode in 64.fs format with a sampling frequency ( $f_s$ ) of 32 kHz. The I<sup>2</sup>S\_PCM\_CLK signal can be used as a master clock in 512.fs format if required for the slave interface. Both standard and non-standard modes are available, see [Figure 24](#).

**Figure 22. TQFP 80 I<sup>2</sup>S output block diagram**



*Note:* The I<sup>2</sup>S input and output modes are exclusive (this means that the I2S\_DATA0 can be used as input or as output)

**Figure 23. I<sup>2</sup>S output selection**

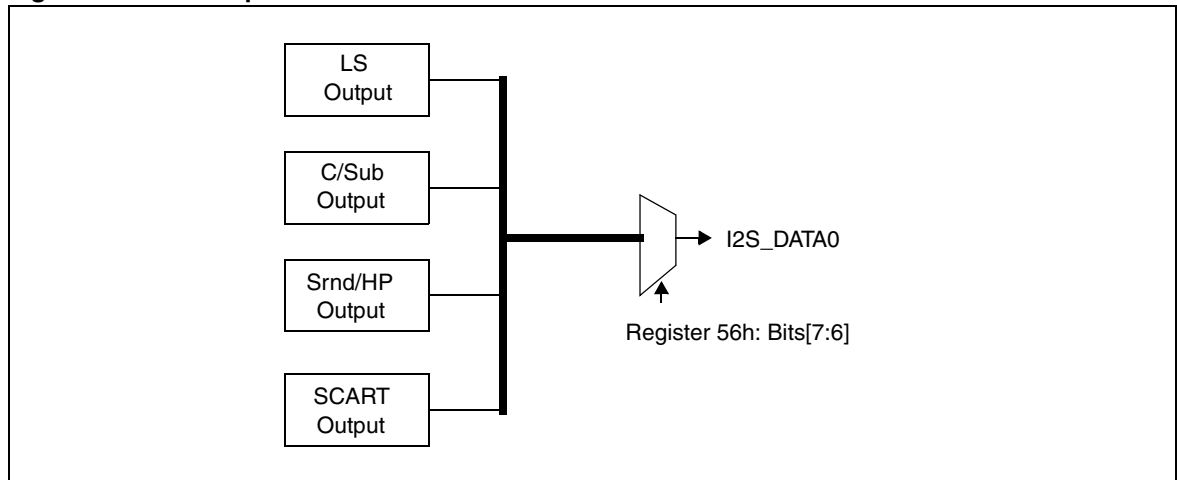
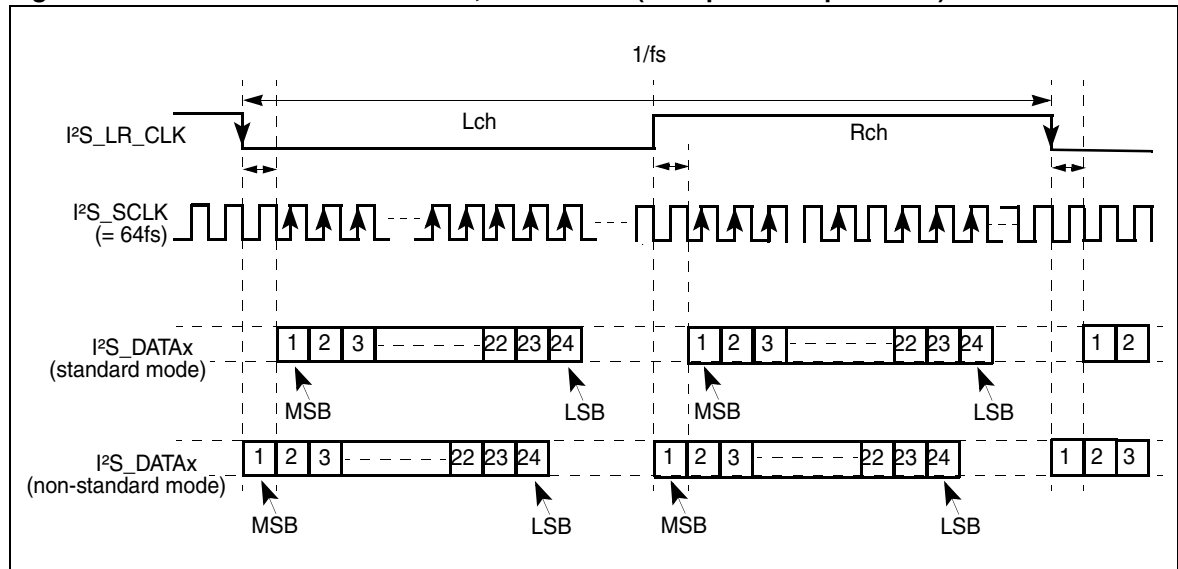


Figure 24. I<sup>2</sup>S data format: Lch = LOW, Rch = HIGH (I<sup>2</sup>S input or output mode)



## 7 S/PDIF input/output

An S/PDIF output is available for connection with an external A/V decoder/amplifier.

The signal on this S/PDIF output is selected by an on chip multiplexer between the internal signal and an external signal present on S/PDIF bypass input (Pin 44) with SPDIF\_MUX bit in the DAC\_CONTROL register.

The outputted internal signal can be selected from:

- L/R
- C/Subwoofer
- HP or surround L/R
- SCART L/R

The external signal is for example the signal provided by an external Dolby<sup>®</sup> Digital decoder (STD2000).

Mute facility is also provided on the S/PDIF output.

*Note: The S/PDIF\_IN pin (pin 44) is a CMOS digital pin and input signals on this pin must fulfill the characteristics as mentioned in [Section 17.12: Digital I/Os characteristics on page 160](#) ( $\pm 0.5 V_{PP}$  standard S/PDIF input level is not directly supported by the device and needs external circuitry).*



## 8 Power supply management

A mixed supply voltage environment requires the following voltages:

- 3.3 V capable inputs/outputs for digital pins;
- 1.8 V digital core;
- 8 V capable inputs/outputs for analog audio interfaces (capability to output 2 V<sub>RMS</sub> for SCART requirements);
- 3.3 V for stereo ADC and DAC (analog part);
- 1.8 V for stereo ADC and DAC (digital part);
- 1.8 V for IF ADC and AGC.

These voltages will be delivered by the application with an accuracy of  $\pm 5\%$ . For more information, refer to [Section 17.3: Power supply data](#).

Other specific DC voltages or features are provided:

- Voltage reference and biasing generation (AGC, ADCs, DACs),
- Bandgap reference.

### 8.1 Standby mode (loop-through mode)

The STV82x7 provides a loop-through mode configuration that bypasses IC functions via a SCART I/O pin (full analog path only). In this case, only a minimum power of 200 mW is required.

In standby mode, the digital and analog power supplies are switched off, except for pins VCC\_H, VCC33\_LS, VCC33\_SC, and VCC\_NISO which are used to maintain the SCART path with the last configuration programmed by analog matrixing (register [SCART1\\_2\\_OUTPUT\\_CTRL](#) and [SCART3\\_OUTPUT\\_CTRL](#)). When switching back to normal Full Power mode, all I<sup>2</sup>C registers are reset except for those used in Standby mode to maintain the original configuration.

In standby mode, the I<sup>2</sup>C bus does not operate. However, the bus can still be used by other ICs since the I<sup>2</sup>C I/O pins (SDA and SCL) of the STV82x7 are forced into a high-impedance configuration.

### 8.2 Power on reset

The following supply voltages are involved for power on reset for the STV82x7:

- for 1.8 V: VDD18 on pins 38, 42, 50 and 66, VCC18\_CLK1 on pin 54 and VCC18\_CLK2 on pin 57.
- for 3.3 V: VDD33\_IO1 on pin 46 and VDD33\_IO2 on pin 59.

The first condition for a valid reset is that all 1.8 V supply voltages involved have reached a minimum valid voltage of 1.7 V and that all 3.3 V supply voltages involved have reached a minimum valid voltage of 3.1 V. When this is the case and starting from this point, the reset must be maintained at a low level (<1 V) for at least 100  $\mu$ s then put to a high level.

## 9 Additional controls and flag

This logic contains:

- the headphone detection,
- the IRQ generation, signal to be output to the MCU,
- the I<sup>2</sup>C bus expander output pin.

### 9.1 Headphone detection

For headphone, the  $\overline{\text{HP\_DET}}$  input can be used to automatically mute the loudspeakers and subwoofer outputs when the HP\_LS\_MUTE bit is set in register [HEADPHONE\\_CONFIG](#) (active low). When a headphone is detected (the  $\overline{\text{HP\_DET}}$  pin is set to 0) and the mute function is enabled. Each change on the  $\overline{\text{HP\_DET}}$  pin generates an IRQ request to the microprocessor on the IRQ pin.

### 9.2 IRQ generation

Four IRQs are generated by the STV82x7. On each IRQ generation, the IRQ pin is set to 1. The pending IRQ status must be read at the I<sup>2</sup>S address 81h and the acknowledge is done by writing 0 to this register.

The four available IRQs are:

**IRQ0:** The identified TV sound standard is displayed in register [AUTOSTD\\_STATUS](#). Each change in the detected standard is flagged to the host system via hardware pin IRQ. The flag must be reset by re-programming the IRQ bit in register [AUTOSTD\\_CTRL](#) and then checking the detected standard status by reading registers [AUTOSTD\\_STATUS](#), [NICAM\\_STAT](#), and [ZWT\\_STAT](#).

**IRQ1:** This IRQ is enabled only in digital input mode. In case of I<sup>2</sup>S synchronisation loss, this IRQ is set to 1.

**IRQ2:** This IRQ is set to 1 when the device detects any change on the HP detection pin (headphone connection or disconnection).

**IRQ3:** On the STV82x7, same pins are used for both headphone and surround loudspeaker signal output. A change in the Headphone configuration (HP active or not active) will lead to a signal switch on those hardware pins. In order to ensure a smooth audio transition, the output is soft muted before the signal is switched. The IRQ3 is then set to 1 to advise the master processor that the signal has been switched and to request a HP/Srnd output un-mute.

#### 9.2.1 I<sup>2</sup>C bus expander

Pin BUS\_EXP can be used to control external switchable IF SAW filters or audio switches. This pin can be directly programmed by register [RESET](#).

## 10 STV82x7 reset

All STV82x7 features are controlled via the I<sup>2</sup>C bus.

The STV82x7 can be "reset" in 2 ways:

1. By software via the I<sup>2</sup>C bus: This clears all synchronous logic, except for the I<sup>2</sup>C bus registers.
2. By hardware via the RESET pin: In addition to clearing all synchronous logic, the RESET input (active on the low level) resets all the I<sup>2</sup>C bus registers to the *default values* listed below.

**Table 6. RESET default values**

Function	Default mode
<b>Demodulation</b>	
Auto-standard	ON
Scanned standards	M/N, B/G, I, L/L'
FM deviation	± 125 kHz (Max.)
<b>Audio outputs</b>	
Automatic mte mode	ON
Loudspeaker source	Demodulated sound
Loudspeaker volume	-40 dB, differential mode, muted
Loudspeaker L/R balance	L/R = 100%
Subwoofer	-40 dB / OFF
Headphone source	Demodulated sound
Headphone automatic detection	ON
Headphone volume	-40 dB, differential mode, muted
Headphone L/R balance	L/R = 100%
SCART-1 out	Demodulated sound
SCART-2 out	SCART1 source
SCART volume	-5.5 dB, independent mode, muted
I <sup>2</sup> S out	OFF
<b>Audio processing</b>	
Loudspeaker/Headphone SVC	OFF, 0 dB reference value
Loudspeaker surround	OFF
Loudspeaker 5-band equalizer	OFF, 0 dB (flatband)
Loudspeaker loudness	OFF
Headphone bass/treble	OFF, 0 dB (flat band)
Loudspeaker/Headphone beeper	-40 dB / OFF

## 11 I<sup>2</sup>C interface

### 11.1 I<sup>2</sup>C address and protocol

The STV82x7 I<sup>2</sup>C interface works in Slave mode and is fully compliant with I<sup>2</sup>C standards in Fast mode (maximum frequency of 400 kHz). Two pairs of I<sup>2</sup>C chip addresses are used to connect two STV82x7 chips to the same I<sup>2</sup>C serial bus. The device address pairs are defined by the polarity of the ADR\_SEL pin and are listed in the following table:

**Table 7. I<sup>2</sup>C Read/Write addresses**

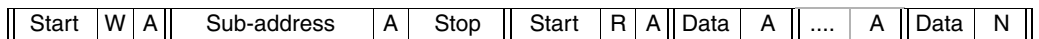
ADR	Write address (W)	Read address (R)
LOW (connected to GND1)	80h	81h
HIGH (connected to VDD1)	84h	85h

#### Protocol description

- Write protocol



- Read protocol



- W = Write address
- R = Read address
- A = Acknowledge
- N = No acknowledgement
- Sub-address is the register address pointer; this value auto-increments for both write and read.

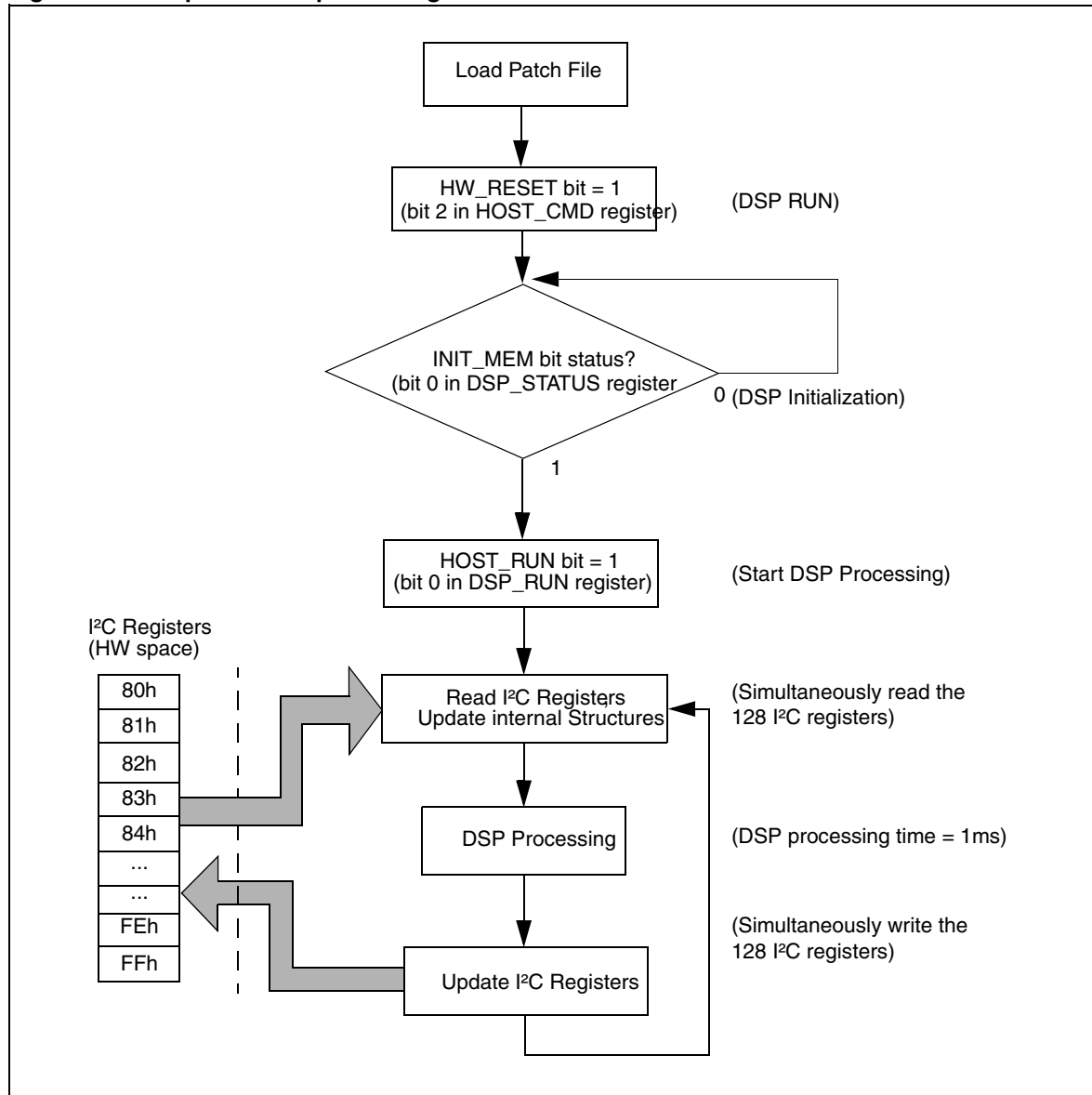
### 11.2 Start-up and configuration change procedure

The DSP running loop is:

- Read I<sup>2</sup>C registers and update internal structures (memory variables)
- Process sound samples
- Write I<sup>2</sup>C registers with new updated values

The step “process sound sample” duration is **1ms**. This is shown in [Figure 25](#).

Figure 25. Simplified DSP processing flow

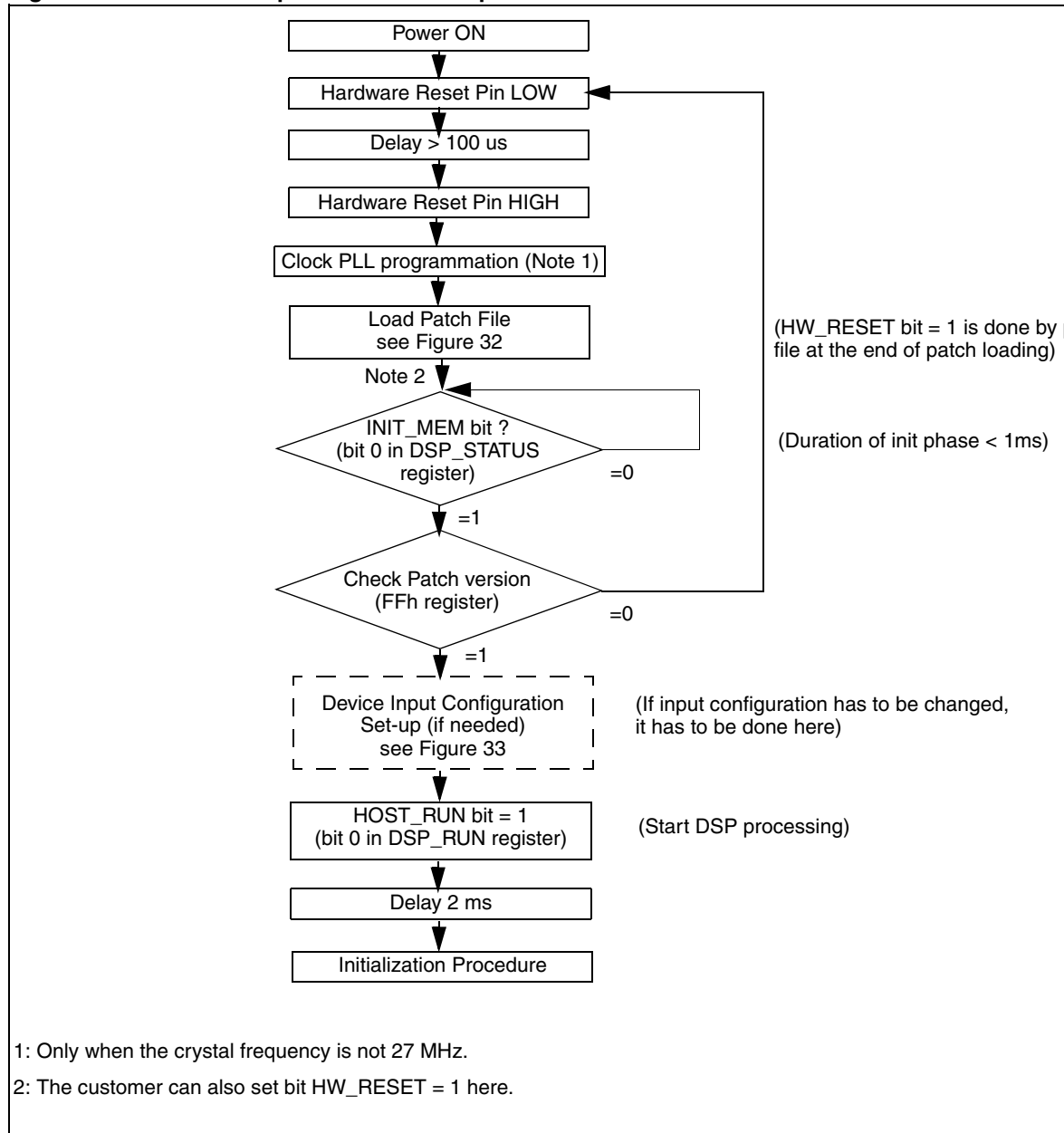


When programming I<sup>2</sup>C read/write register with addresses between 80h and FFh this flow has to be taken into account.

For example, if two different values are written in the **same** register in less than 2 ms, it is possible that the DSP doesn't see the first value (because the second value over-writes the first one during the "DSP processing" phase, before DSP can read the registers again).

In the same way, when waiting for a register value change, the software programme must wait for at least 2 ms in order to allow sufficient time for the DSP to update the register values.

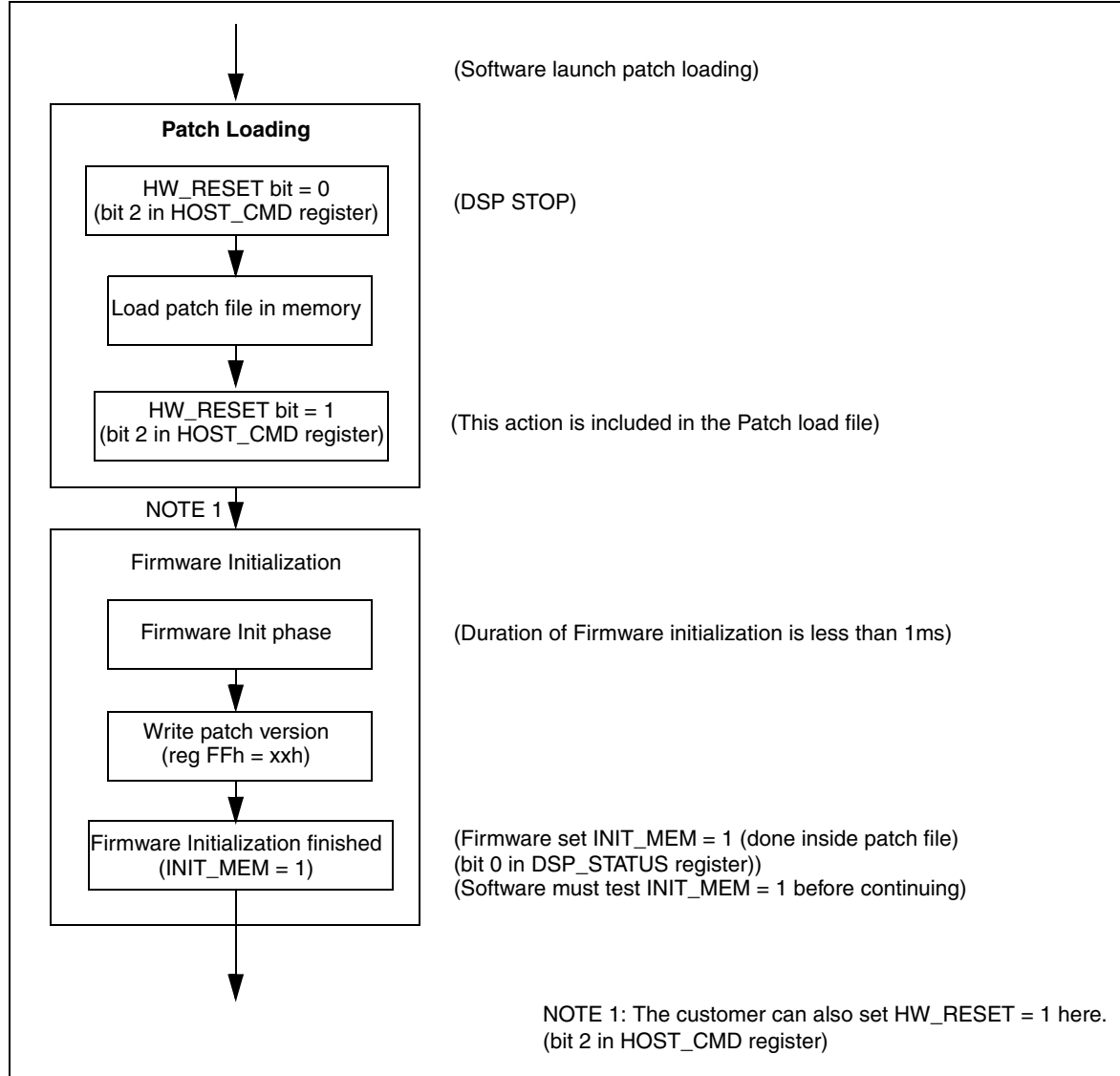
Figure 26. Initialization procedure at sartup



### 11.3 Process flow during patch loading and DSP initialization

Patch loading and DSP firmware initialization are shown in [Figure 27](#)

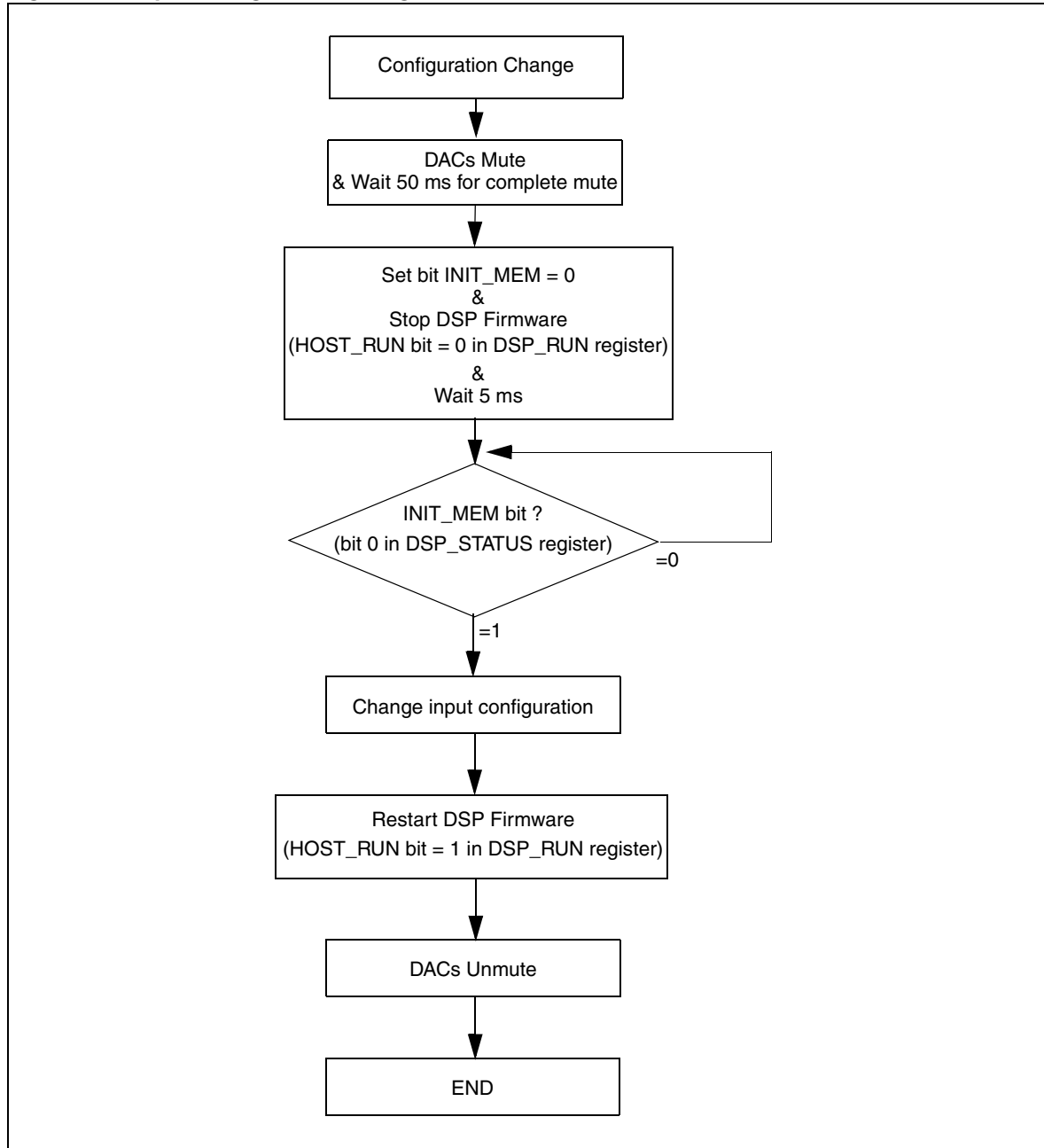
**Figure 27. Patch loading and DSP initialization**



## 11.4 Input configuration change

The input configuration change must be programmed as shown in [Figure 28](#):

**Figure 28. Input configuration change**





## 12 Register list

*Note:* The unused bits (defined as 'Reserved') in the I<sup>2</sup>C registers must be kept to zero.

The system clock registers (from address 0x08 to 0x0B and from address 0x5A to 0x5D) do not need to be modified if a standard 27 MHz quartz crystal oscillator is used.

The default values of the demodulator registers (from address 0x0C to 0x55) are for optimum performances and any change is not recommended, except for:

- **AGC\_GAIN** (0x0F) to adjust AGC gain for AM carrier in L/L' standard (AGC used in open loop).
- **CAROFFSET1** (0x22) and **CAROFFSET2** (0x3A) to compensate IF carrier frequency with an out-of-standard offset.
- Soundlevel Prescaling **PRESCALE\_AM** (0x94), **PRESCALE\_FM** (0x95), **PRESCALE\_NICAM** (0x96) and **PRESCALE\_SCART** (0x97) to equalize demodulated or external audio signal before audio processing. Peak detector registers **PEAK\_DET\_INPUT** (0x9D), **PEAK\_DET\_L** (0x9E), **PEAK\_DET\_R** (0x9F), **PEAK\_DET\_L\_R** (0xA0) can be used to measure internal sound level.

Sound source selection for each audio output channel Loudspeakers, Headphone and SCART to be done using **AUDIO\_MATRIX\_INPUT** (0xA2).

In multilingual mode, **AUDIO\_MATRIX\_LANGUAGE** (0xA4) selects separately the language for each audio output channel.

Register **AUTOSTD\_CTRL** (0x8A) is used to select between L/L' or D/K/K1/K2/K3 standard which can be discriminated automatically. To be used also to change maximum FM deviation (125 kHz, by default) in case of wide overmodulation.

**AUTOSTD\_STANDARD\_DETECT** (0x8B) and **AUTOSTD\_STEREO\_DETECT** (0x8C) to define the list of mono and stereo standards to be recognized automatically.

*Note:* ( ) used in reset value column means that the bit or the byte is read-only.  
 (S) symbol indicates that the field value is represented in signed binary format.  
 (\*) The field **AGC\_ERR[4:0]** (**AGC\_GAIN**) can be written by user if the bit **AGC\_CMD** (**AGC\_CTRL**) is set to one (by default controlled by Automatic Standard Recognition System). To be used to adjust manually the input gain of analog AGC amplifier for AM carrier (L/L').

## 12.1 I<sup>2</sup>C register map

By default, all I<sup>2</sup>C registers controlled by Automatic Standard Recognition System (Autostandard) are forced to read-only mode for the user. These registers and bits are shaded in [Table 8](#).

**Table 8. List of I<sup>2</sup>C registers**

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------

### IC general control

<i>CUT_ID</i>	0x00	(0000 0001)	0	0	CUT_NUMBER[5:0]					
<i>RESET</i>	0x01	0000 0000	BUS_EX P	I <sup>2</sup> S_OUT PUT	0	EN_STB Y	0	SOFT_ LRST2	SOFT_ LRST1	SOFT_ R ST
<i>I2S_CTRL</i>	0x04	0000 0000	SYNC_O FF	SYNC_SI GN	0	LOCK_TH[1:0]		LOCK_M ODE	SYNC_CST[1:0]	
<i>I2S_STAT</i>	0x05	(0000 0000)	0	0	0	0	0	0	LR_OFF	LOCK_ FLAG
<i>I2S_SYNC_OFFSET</i>	0x06	0000 0000	I2S_SFO[7:0]							

### Clocking 1

<i>SYS_CONFIG</i>	0x07	0000 0000	I2S_CH_NB[1:0]		INPUT_FREQ[3:0]			INPUT_CONFIG[1:0]		
<i>FS1_DIV</i>	0x08	0001 0010	EN_PRO G	0	NDIV1[1:0]		0	SDIV1[2:0]		
<i>FS1_MD</i>	0x09	0001 0001	0	0	0	MD1[4:0]				
<i>FS1_PE_H</i>	0x0A	0011 0110	PE_H1[7:0]							
<i>FS1_PE_L</i>	0x0B	0000 0000	PE_L1[7:0]							

### Demodulator

<i>DEMOD_CTRL</i>	0x0C	0000 0110	0	0	FAR_MO DE	GAP_MO DE	AM_SEL	DEMOD_MODE[2:0]		
<i>DEMOD_STAT</i>	0x0D	(0000 0000)	0	0	0	QPSK_L K	FM2_CA R	FM2_SQ	FM1_CA R	FM1_SQ
<i>AGC_CTRL</i>	0x0E	0001 0001	AGC_ CMD	0	0	AGC_REF[2:0]			AGC_CST[1:0]	
<i>AGC_GAIN</i>	0x0F	(0000 0000)	0	AGC_ERR[4:0]					SIG_OVE R	SIG_ UNDER
<i>DC_ERR_IF</i>	0x10	(0000 0000)	DC_ERR[7:0]							

### Demodulator channel 1

<i>CARFQ1H</i>	0x12	0011 1110	CARFQ1[23:16]							
<i>CARFQ1M</i>	0x13	1000 0000	CARFQ1[15:8]							
<i>CARFQ1L</i>	0x14	0000 0000	CARFQ1[7:0]							
FIR1C0	0x15	0000 0000	FIR1C0[7:0] (S)							

**Table 8. List of I<sup>2</sup>C registers (continued)**

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIR1C1	0x16	1111 1110	FIR1C1[7:0] (S)							
FIR1C2	0x17	1111 1100	FIR1C2[7:0] (S)							
FIR1C3	0x18	1111 1101	FIR1C3[7:0] (S)							
FIR1C4	0x19	0000 0010	FIR1C4[7:0] (S)							
FIR1C5	0x1A	0000 1101	FIR1C5[7:0] (S)							
FIR1C6	0x1B	0001 1000	FIR1C6[7:0]6 (S)							
FIR1C7	0x1C	0001 1111	FIR1C7[7:0] (S)							
<i>ACOEFF1</i>	0x1D	0010 0011	ACOEFF1[7:0]							
<i>BCOEFF1</i>	0x1E	0001 0010	BCOEFF1[7:0]							
<i>CRF1</i>	0x1F	(0000 0000)	CRF1[7:0] (S)							
<i>CETH1</i>	0x20	0010 0000	CETH1[7:0]							
<i>SQTH1</i>	0x21	0011 1100	SQTH1[7:0]							
<i>CAROFFSET1</i>	0x22	0000 0000	CAROFFSET1[7:0] (S)							

**Demodulator channel 2**

<i>IAGCR</i>	0x25	1000 1000	IAGC_REF[7:0]							
<i>IAGCC</i>	0x26	0000 0011	IAGC_OFF	FAR_FLT_EN	MONO_FLT_EN	BG_SEL	MONO_PROG	IAGC_CST[2:0]		
<i>IAGCS</i>	0x27	(0000 0000)	IAGC_CTRL[7:0]							
CARFQ2H	0x28	0100 0100	CARFQ2[23:16]							
CARFQ2M	0x29	0100 0000	CARFQ2[15:8]							
CARFQ2L	0x2A	0000 0000	CARFQ2[7:0]							
FIR2C0	0x2B	0000 0000	FIR2C0[7:0] (S)							
FIR2C1	0x2C	0000 0000	FIR2C1[7:0] (S)							
FIR2C2	0x2D	0000 0000	FIR2C2[7:0] (S)							
FIR2C3	0x2E	0000 0000	FIR2C3[7:0] (S)							
FIR2C4	0x2F	1111 1111	FIR2C4[7:0] (S)							
FIR2C5	0x30	0000 0100	FIR2C5[7:0] (S)							

Table 8. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIR2C6	0x31	0001 0100	FIR2C6[7:0] (S)							
FIR2C7	0x32	0010 0101	FIR2C7[7:0] (S)							
<i>ACOEFF2</i>	0x33	1001 0000	ACOEFF2[7:0]							
<i>BCOEFF2</i>	0x34	1010 1100	BCOEFF2[7:0]							
<i>SCOEFF</i>	0x35	0001 1100	SCOEFF[7:0]							
<i>SRF</i>	0x36	(0000 0000)	SRF[7:0] (S)							
<i>CRF2</i>	0x37	(0000 0000)	CRF2[7:0] (S)							
<i>CAROFFSET2</i>	0x3A	0000 0000	CAROFFSET2[7:0] (S)							

**NICAM**

<i>NICAM_CTRL</i>	0x3D	0000 0000	0	0	0	0	0	DIF_POL	ECT	MAE
<i>NICAM_BER</i>	0x3E	(0000 0000)	ERROR[7:0]							
<i>NICAM_STAT</i>	0x3F	(0000 0000)	NIC_DET	F_MUTE	LOA	CBI[3:0]			NIC_MU TE	

**Stereo FM**

<i>ZWT_CTRL</i>	0x40	0011 0001	LRST_ TONE_O FF	STD_MO DE	THRESH[3:0]			TSCTRL[1:0]		
<i>ZWT_TIME</i>	0x41	0000 0100	0	0	0	0	0	ZWT_TIME[2:0]		
<i>ZWT_STAT</i>	0x42	(0000 0000)	0	0	0	0	ZW_STA T_ RDY	ZW_DET	ZW_ST	ZW_DM

**Analog control**

<i>ADC_CTRL</i>	0x56	0000 1000	I2S_DATA0_CTRL[1: 0]		0	0	ADC_ POWER_ UP	ADC_INPUT_SEL[2:0]		
<i>SCART1_2_OUTPUT_CTRL</i>	0x57	1010 1000	SC2_MU TE	SC2_OUTPUT_SEL[2:0]			SC1_MU TE	SC1_OUTPUT_SEL[2:0]		
<i>SCART3_OUTPUT_CTRL</i>	0x58	0000 1011	0	0	0	0	SC3_MU TE	SC3_OUTPUT_SEL[2:0]		

**Clocking 2**

<i>FS2_DIV</i>	0x5A	0001 0001	0	NDIV2[1:0]			0	SDIV2[2:0]		
<i>FS2_MD</i>	0x5B	0001 0001	0	0	0	MD2[4:0]				
<i>FS2_PE_H</i>	0x5C	0101 1100	PE_H2[7:0]							
<i>FS2_PE_L</i>	0x5D	0010 1001	PE_L2[7:0]							

**DSP control**

Table 8. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
<i>HOST_CMD</i>	0x80	0000 0000	IT_IN_D SP	0	0	0	0	HW_RES ET	0	0	
<i>IRQ_STATUS</i>	0x81	0000 0000	0	0	0	0	IRQ3 (HP/Srmd unmute ready)	IRQ2 (HP detected)	IRQ1 (I2S sync lost)	IRQ0 (autostd)	
<i>SOFT_VERSION</i>	0x82	(0000 0002)	SOFT_VERSION[7:0]								
<i>ONCHIP_ALGOS</i>	0x83	(0000 0000)	0	PRO_LO GIC_SEL ECT	NICAM	I2S_INP UT	TRUBAS S	TRU SURROU ND	PRO_LO GIC	MULTICH ANEL	
<i>DSP_STATUS</i>	0x84	0000 0000	0	0	0	0	0	0	0	INIT_ME M	
<i>DSP_RUN</i>	0x85	0000 0000	0	0	0	0	0	0	HOST_ NO_INIT	HOST_R UN	
<i>I2S_IN_CONFIG</i>	0x86	1000 1110	LOCK_ MODE_E N	0	SYNC	LRCLK_ START	LRCLK_ POLARIT Y	SCLK_ POLARIT Y	DATA_CF G	I2S_MO DE	
<i>AV_DELAY</i>	0x89	0000 0000	DELAY_TIME[6:0]								DELAY_ ON

## Automatic Standard Recognition System

<i>AUTOSTD_CTRL</i>	0x8A	0000 0001	0	0	0	FORCE_ SQUELC H	SINGLE_ SHOT	DK_DEV[1:0]		LDK_SW
<i>AUTOSTD_STANDARD_DE TECT</i>	0x8B	0010 1111	0	NICAM_ C4_OFF	NICAM_ GAP_MO DE	NICAM_ MONO_I N	LDK_SC K	I_SCK	BG_SCK	MN_SCK
<i>AUTOSTD_STEREO_DETE CT</i>	0x8C	0001 1111	LDK_ZW T3	LDK_ZW T2	LDK_SW T1	LDK_ NICAM	I_NICAM	BG_ZWT	BG_NIC AM	MN_ZWT
<i>AUTOSTD_TIMERS</i>	0x8D	1010 0100	FM_TIME[1:0]		NICAM_TIME[2:0]		ZWEITON_TIME[2:0]			
<i>AUTOSTD_STATUS</i>	0x8E	(0000 0000)	STEREO ID	STEREO OK	MONO_ OK	AUTOST D_ON	STEREO_SID[1:0]		MONO_SID[1:0]	

## Audio preprocessing &amp; selection

<i>DC_REMOVAL_INPUT</i>	0x90	0000 0111	0	0	0	0	0	DC_SCA RT	DC_NIC AM	DC_ DEMOD	
<i>DC_REMOVAL_L</i>	0x91	(0000 0000)	DC_REMOVAL_L[7:0] (S)								
<i>DC_REMOVAL_R</i>	0x92	(0000 0000)	DC_REMOVAL_R[7:0] (S)								
<i>PRESCALE_SELECT</i>	0x93	0000 0000	0	0	0	0	0	0	0	AM_FM_ SELECT	
<i>PRESCALE_AM</i>	0x94	0000 0000	0	PRESCALE_AM[6:0] (S)							
<i>PRESCALE_FM</i>	0x95	0000 1100	0	PRESCALE_FM[6:0] (S)							
<i>PRESCALE_NICAM</i>	0x96	0001 1010	0	PRESCALE_NICAM[6:0] (S)							
<i>PRESCALE_SCART</i>	0x97	0000 0000	0	0	PRESCALE_SCART[5:0] (S)						
<i>PRESCALE_I2S_0</i>	0x98	0000 0000	0	0	PRESCALE_I2S_0[5:0] (S)						

Table 8. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>PRESCALE_I2S_1</i>	0x99	0000 0000	0	0	PRESCALE_I2S_1[5:0] (S)					
<i>PRESCALE_I2S_2</i>	0x9A	0000 0000	0	0	PRESCALE_I2S_2[5:0] (S)					
<i>DEEMPHASIS_DEMATRIX</i>	0x9B	0000 0000	0	0	NICAM_ DEMATRIX	NICAM_ DEEMPH _BY PASS	FM_DEMATRIX[1:0]		FM_DEE MPH_BY PASS	FM_DEE MPH_S W
<i>PEAK_DET_INPUT</i>	0x9D	0000 0000	PEAK_ LOCATIO N	0	PEAK_L_R_RANGE				PEAK_DET_INPUT[ 1:0]	
<i>PEAK_DET_L</i>	0x9E	0(0000 0000)	OVERLO AD_L[7:0 ]	PEAK_L[6:0]						
<i>PEAK_DET_R</i>	0x9F	0(0000 0000)	OVERLO AD_R[7:0 ]	PEAK_R[6:0]						
<i>PEAK_DET_L_R</i>	0xA0	0(0000 0000)	OVERLO AD_L_R[ 7:0]	PEAK_L_R[6:0]						

**Matrixing**

<i>AUDIO_MATRIX_INPUT</i>	0xA2	0000 0000	0	0	0	0	0	SCART_ INPUT_ SOURCE	HP_INPU T_ SOURCE	LS_INPU T_ SOURCE
<i>AUDIO_MATRIX_CONFIG</i>	0xA3	0000 0000	0	0	0	SCART_ MATRIX	DEMOM_MATRIX[3:0]			
<i>AUDIO_MATRIX_LANGUAG E</i>	0xA4	0000 0000	MUTE_ STEREO	MUTE_ ALL	SCART_LANGUAGE [1:0]		HP_LANGUAGE[1:0]		LS_LANGUAGE[1:0]	
<i>DOWNMIX_IN_MODE</i>	0xA6	0000 0010	0	0	0	0	LFE_IN	MIX_IN_MODE[2:0]		
<i>DOWNMIX_OUT_MODE</i>	0xA7	0100 1010	0	HP_MODE[1:0]		SCART_MODE[1:0]		MIX_OUT_MODE[2:0]		
<i>DOWNMIX_DUAL_MODE</i>	0xA8	0000 0000	0	DUAL_O N	LS_DUAL_SELECT[ 1:0]		SCART_DUAL_SEL ECT [1:0]		HP_DUAL_SELECT[ 1:0]	
<i>DOWNMIX_CONFIG</i>	0xA9	0000 0001	0	0	SRND_FACTOR[1:0]		CENTER_FACTOR[1 :0]		LR_UPMI X	NORMAL IZE

**Audio processing**

<i>PRO_LOGIC2_CONTROL</i>	0xAA	0011 1010	PL2_LFE	PL2_OUTPUT_DOWNMIX[2:0]			PL2_MODES[2:0]		PL2_ACT IVE		
<i>PCM_SRND_DELAY</i>	0xAB	0000 0000	0	0	0	SNRD_DELAY[4:0]					
<i>PCM_CENTER_DELAY</i>	0xAC	0000 0000	0	0	0	0	CENTER_DELAY[3:0]				
<i>PRO_LOGIC2_CONFIG</i>	0xAD	0000 0000	0	0	0	PL2_SRND_FILTER		PL2_RS_ POLARIT Y	PL2_ PANORA MA	PL2_AUT O BALANC E	
<i>PRO_LOGIC2_DIMENSION</i>	0xAE	0000 0000	0	PL2_C_WIDTH			0	PL2_DIMENSION			
<i>PRO_LOGIC2_LEVEL</i>	0xAF	0000 0000	PL2_LEVEL								

Table 8. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>NOISE_GENERATOR</i>	0xB0	0000 0000	10_DB_ ATTENU ATE	SRIGHT_ NOISE	SLEFT_ NOISE	SUB_ NOISE	CENTER_ NOISE	RIGHT_ NOISE	LEFT_ NOISE	NOISE_ ON
<i>TRUSRND_CONTROL</i>	0xB1	0000 0000	0	TRUSRND_ MON O_ SRND	TRUSRND_INPUT_MODE[3:0]				TRUSRND_ MODE	TRUSRND_ ON
<i>TRUSRND_INPUT_GAIN</i>	0xB6	0000 0000	TRUSRND_INPUT_GAIN[7:0]							
<i>TRUSRND_HP_DCL</i>	0xB7	0000 0000	0	0	0	0	0	DIALOG_ CLARITY_ ON	HEADPH ONE_ON	0
<i>TRUSRND_DC_ELEVATION</i>	0xB8	0000 1100	TRUSRND_DC_ELEVATION[7:0]							
<i>TRUBASS_LS_CONTROL</i>	0xBA	0000 0110	0	0	0	TRUBASS_LS_SIZE[3:0]				TRUBASS_ S_ LS_ON
<i>TRUBASS_LS_LEVEL</i>	0xBB	00001 1001	TRUBASS_LS_LEVEL[7:0]							
<i>TRUBASS_HP_CONTROL</i>	0xBC	0000 0110	0	0	0	TRUBASS_HP_SIZE[3:0]				TRUBASS_ S_ HP_ON
<i>TRUBASS_HP_LEVEL</i>	0xBD	0000 1001	TRUBASS_HP_LEVEL[7:0]							
<i>SVC_LS_CONTROL</i>	0xBE	0000 0010	0	0	0	0	SVC_LS_INPUT[1:0]	SVC_ LS_AMP	SVC_ LS_ON	
<i>SVC_LS_TIME_TH</i>	0xBF	1001 1000	SVC_LS_TIME[2:0]			SVC_LS_THRESHOLD[4:0] (S)				
<i>SVC_HP_CONTROL</i>	0xC0	0000 0010	0	0	0	0	0	0	SVC_ LHP_AMP	SVC_ HP_ON
<i>SVC_HP_TIME_TH</i>	0xC1	1001 1000	SVC_HP_TIME[2:0]			SVC_HP_THRESHOLD[4:0] (S)				
<i>SVC_LS_GAIN</i>	0xC2	0000 0000	0	0	0	SVC_LS_MAKE_UP_GAIN[4:0]				
<i>SVC_HP_GAIN</i>	0xC3	0000 0000	0	0	0	SVC_HP_MAKE_UP_GAIN[4:0]				
<i>STSRND_CONTROL</i>	0xC4	0000 0000						STSRND_ STEREO	STSRND_ MODE	STSRND_ ON
<i>STSRND_FREQ</i>	0xC5	0001 0101	0	0	STSRND_BASS[1:0]	STSRND_MEDIUM[1: :0]	STSRND_TREBLE[1: :0]			
<i>STSRND_LEVEL</i>	0xC6	1000 0000	STSRND_GAIN[7:0]							
<i>OMNISURROUND_CONTR OL</i>	0xC7	0000 0000		ST_VOICE		OMNISURROUND_INPUT_MODE				OMNISUR ROUND_ON
<i>ST_DYNAMIC_BASS</i>	0xC8	0000 0000	BASS_LEVEL					BASS_FREQ		DYN_BA SS_ON
<i>LS_EQ_BT_CTRL</i>	0xC9	0000 0000	0	0	0	0	0	0	LS_EQ_ BT_ SW	LS_EQ_ ON
<i>LS_EQ_BAND1</i>	0xCA	0000 0000	EQ_BAND1[7:0] (S)							

Table 8. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_EQ_BAND2	0xCB	0000 0000	EQ_BAND2[7:0] (S)							
LS_EQ_BAND3	0xCC	0000 0000	EQ_BAND3[7:0] (S)							
LS_EQ_BAND4	0xCD	0000 0000	EQ_BAND4[7:0] (S)							
LS_EQ_BAND5	0xCE	0000 0000	EQ_BAND5[7:0] (S)							
<i>LS_BASS_GAIN</i>	0xCF	0000 0000	LS_BASS[7:0] (S)							
<i>LS_TREBLE_GAIN</i>	0xD0	0000 0000	LS_TREBLE[7:0] (S)							
<i>HP_BT_CONTROL</i>	0xD1	0000 0000	0	0	0	0	0	0	0	HP_BT_ON
<i>HP_BASS_GAIN</i>	0xD2	0000 0000	HP_BASS[7:0] (S)							
<i>HP_TREBLE_GAIN</i>	0xD3	0000 0000	HP_TREBLE[7:0] (S)							
<i>OUTPUT_BASS_MNGT</i>	0xD4	0000 0000	BASS_MANAGE_ON	0	SUB_ACTIVE	GAIN_SWITCH	0	OCFG_NUM[2:0]		
<i>LS_LOUDNESS</i>	0xD5	0000 0100	0	LS_LOUD_THRESHOLD[2:0]			LS_LOUD_GAIN_HR[2:0]			LS_LOUD_ON
<i>HP_LOUDNESS</i>	0xD6	0000 0100	0	HP_LOUD_THRESHOLD[2:0]			HP_LOUD_GAIN_HR[2:0]			HP_LOUD_ON

## Volume

<i>VOLUME_MODES</i>	0xD7	1100 0111	ANTCLIP_HP_VOL_CLAMP	ANTCLIP_LS_VOL_CLAMP	0	0	SCART_VOLUME_MODE	SRND_VOLUME_MODE	HP_VOLUME_MODE	LS_VOLUME_MODE
<i>LS_L_VOLUME_MSB</i>	0xD8	1001 1000	LS_L_VOLUME_MSB[7:0]							
<i>LS_L_VOLUME_LSB</i>	0xD9	0000 0000	0	0	0	0	0	0	LS_L_VOLUME_LSB[1:0]	
<i>LS_R_VOLUME_MSB</i>	0xDA	0000 0000	LS_R_VOLUME_MSB[7:0]							
<i>LS_R_VOLUME_LSB</i>	0xDB	0000 0000	0	0	0	0	0	0	LS_R_VOLUME_LSB[1:0]	
<i>LS_C_VOLUME_MSB</i>	0xDC	1001 1000	LS_C_VOLUME_MSB[7:0]							
<i>LS_C_VOLUME_LSB</i>	0xDD	0000 0000	0	0	0	0	0	0	LS_C_VOLUME_LSB[1:0]	
<i>LS_SUB_VOLUME_MSB</i>	0xDE	1001 1000	LS_SUB_VOLUME_MSB[7:0]							
<i>LS_SUB_VOLUME_LSB</i>	0xDF	0000 0000	0	0	0	0	0	0	LS_SUB_VOLUME_LSB[1:0]	
<i>LS_SL_VOLUME_MSB</i>	0xE0	1001 1000	LS_SL_VOLUME_MSB[7:0]							
<i>LS_SL_VOLUME_LSB</i>	0xE1	0000 0000	0	0	0	0	0	0	LS_SL_VOLUME_LSB[1:0]	



Table 8. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>LS_SR_VOLUME_MSB</i>	0xE2	0000 0000	LS_SR_VOLUME_MSB[7:0]							
<i>LS_SR_VOLUME_LSB</i>	0xE3	0000 0000	0	0	0	0	0	0	0	LS_SR_VOLUME_LSB[1:0]
<i>LS_MASTER_VOLUME_MSB</i>	0xE4	1110 1000	LS_MASTER_VOLUME_MSB[7:0]							
<i>LS_MASTER_VOLUME_LSB</i>	0xE5	0000 0000	0	0	0	0	0	0	0	LS_MASTER_VOLUME_LSB[1:0]
<i>HP_L_VOLUME_MSB</i>	0xE6	1001 1000	HP_L_VOLUME_MSB[7:0]							
<i>HP_L_VOLUME_LSB</i>	0xE7	0000 0000	0	0	0	0	0	0	0	HP_L_VOLUME_LSB[1:0]
<i>HP_R_VOLUME_MSB</i>	0xE8	0000 0000	HP_R_VOLUME_MSB[7:0]							
<i>HP_R_VOLUME_LSB</i>	0xE9	0000 0000	0	0	0	0	0	0	0	HP_R_VOLUME_LSB[1:0]
<i>SCART_L_VOLUME_MSB</i>	0xEA	1101 1101	SCART_L_VOLUME_MSB[7:0]							
<i>SCART_L_VOLUME_LSB</i>	0xEB	0000 0000	0	0	0	0	0	0	0	SCART_L_VOLUME_LSB[1:0]
<i>SCART_R_VOLUME_MSB</i>	0xEC	1101 1101	SCART_R_VOLUME_MSB[7:0]							
<i>SCART_R_VOLUME_LSB</i>	0xED	0000 0000	0	0	0	0	0	0	0	SCART_R_VOLUME_LSB[1:0]

**Beeper**

<i>BEEPER_ON</i>	0xEE	0000 0000	0	0	0	0	0	0	0	BEEPER_ON
<i>BEEPER_MODE</i>	0xEF	0000 0011	0	0	0	BEEPER_DURATION[1:0]		BEEPER_PULSE	BEEPER_PATH[1:0]	
<i>BEEPER_FREQ_VOL</i>	0xF0	0111 0000	BEEPER_FREQ[2:0]			BEEPER_VOLUME[4:0]				

**Mute**

<i>MUTE_DIGITAL</i>	0xF1	1001 1111	AUTOST_D_MUTE_ON	0	0	SCART_D_MUTE	SRND_HP_D_MUTE	SUB_D_MUTE	C_D_MUTE	LS_D_MUTE
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**S/PDIF**

<i>S/PDIF_OUT_CONFIG</i>	0xF2	0000 0100	0	0	0	0	0	SPDIF_OUT_MUTE	S/PDIF_OUT_SELECT[2:0]	
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**Headphone configuration**

<i>HEADPHONE_CONFIG</i>	0xF3	0000 001(0)	0	0	0	0	HP_FORCE	HP_LS_MUTE	HP_DETECT_ACTIVE	HP_DETECTED
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Table 8. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
<b>DAC Control</b>											
<i>DAC_CONTROL</i>	0xF4	0001 1111	0	0	S/PDIF_ MUX	DAC_SC ART_MU TE	DAC_SH P_MUTE	DAC_CS UB_MUT E	DAC_LS LR_MUT E	POWER_ UP	
<i>DAC_SW_CHANNELS</i>	0xF5	0000 0000	SUR_HP_SW		C_SUB_SW		LS_L_R_SW		SCART_SW		
<i>SPDIF_SW_CHANNELS</i>	0xF6	0000 0000	0	0	0	0	0	0	SPFI_SW		
<i>SPDIF_CHANNEL_STATUS</i>	0xF9	0000 0000	CHANNEL_STATUS		EMPHASIS			COPYRI GHT	NON_AU DIO	PRO_CO N	
<b>Autostandard coefficients settings</b>											
<i>AUTOSTD_COEFF_CTRL</i>	0xFB	0000 0001	0	0	0	0	0	0	AUTOSTD_COEFF_ CTRL[1:0]		
<i>AUTOSTD_COEFF_INDEX_MSB</i>	0xFC	0000 0000	0	0	0	0	0	0	0	AUTOST D_ COEFF_ INDEX_ MSB	
<i>AUTOSTD_COEFF_INDEX_LSB</i>	0xFD	0000 0000	AUTOSTD_COEFF_INDEX_LSB[7:0]								
<i>AUTOSTD_COEFF_VALUE</i>	0xFE	0000 0000	AUTOSTD_COEFF_VALUE[7:0]								
<i>PATCH_VERSION</i>	0xFF	0000 0000	PATCH_VERSION[7:0]								

## 12.2 STV82x7 general control registers

### CUT\_ID Version identification

7	6	5	4	3	2	1	0
0	0	CUT_NUMBER[5:0]					
R							

**Address:** 0x00

**Type:** R

**Reset:** 0x01

[7:6] Reserved

[5:0] Dice version identification

### RESET Software reset

7	6	5	4	3	2	1	0
BUS_EXP	I <sup>2</sup> S_OUTPUT	0	EN_STBY	0	SOFT_LRST2	SOFT_LRST1	SOFT_RST
R/W							

**Address:** 0x01

**Type:** R/W

**Reset:** 0x00

**Description:** The built-in Automatic Standard Recognition System (Autostandard) can be disabled. In this case, the software reset function (bits SOFT\_LRST1 and SOFT\_LRST2) can be used to implement the Automatic Standard Recognition by I<sup>2</sup>C Software. This is not required if the built-in Automatic Standard Recognition System function is used (default).

[7] Static control by I<sup>2</sup>C of hardware pin BUS\_EXP

[6] 0: I<sup>2</sup>S Input (I2S\_DATA0 , I2S\_SCLK, I2S\_LR\_CLK, I2S\_PCM\_CLK in input mode)

1: I<sup>2</sup>S Output (I2S\_DATA0 , I2S\_SCLK, I2S\_LR\_CLK, I2S\_PCM\_CLK in output mode, 512 x Fs will be provided on the I2S\_PCM\_CLK pin)

[5] Reserved.

[4] Standby mode enabling:

0: Normal mode

1: To lock the digital signals before to settle the device in standby mode

[3] Reserved.

[2] Softreset (active high) of channel 2 detectors only.

[1] Softreset (active high) of channel 1 detectors only.

[0] General softreset (active high) to reset all hardware registers except for I<sup>2</sup>C data.

**I2S\_CTRL****I<sup>2</sup>S synchronization control**

7	6	5	4	3	2	1	0
SYNC_OFF	SYNC_SIGN	0	LOCK_TH[1:0]		LOCK_MODE	SYNC_CST[1:0]	
R/W							

**Address:** 0x04**Type:** R/W**Reset:** 0x01

- [7] Open the loop of synchronization - external PCM clock is used internally and must be equal to  $512 \times f_{\text{SOUT}}$
- [6] Sign of the loop reversion (to be used in case of gain inversion of the frequency synthesizer)
- [5] Reserved
- [4:3] Lock detector threshold programming:
  - 00:  $\pm 1$  CLK period error of accumulation
  - 01:  $\pm 2$  CLK period error of accumulation
  - 10:  $\pm 4$  CLK period error of accumulation
  - 11:  $\pm 8$  CLK period error of accumulation
- [2] Lock detector mode
  - 0: Lock when accumulation error within lock threshold and LR detected (period counter not saturated)
  - 1: Lock when only accumulation error within lock threshold. Disregard the LR detection
- [1:0] Synchronization time constant
  - Defines the measurement period of LR:
  - 00: Half period measured (lowest accuracy)
  - 01: One full period measured
  - 10: Two full periods measured
  - 11: Four full periods measured (highest accuracy)

**I2S\_STAT****I<sup>2</sup>S synchronization status**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LR_OFF	LOCK_FLAG
R/W							

**Address:** 0x05**Type:** R/W**Reset:** 0x00

- [7:2] Reserved.
- [1] LR signal detection:
  - 0: LR signal detected and correct
  - 1: Missing LR pulses detected
- [0] Lock flag allowing unmute of audio output

**I2S\_SYNC\_OFFSET**                      **I<sup>2</sup>S synchronization offset frequency**

7	6	5	4	3	2	1	0
I2S_SFO[7:0]							
R/W							

**Address:**            0x06**Type:**              R/W**Reset:**             0x00[7:0] I<sup>2</sup>S synchronization frequency offset (±450 ppm full scale)**12.3 Clocking 1**

A low-jitter PLL Clock is integrated and can be fully reprogrammed using the registers described below. By default, the programming is defined for a 27-MHz quartz crystal frequency, which is the frequency recommended for reducing potential RF interference in the application. However, if necessary, the PLL Clock can be re-programmed for other quartz crystal frequencies within a range from 23 to 30 MHz. Other quartz crystal frequencies can be programmed on your demand.

*Note:*            *A Crystal Frequency change is compatible with other default I<sup>2</sup>C programming including the built-in Automatic Standard Recognition System.*

**SYS\_CONFIG**                              **System configuration control**

7	6	5	4	3	2	1	0
I2S_CH_NB[1:0]		INPUT_FREQ[3:0]				INPUT_CONFIG[1:0]	
R/W							

**Address:**            0x07**Type:**              R/W**Reset:**             0x00[7:6] Number of I<sup>2</sup>S channels input:

00: N/A  
 01: 2 channels  
 10: 4 channels  
 11: 6 channels

[5:2] I<sup>2</sup>S Input frequency:

0000 : 32 kHz  
 0001: 44.1 kHz  
 0010: 48 kHz  
 0011: 8 kHz (I<sup>2</sup>S input, 2 channels only)  
 0100 : 11.025 kHz (I<sup>2</sup>S input, 2 channels only)  
 0101 : 12 kHz (I<sup>2</sup>S input, 2 channels only)  
 0110 : 16 kHz (I<sup>2</sup>S input, 2 channels only)  
 0111 : 22.05 kHz (I<sup>2</sup>S input, 2 channels only)  
 1000 : 24 kHz (I<sup>2</sup>S input, 2 channels only)

- [1:0] Input stream to process  
 0 : SIF & SCART input (32 kHz)  
 1 : SCART input only (48 kHz)  
 2 : I<sup>2</sup>S input only

**FS1\_DIV****FS1 I/O divider programming**

7	6	5	4	3	2	1	0
EN_PROG	0	NDIV1[1:0]		0	SDIV1[2:0]		
R/W							

**Address:** 0x08  
**Type:** R/W  
**Reset:** 0x02

- [7] FS1 programming enable:  
 0: FS1 I<sup>2</sup>C registers programming ignored by system - FS1 pre-programmed automatically by SYS-CONFIG register (normal use with standard quartz of 27 MHz)  
 1: FS1 I<sup>2</sup>C registers programming used by system - FS1 pre-programming by SYS-CONFIG deactivated (to be used in case of no standard quartz, different from 27 MHz)
- [6] Reserved.
- [5:4] FS1 input clock divider selection
- [3] Reserved.
- [2:0] FS1 output clock divider selection

**FS1\_MD****FS1 coarse selection**

7	6	5	4	3	2	1	0
0	0	0	MD1[4:0]				
R/W							

**Address:** 0x09  
**Type:** R/W  
**Reset:** 0x11

- [7:5] Reserved.
- [4:0] FS1 coarse selection

**FS1\_PE\_H** **FS1 fine selection (MSBs)**

7	6	5	4	3	2	1	0
PE_H1[7:0]							
R/W							

**Address:** 0x0A**Type:** R/W**Reset:** 0x36

[7:0] FS1 fine selection (MSBs)

**FS1\_PE\_L** **FS1 fine selection (LSBs)**

7	6	5	4	3	2	1	0
PE_L1[7:0]							
R/W							

**Address:** 0x0B**Type:** R/W**Reset:** 0x00

[7:0] FS1 Fine Selection (LSBs)

**12.4 Demodulator****DEMOD\_CTRL** **Demodulator control**

7	6	5	4	3	2	1	0
0	0	FAR_MODE	GAP_MODE	AM_SEL	DEMOD_MODE[2:0]		
R/W							

**Address:** 0x0C**Type:** R/W**Reset:** 0x06

[7:6] Reserved

[5] 1: Farrow and mono filter for NICAM active

*Note: The following register bits are controlled by Autostandard and are forced by default to read-only mode.*

[4] Defines the clock gapping mode of the demodulator

0: (default), the FS1 freq is controlled by stl-error (clock-pll mode) to align the instantaneous value of the internal clock with respect to the received NICAM clock

1: the FS1 freq is fixed and the mean value of the internal clock is aligned by variable gapping (src-error) with respect to the received NICAM clock

- [3] Demodulator configuration select:
  - 0: FM configuration of demodulator (default)
  - 1: AM configuration of demodulator

- [2:0] Demodulator mode select:
 

	<u>CH1 FM</u>	<u>CH2 FM/QPSK</u>
000:	Normal	FM Normal
001:	Wide	FM Wide
010:	Normal	QPSK System B/G/L/D/K
011:	Wide	QPSK System B/G/L/D/K
100:	Normal	FM Wide
101:	Wide	FM Normal
110:	Normal	QPSK System I
111:	Wide	QPSK System I

**DEMOD\_STAT**

**Demodulator detection status**

7	6	5	4	3	2	1	0
0	0	0	QPSK_LK	FM2_CAR	FM2_SQ	FM1_CAR	FM1_SQ
R							

**Address:** 0x0D

**Type:** R

**Reset:** 0x00

- [7:5] Reserved.
- [4] QPSK lock detection flag
  - 0: Not detected
  - 1: Detected
- [3] Channel 2 FM/AM carrier detection flag
  - 0: Not detected
  - 1: Detected
- [2] Channel 2 FM squelch detection flag
  - 0: Not detected
  - 1: Detected
- [1] Channel 1 FM/AM carrier detection flag
  - 0: Not detected
  - 1: Detected
- [0] Channel 1 FM squelch detection flag
  - 0: Not detected
  - 1: Detected

*Note:* These registers allow direct access to the demodulator signal detectors.



**AGC\_CTRL** **IF AGC control**

7	6	5	4	3	2	1	0
AGC_CMD	0	0	AGC_REF[2:0]			AGC_CST[1:0]	
R/W							

**Address:** 0x0E

**Type:** R/W

**Reset:** 0x11

*Note: The following register bit is controlled by Autostandard and is forced by default to read-only mode.*

[7] Automatic gain control command mode:

Normally set to 0 enabling automatic mode. For L/L' standards, the AGC should be switched off due to the presence of the AM sound carrier. In this case, a fixed gain value should be set using the AGCS register.

0: Automatic mode. AGC controlled by the Autostandard function. (default)

1: Manual/Forced mode

[6:5] Reserved.

[4:2] This bit is used to defines the clipping level which adjusts the allowable proportion of samples at the input of the ADC which will be clipped. The AGC tries to maximize the use of the full scale range of the ADC. The default setting gives a ratio of 1/256.

<u>Clipping ratio</u>	<u>Clipping ratio</u>
000: 1/16 (single carrier)	100: 1/256 (default)
001: 1/32	101: 1/512
010: 1/64	110: 1/1024
011: 1/128	111: 1/2048 (multiple carriers)

[1:0] AGC time constant

This is the time constant between each step of 1.5 dB by the AGC.

<u>Step duration (ms)</u>	
00	1.33
01	2.66
10	5.33
11	10.66

**AGC\_GAIN** **IF AGC control and status**

7	6	5	4	3	2	1	0
0	AGC_ERR[4:0]				SIG_OVER	SIG_UNDER	
R/W							

**Address:** 0x0F

**Type:** R/W

**Reset:** 0x00

[7] Reserved.

- [6:2] Amplifier gain control:  
 This is the gain control value of AGC. There are 20 steps of +1.5 dB (see Note below).  
 00000: Gain-min  
 10100: Gain-min + 30 db  
 11111: Gain-min + 30 db
- [1] AGC input signal upper threshold  
 0: Normal signal  
 1: Signal too large and AGC is overloaded
- [0] AGC input signal lower threshold:  
 0: Normal signal  
 1: Signal too small and AGC is underloaded  
 When the AGC is in automatic mode (AGC\_CMD = 0), bits SIG\_OVER and SIG\_UNDER indicate if the input signal is too small/large and the AGC is under/overloaded. This is useful when setting the STV82x7 SIF input level.

*Note:* When **AGC\_CMD = 0**, **AGC\_ERR[4:0]** can be read -- indicating the input level. It can also be written to -- presetting the AGC level which will then adjust itself to the final value.

When **AGC\_CMD = 1**, the AGC is off and writing to **AGC\_ERR[4:0]** directly controls the AGC amplifier gain. Reading AGC\_ERR just confirms the fixed value.

**DC\_ERR\_IF DC offset status for IF ADC**

7	6	5	4	3	2	1	0
DC_ERR[7:0]							
R							

**Address:** 0x10  
**Type:** R  
**Reset:** 0x00

[7:0] DC offset error of IF ADC output

**12.5 Demodulator channel 1**

**CARFQ1H Channel 1 carrier DCO frequency**

**Address:** 0x12  
**Type:** R/W  
**Reset:** 0x3E

7	6	5	4	3	2	1	0
CARFQ1H[23:16]							
R/W							

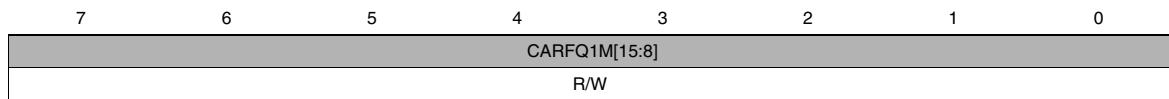
[7:0] Channel 1 DCO carrier frequency (8 MSBs).



Note: This register is controlled by Autostandard and is forced by default to read-only mode

**CARFQ1M Channel carrier DCO frequency**

**Address:** 0x13  
**Type:** R/W  
**Reset:** 0x80

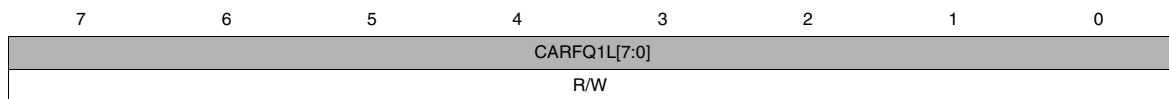


[7:0] Channel 1 DCO carrier frequency.

Note: This register is controlled by Autostandard and is forced by default to read-only mode

**CARFQ1L Channel 1 carrier DCO frequency**

**Address:** 0x14  
**Type:** R/W  
**Reset:** 0x00



[7]:0 Channel 1 DCO carrier frequency (8 LSBs), see [Table 9](#)

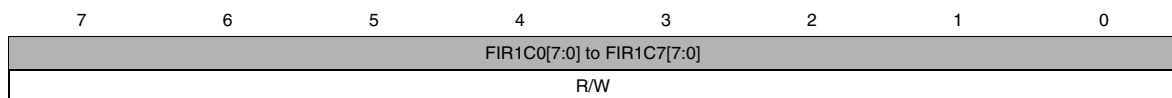
Note: This register is controlled by Autostandard and is forced by default to read-only mode.

**Table 9. Mono carrier frequencies by system**

System	Mono carrier freq. (MHz)	CARFQ1[23:0] (dec)	CARFQ1[23:0]
M/N	4.5	3072000	0x2EE000
B/G	5.5	3754667	0x394AAB
I	6.0	4096000	0x3E8000
L	6.5	4453717	0x43F555
D/K/K1/K2	6.5	4437333	0x43B555

Note: Carrier frequency:  $CARFQ1(dec) \cdot f_S / 2^{24}$  with  $f_S = 24.576$  MHz (crystal oscillator frequency independent)

**FIR1C Channel 1 FIR coefficients**



Address: 0x15 to 0x1C

Type: R/W

Table 10. Channel 1 FIR coefficients

Bitfield	Description							
	FM 27 kHz <sup>(1)</sup>	FM 50 kHz <sup>(2)</sup>	FM 75 kHz	FM 100 kHz	FM 200 kHz	FM 350 kHz	FM 500 kHz	AM
FIR1C0[7:0]	0xFF	0x00	0x01	0xFF	0x00	0x02	0x01	0x00
FIR1C1[7:0]	0xFE	0xFE	0x03	0x00	0x01	0x01	0x00	0xFE
FIR1C2[7:0]	0xFE	0xFC	0x02	0x05	0x01	0xFC	0x04	0xFD
FIR1C3[7:0]	0x00	0xFD	0xFC	0x02	0xFC	0x03	0xFA	0xFE
FIR1C4[7:0]	0x06	0x02	0xF8	0xF8	0x08	0x04	0x05	0x04
FIR1C5[7:0]	0x0E	0x0D	0x01	0xF9	0xF6	0xF2	0x00	0x0D
FIR1C6[7:0]	0x16	0x18	0x18	0x15	0xF8	0x06	0xF2	0x16
FIR1C7[7:0]	0x1B	0x1F	0x2D	0x35	0x4A	0x43	0x4D	0x1D

1. Default mode for M/N standard.

2. Default mode for B/G/I/D/K standards

Note: The above registers are controlled by Autostandard and are forced by default to read-only mode.

**ACOEFF1****Channel 1 baseband PLL loop filter proportional coefficient**

7	6	5	4	3	2	1	0
ACOEFF1[7:0]							
R/W							

Address: 0x1D

Type: R/W

Reset: 0x23

Note: This register is controlled by Autostandard and is forced by default to read-only mode.

[7:0] Used to program the proportional coefficient of the baseband PLL loop filter (channel 1)  
 Defines the damping factor of the loop. For values, refer to [Table 11](#).

**BCOEFF1****Channel 1 baseband PLL loop filter integral coefficient and DCO gain**

7	6	5	4	3	2	1	0
BCOEFF1[7:0]							
R/W							

Address: 0x1E

**Type:** R/W

**Reset:** 0x12

*Note:* This register is controlled by Autostandard and is forced by default to read-only mode.

[7:0] Used to program the Integral coefficient of the baseband PLL loop filter and DCO gain  
Defines the bandwidth of the loop. For values, refer to [Table 11](#).

**Table 11. Baseband PLL loop filter adjustment (FM mode)**

FM mode	Small	Standard	Medium	Wide <sup>(1)</sup>	A2 standard
ACOEFF	0x10	0x22	0x2C	0x2C	0x10
BCOEFF	0x1A	0x12	0x0A	0x0A	0x11
FM_DEV max (kHz)	62.5	125	250	500	125
DCO Range (kHz)	96	192	384	768	192

1. Refer to DEMOD\_MODE[2:0] bits in the DEMOD\_CTRL register.

*Note:* 1 FM Pre-scale has to be adjusted depending on the chosen FM Mode.

2 FM squelch threshold has to be adjusted depending on the chosen FM Mode.

**CRF1 Channel 1 baseband PLL demodulator offset**

7	6	5	4	3	2	1	0
CRF1[7:0]							
R							

**Address:** 0x1F**Type:** R**Reset:** 0x00

[7:0] Channel 1 carrier recovery frequency  
Displays the instantaneous frequency offset of the channel 1 baseband PLL demodulator.

**CETH1 Channel 1 FM/AM carrier level threshold**

7	6	5	4	3	2	1	0
CETH1[7:0]							
R/W							

**Address:** 0x20**Type:** R/W**Reset:** 0x20

[7:0] This register is used to compare the carrier level in the channel and the threshold value. This level is measured after the channel filter and is relative to the full scale reference level (0 dB). This is used as part of the validation of an FM signal, if the carrier level is below the threshold, the signal is considered to be non-valid.

<u>CETH</u>	<u>Threshold (dB)</u>	<u>CETH</u>	<u>Threshold (dB)</u>
0xFF	-6	0x10	-32 (recommended value)
0x80	-12	0x08	-38
0x40	-18	0x00	OFF (all carrier levels are accepted)
0x20	-24 (default)		

**SQTH1 Channel 1 FM squelch threshold**

7	6	5	4	3	2	1	0
SQTH1[7:0]							
R/W							

**Address:** 0x21**Type:** R/W**Reset:** 0x3C

[7:0] The squelch detector measures the level of high frequency noise and compares it to the threshold level (SQTH). If the level is below this value, the S/N of the FM signal is considered to be acceptable. Values are given for FM with standard deviation.

<u>SQTH</u>	<u>S/N (dB)</u>
0xFA	0
0x77	10
0x3C	15 (default)
0x23	20
0x19	25

*Note:* FM squelch threshold has to be adjusted depending on the chosen FM Mode.

## CAROFFSET1 Channel 1 DCO carrier offset compensation

7	6	5	4	3	2	1	0
CAROFFSET1[7:0] (S)							
R/W							

**Address:** 0x22  
**Type:** R/W  
**Reset:** 0x00

[7:0] This value is used to correct the carrier frequency offset of the incoming IF signal. Automatic frequency control in FM mode can be implemented by registers [DC\\_REMOVAL\\_L](#) and [DC\\_REMOVAL\\_R](#).

A DCO frequency offset (in two's complement format) is added to the pre-programming value by AUTOTSD in the CARFQ1 registers (corresponding to the standard IF carrier frequency). The programmable carrier offset ranges from -192 kHz to +190.5 kHz with a resolution of 1.5 kHz.

For standard FM deviation, the value displays by [DC\\_REMOVAL\\_L](#) and [DC\\_REMOVAL\\_R](#) can be directly loaded in CAROFFSET1 to exactly compensate the carrier offset on channel 1.

## 12.6 Demodulator channel 2

### IAGCR Channel 2 internal AGC reference for QPSK

7	6	5	4	3	2	1	0
IAGC_REF[7:0]							
R/W							

**Address:** 0x25  
**Type:** R/W  
**Reset:** 0x88

[7:0] Sets the mean value of the internal AGC, used for QPSK demodulation. The default setting corresponds to half full scale amplitude at the baseband PLL input.

**IAGCC****Channel 2 internal AGC time constant for QPSK**

7	6	5	4	3	2	1	0
IAGC_OFF	FAR_FLT_EN	MONO_FLT_EN	BG_SEL	MONO_PROG	IAGC_CST[2:0]		
R/W							

**Address:** 0x26**Type:** R/W**Reset:** 0x03

[7] AGC disable:  
 0: Internal AGC is active  
 1: Internal AGC is disabled

[6] 1: Enable farrow filter for NICAM

[5] 1: Enable mono filter for NICAM

[4] 1: BG NICAM mono filter selected

*Note: The above register bits are controlled by Autostandard and are forced by default to read-only mode.*

[3] 1: Enable programming of mono filter

[2:0] Internal AGC programmable step constant.

These bits control the time per step (values given for QPSK mode). The default value defines the optimum trade-off between fast settling time (for the fastest NICAM identification) and the noise immunity (minimum BER degradation)

	<u>Step time (us)</u>	<u>Time response (ms)</u>
000	703	128
001	352	64
010	176	32
011	88	16
100	44	8
101	22	4
110	11	2
111	5.5	0.82

**IAGCS****Channel 2 internal AGC status for QPSK**

7	6	5	4	3	2	1	0
IAGC_CTRL[7:0]							
R							

**Address:** 0x27**Type:** R**Reset:** 0x00

[7:0] Indicates the value of the internal AGC gain control



**CARFQ2H** Channel 2 carrier DCO frequency

**Address:** 0x28  
**Type:** R/W  
**Reset:** 0x44

7	6	5	4	3	2	1	0
CARFQ1H[23:16]							
R/W							

[7:0] Channel 2 DCO carrier frequency (8 MSBs).

*Note: This register is controlled by Autostandard and is forced by default to read-only mode*

**CARFQ2M** Channel 2 carrier DCO frequency

**Address:** 0x29  
**Type:** R/W  
**Reset:** 0x40

7	6	5	4	3	2	1	0
CARFQ1M[15:8]							
R/W							

[7:0] Channel 2 DCO carrier frequency.

*Note: This register is controlled by Autostandard and is forced by default to read-only mode*

**CARFQ2L** Channel 2 carrier DCO frequency

**Address:** 0x2A  
**Type:** R/W  
**Reset:** 0x00

7	6	5	4	3	2	1	0
CARFQ1L[7:0]							
R/W							

[7:0] Channel 2 DCO carrier frequency (8 LSBs), see [Table 12](#)..

*Note: This register is controlled by Autostandard and is forced by default to read-only mode.*

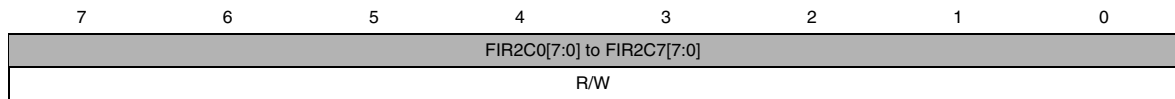
**Table 12. Stereo carrier frequencies by system**

System	Stereo carrier freq. (MHz)	CARFQ2[23:0] (dec)	CARFQ2[23:0]
M/N A2+	4.724212	3225062	0x3135E6
B/G NICAM	5.85	3993600	0x3CF000
BG A2	5.7421875	3920000	0x3BD080
I NICAM	6.552	4472832	0x444000

**Table 12. Stereo carrier frequencies by system (continued)**

System	Stereo carrier freq. (MHz)	CARFQ2[23:0] (dec)	CARFQ2[23:0]
L NICAM	5.85	3993600	0x3CF000
DK NICAM	5.85	3993600	0x3CF000
DK1 A2*	6.2578125	4272000	0x412F80
DK2 A2*	6.7421875	4602667	0x463B2B
DK3 A2*	5.7421875	3920000	0x3BD080

**FIR2C Channel 2 FIR coefficients**



**Address:** 0x2B to 0x32

**Type:** R/W

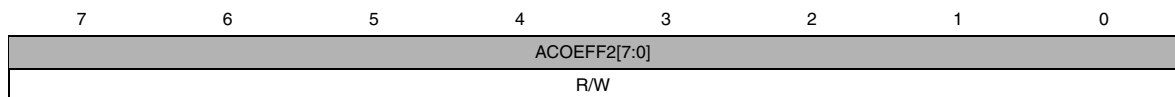
[7:0] Channel 2 FIR coefficients

**Table 13. Channel 2 FIR coefficients**

Bitfield	Description			
	FM 27 kHz	FM 50 kHz	QPSK 40%	(reset state) QPSK100%
FIR2C0[7:0]	0xFF	0x00	0x00	0x00
FIR2C1[7:0]	0xFE	0xFE	0x00	0x00
FIR2C2[7:0]	0xFE	0xFC	0xFF	0x00
FIR2C3[7:0]	0x00	0xFD	0x03	0x00
FIR2C4[7:0]	0x06	0x02	0x00	0xFF
FIR2C5[7:0]	0x0E	0x0D	0xF4	0x04
FIR2C6[7:0]	0x16	0x18	0x0A	0x14
FIR2C7[7:0]	0x1B	0x1F	0x3D	0x25

*Note:* The above registers are controlled by Autostandard and are forced by default to read-only mode.

**ACOEFF2 Channel 2 baseband PLL loop filter proportional coefficient**



**Address:** 0x33

**Type:** R/W  
**Reset:** 0x90

*Note:* This register is controlled by Autostandard and is forced by default to read-only mode.

[7:0] This value defines the loop clamping factor used to program the proportional coefficient of the baseband PLL loop filter (channel 2). See [Table 14](#) and [Table 15](#).

## BCOEFF2 Channel 2 baseband PLL loop filter integral coefficient and DCO gain

7	6	5	4	3	2	1	0
BCOEFF2[7:0]							
R/W							

**Address:** 0x34  
**Type:** R/W  
**Reset:** 0xAC

[7:0] This value defines the loop bandwidth used to program the integral coefficient of the baseband PLL loop filter and DCO gain. See [Table 14](#) and [Table 15](#).

**Table 14. Baseband PLL loop filter adjustments (FM mode)**

FM mode	Small	Standard	Mid	Wide	A2 standard
ACOEFF	0x10	0x22	0x2C	0x2C	0x10
BCOEFF	0x1A	0x12	0x0A	0x0A	0x11
FM_DEV max (kHz)	62.5	125	250	500	125
DCO Range (kHz)	96	192	384	768	192

**Table 15. Baseband PLL loop filter adjustments (QPSK mode)**

QPSK mode	Small	Medium	Large	Extra-large
ACOEFF	0x90	0x90	0x90	0x90
BCOEFF	0xAC	0xA3	0x9A	0x91
DCO_DEV max (kHz)	2.84375	5.6875	11.375	22.75

## SCOEFF Channel 2 symbol tracking loop coefficients

7	6	5	4	3	2	1	0
SCOEFF[7:0]							
R/W							

**Address:** 0x35  
**Type:** R/W  
**Reset:** 0x1C

Note: This register is controlled by Autostandard and is forced by default to read-only mode.

[7:0] This value is used to program the proportional and integral coefficients of the QPSK Symbol tracking loop. See [Table 16](#) and [Table 17](#).

**Table 16. QPSK system - BG/L/DK standards (40% Roll-off)**

	Extra-small	Small	Medium	Large	Extra-large	Open loop
SCOEFF	0x1E	0x25	0x24	0x26	0x2A	0x80

**Table 17. QPSK system - I standard (100% Roll-off)**

	Extra-small	Small	Medium	Large	Extra-large
SCOEFF	0x16	0x1D	0x1C	0x23	0x22

## SRF

### Channel 2 symbol tracking loop frequency

7	6	5	4	3	2	1	0
SRF[7:0]							
R/W							

**Address:** 0x36

**Type:** R/W

**Reset:** 0x00

[7:0] Displays in two's complement format the frequency deviation between the incoming NICAM bitstream and the quartz clocks. The maximum error is  $\pm 250$  ppm.

## CRF2

### Channel 2 baseband PLL demodulator offset

7	6	5	4	3	2	1	0
CRF2[7:0]							
R/W							

**Address:** 0x37

**Type:** R/W

**Reset:** 0x00

[7:0] Channel 2 carrier recovery frequency.  
Displays the instantaneous frequency offset of the channel 2 baseband PLL

**CAROFFSET2****Channel 2 DCO carrier offset compensation**

7	6	5	4	3	2	1	0
CAROFFSET2[7:0] (S)							
R/W							

**Address:** 0x3A**Type:** R/W**Reset:** 0x00

[7:0] This value is used to correct the carrier frequency offset of the incoming IF signal. Automatic frequency control in FM mode can be implemented by registers [DC\\_REMOVAL\\_L](#) and [DC\\_REMOVAL\\_R](#).

A DCO frequency offset (in two's complement format) is added to the pre-programming value by AUTOTSD in the CARFQ2 registers (corresponding to the standard IF carrier frequency). The programmable carrier offset ranges from -192 kHz to +190.5 kHz with a resolution of 1.5 kHz.

For standard FM deviation, the value displayed by register [DC\\_REMOVAL\\_R](#) can be directly loaded in register [CAROFFSET2](#) to exactly compensate the carrier offset on channel 2.

**12.7 NICAM registers****NICAM\_CTRL****NICAM decoder control**

7	6	5	4	3	2	1	0
0	0	0	0	0	DIF_POL	ECT	MAE
R/W							

**Address:** 0x3D**Type:** R/W**Reset:** 0x00

[7:3] Reserved.

[2] 0: No polarity inversion (default)  
1: Polarity inversion of the differential decoding

[1] Error counter timer: Defines the NICAM error measurement period  
0: 128 ms (default)  
1: 64 ms

[0] Max. allowed errors: Defines the NICAM error decoding for mute function.  
0: 511 Max (default)  
1: 255 Max

**NICAM\_BER**                      **NICAM bit error rate**

7	6	5	4	3	2	1	0
ERROR[7:0]							
R							

**Address:** 0x3E**Type:** R**Reset:** 0x00

[7:0] NICAM error counter value

**NICAM\_STAT**                      **NICAM detection status**

7	6	5	4	3	2	1	0
NIC_DET	F_MUTE	LOA	CBI[3:0]			NIC_MUTE	
R							

**Address:** 0x3F**Type:** R**Reset:** 0x00

- [7] NICAM signal detect:
  - 0: NICAM signal no detected
  - 1: NICAM signal detected
- [6] Frame mute:
  - 0: No mute
  - 1: Mute due to superframe alignment loss
- [5] Loss of the frame alignment word (FAW):
  - 0: No alignment lost
  - 1: Frame alignment word lost
- [4:1] Indicates the received NICAM control bits
- [0] Indicates the NICAM decoder mute

**12.8 Stereo mode****ZWT\_CTRL**                      **Zweiton detector control**

7	6	5	4	3	2	1	0
LRST_TONE_O FF	STD_MODE	THRESH[3:0]			TSCTRL[1:0]		
R/W							

**Address:** 0x40**Type:** R/W

**Reset:** 0x30

- [7] Control of the reset of the tone detector:
  - 0: Periodical reset of tone detection enabled
  - 1: Periodical reset of tone detection disabled

*Note: The following register bit is controlled by Autostandard and is forced by default to read-only mode.*

- [6] 0: German standard (default)
- 1: Korean standard

[5:2] Defines the threshold of the detector for pilot and tone frequencies:

	Level (% of the mid scale)		Level (% of the mid scale)	
0000	0	1000	50	
0001	6.25	1001	56.25	
0010	12.5	1010	62.5	
0011	18.75	1011	68.75	
0100	25	1100 (default)	75	
0101	31.25	1101	81.25	
0110	37.5	1110	87.5	
0111	43.75	1111	93.75	

[1:0] Defines both the detection time and the error probability (reliability of the detection).

	Sample Accumulation	Decision Count	Time (ms)	Error Probability
00	1024	2	256	10 <sup>-4</sup>
01 (default)	1024	3	384	10 <sup>-6</sup>
10	2048	2	512	10 <sup>-7</sup>
11	2048	3	768	10 <sup>-9</sup>

**ZWT\_TIME**

**Zweiton detector timing**

7	6	5	4	3	2	1	0
0	0	0	0	0	ZWT_TIME[2:0]		
R/W							

**Address:** 0x41

**Type:** R/W

**Reset:** 0x04

[7:3] Reserved.

*Note: The following register bits are controlled by Autostandard and are forced by default to read-only mode.*

[2:0] Defines the period (duration) of the reset tone used for tone detection system reset.

000: 256 ms	100: 1280 ms
001: 512 ms	101: 1536 ms
010: 768 ms	110: 1792 ms
011: 1024 ms	111: 2040 ms

**ZWT\_STAT****Zweiton status**

7	6	5	4	3	2	1	0
LRST_TONE_O FF	0	0	0	ZW_STAT_ RDY	ZW_DET	ZW_ST	ZW_DM
R							

**Address:** 0x42**Type:** R**Reset:** 0x00

[7] Indicates the status of the control bit programmed in the reg ZWT-CTRL:

- 0: Periodical reset of tone detection enabled
- 1: Periodical reset of tone detection disabled

[6:4] Reserved.

[3] Periodic flag indicating when the tone detection flags are updated and ready to be read

[2] Pilot detection flag

[1] Stereo tone detection flag

[0] Dual mono tone detection flag

**12.9 Analog control****ADC\_CTRL****I2S\_DATA0 and ADC input selection and power-up**

7	6	5	4	3	2	1	0
I2S_DATA0_CTRL[1:0]	0	0	ADC_POWER_ UP	ADC_INPUT_SEL[2:0]			
R/W							

**Address:** 0x56**Type:** R/W**Reset:** 0x08

[7:6] Source selection for output I2S\_DATA0

- 00 = SCART
- 01 = L, R
- 10 = HP or Srnd
- 11 = C/Sub

[5:4] Reserved.

[3] Control of the power up of the audio ADC:

- 0: ADC in power down mode
- 1: Wake up of the ADC



[2:0] Selection of the ADC input signal:  
 000: SCART 1 (default) 011: SCART 4  
 001: SCART 2 100: Mono input  
 010: SCART 3 Other: reserved

**SCART1\_2\_OUTPUT\_CTRL SCART 1\_2 output selection and mute**

7	6	5	4	3	2	1	0
SC2_MUTE	SC2_OUTPUT_SEL[2:0]			SC1_MUTE	SC1_OUTPUT_SEL[2:0]		
R/W							

**Address:** 0x57  
**Type:** R/W  
**Reset:** 0xA8

- [7] Mute command for the output SCART 2:  
 0: output not muted  
 1: output muted
- [6] Selection of the output SCART 2 configuration:  
 000: DSP 100: Input SCART 3  
 001: Mono input 101: Input SCART 4  
 010: Input SCART 1 (default) Other: Reserved  
 011: Input SCART 2
- [5] Mute command for the output scart 1:  
 0: output not muted  
 1: output muted
- [4] Selection of the output SCART 1 configuration:  
 000: DSP (default) 100: Input SCART 3  
 001: Mono input 101: Input SCART 4  
 010: Input SCART 1 Other: Reserved  
 011: Input SCART 2

**SCART3\_OUTPUT\_CTRL SCART 3 output selection and mute**

7	6	5	4	3	2	1	0
0	0	0	0	SC3_MUTE	SC3_OUTPUT_SEL[2:0]		
R/W							

**Address:** 0x58  
**Type:** R/W  
**Reset:** 0x0B

- [7:4] Reserved.
- [3] Mute command for the output SCART 3:  
 0: output not muted  
 1: output muted

[2:0] Selection of the output SCART 3 configuration:

000: DSP	100: Input SCART 3
001: Mono input	101: Input SCART 4
010: Input SCART 1	Other: Reserved
011: Input SCART 2 (default)	

## Clocking 2

### FS2\_DIV

### FS2 I/O divider programming

7	6	5	4	3	2	1	0
0	0	NDIV2[1:0]			SDIV2[2:0]		
R/W							

**Address:** 0x5A

**Type:** R/W

[7:6] Reserved.

[5:4] FS2 Input clock divider selection

[3] Reserved.

[2:0] FS2 Output clock divider selection

### FS2\_MD

### FS2 coarse selection

7	6	5	4	3	2	1	0
0	0	0					MD2[4:0]
R/W							

**Address:** 0x5B

**Type:** R/W

**Reset:** 0x10

[7:5] Reserved.

[4:0] FS2 coarse selection

**FS2\_PE\_H****FS2 fine selection (MSBs)**

7	6	5	4	3	2	1	0
PE_H2[7:0]							
R/W							

**Address:** 0x5C**Type:** R/W**Reset:** 0x5C

[7:0] FS2 fine selection (MSBs)

**FS2\_PE\_L****FS2 fine selection (LSBs)**

7	6	5	4	3	2	1	0
PE_L2[7:0]							
R/W							

**Address:** 0x5D**Type:** R/W**Reset:** 0x29

[7:0] FS2 fine selection (LSBs)

**12.10 DSP control****HOST\_CMD****DSP hardware control**

7	6	5	4	3	2	1	0
IT_IN_DSP	0	0	0	0	HW_RESET		
R/W							

**Address:** 0x80**Type:** R/W**Reset:** 0x00[7] Valid I<sup>2</sup>C table.

[6:3] Reserved.

[2] DSP hardware run when set

[1:0] Reserved.

**IRQ\_STATUS****IRQ status**

7	6	5	4	3	2	1	0
IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
R/W							

**Address:** 0x81**Type:** R/W**Reset:** 0x00

- [7:4] Reserved
- [3] Unmute HP/Srnd DAC IRQ
- [2] HP connection/deconnection IRQ
- [1] I<sup>2</sup>S lock lost IRQ
- [0] Autostandard IRQ

**SOFT\_VERSION****Embedded software version**

7	6	5	4	3	2	1	0
SOFT_VERSION[7:0]							
R							

**Address:** 0x82**Type:** R**Reset:** 0x02

- [7:0] Version of the embedded software.

**ONCHIP\_ALGOS****Display algorithms available on the chip**

7	6	5	4	3	2	1	0
0	PRO_LOGIC_S ELECT	NICAM	I2S_INPUT	TRUBASS	TRU SURROUND	PRO_LOGIC	MULTICHANNEL
R							

**Address:** 0x83**Type:** R**Reset:** 0x00

- [7] Reserved.
- [6] 0: Dolby Pro Logic I  
1: Dolby Pro Logic II
- [5] NICAM demodulator is present when set.
- [4] 0: 1 I<sup>2</sup>S input  
1: 3 I<sup>2</sup>S inputs

- [3] SRS Trubass algorithm is present when set.
- [2] SRS Trusurround algorithm is present when set.
- [1] Dolby Pro Logic algorithm is present when set.
- [0] Multi-channels output is present when set.

### DSP\_STATUS                      DSP status

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	INIT_MEM
R							

**Address:** 0x84

**Type:** R

**Reset:** 0x00

- [7:1] Reserved.
- [0] DSP initialization:
  - 0: DSP is not initialized.
  - 1: DSP is initialized.

### DSP\_RUN                              DSP configuration and run

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HOST_ NO_INIT	HOST_RUN
R/W							

**Address:** 0x85

**Type:** R/W

**Reset:** 0x00

- [7:2] Reserved
- [1] 0: I<sup>2</sup>C register table is initialized when we soft reset
  - 1: I<sup>2</sup>C register table is not initialized when we soft reset
- [0] 0: Soft reset DSP
  - 1: Start DSP processing

**I2S\_IN\_CONFIG****I<sup>2</sup>S configuration**

7	6	5	4	3	2	1	0
LOCK_MODE_EN	0	SYNC	LRCLK_START	LRCLK_POLARITY	SCLK_POLARITY	DATA_CFG	I2S_MODE
R/W							

**Address:** 0x86**Type:** R/W**Reset:** 0x86

[7] 0: Disable lock mode for external I<sup>2</sup>S input  
 1: Enable lock mode for external I<sup>2</sup>S input

[6] Reserved.

[5] I<sup>2</sup>S synchronisation:  
 0: Capture directly  
 1: Wait for synchro

[4] According to LRCLK POLARITY, first data take:  
 0: Left  
 1: Right

[3] Polarity of the left data

[2] 0: Falling edge  
 1: Rising edge

[1] 0: LSB first  
 1: MSB first

[0] 0: Non standard mode  
 1: Standard mode

**AV\_DELAY****Audio/Video delay**

7	6	5	4	3	2	1	0
DELAY_TIME							DELAY_ON
R/W							

**Address:** 0x89**Type:** R/W**Reset:** 0x00

[7] Audio delay time (see [Table 18](#))  
 0000000: 0 ms  
 ...  
 0111100: 60 ms (48 kHz)  
 ...  
 1011010: 90 ms (32 kHz)

[6] Audio/video delay is enabled when set.

**Note:** AV\_DELAY acts on both LS and HP paths simultaneously (same delay)

**Table 18. Audio/Video delay (lip sync) configuration**

Register values								Output									
Input source	AV_DELAY (89h)		SNRD_DELAY[4:0]	CENTER_DELAY [3:0]	LS_L		LS_R		HP_L/R		Scart_L		Scart_R				
	DELAY_TIME[6:0]	DELAY_ON			Source SIF	Source Scart	Source SIF	Source Scart	Source SIF	Source Scart	Source SIF	Source Scart	Source SIF	Source Scart			
SIF or Scart (32KHz)	10110100	90	1	xxx00000	0	xxxx0000	0	90	90	90	90	90	90	0	0	0	0
	10110100	90	1	xxx00000	0	xxxx1010	10	60	60	60	60	60	60	0	0	0	0
	10110100	90	1	xxx11110	30	xxxx0000	0	60	60	60	60	60	60	0	0	0	0
	10110100	90	1	xxx11110	30	xxxx1010	10	60	60	60	60	60	60	0	0	0	0
Scart only (48KHz)	01111000	60	1	xxx00000	0	xxxx0000	0	-	60	-	60	-	60	-	0	-	0
	01111000	60	1	xxx00000	0	xxxx1010	10	-	30	-	30	-	30	-	0	-	0
	01111000	60	1	xxx11110	30	xxxx0000	0	-	30	-	30	-	30	-	0	-	0
	01111000	60	1	xxx11110	30	xxxx1010	10	-	30	-	30	-	30	-	0	-	0

Note: All audio delay values are in milliseconds.

## 12.11 Automatic standard recognition

### AUTOSTD\_CTRL Automatic standard recognition control

7	6	5	4	3	2	1	0
0	0	0	FORCE_SQUEL CH	SINGLE_SHOT	DK_DEV[1:0]		LDK_SW
R/W							

**Address:** 0x8A  
**Type:** R/W  
**Reset:** 0x01

- [7:5] Reserved.
- [4] Allow to force squelch detection
  - 0: FM squelch is taken into consideration for MONO detection
  - 1: FM squelch is not taken into consideration for MONO detection
- [3] Single shot mode selection:
  - 0: Single Shot mode is not selected
  - 1: Single Shot mode is selected<sup>(1)</sup>
- [2:1] Selects FM deviation configuration to take into account of overmodulation in DK\_NICAM standard.
  - 00: FM 50 kHz (default)
  - 01: FM 200 kHz
  - 10: FM 350 kHz
  - 11: FM 500 kHz
- [0] Makes exclusive the auto search of DK/K1/K2/K3 and L/L' standard
  - 0: DK/K1/K2/K3 standard auto-search / L/L' disabled
  - 1: L/L' standard auto-search DK/K1/K2/K3 disabled

1. **Single\_Shot** mode can be used before disabling the Automatic Standard Recognition (Autostandard) to pre-program demodulator registers in a defined standard and reduce I<sup>2</sup>C programming in Manual mode

**Note:** *Only standard deviation FM 50K kHz is compatible with other D/K1/K2/K3 standards in Automatic Standard Recognition Search mode.*

*FM deviation superior to 350 kHz will degrade strongly NICAM reception due to overlapping of FM and QPSK IF spectrum in DK-NICAM standard.*

*L/L' and DK/K1/K2/K3 standard cannot be discriminated in Automatic Standard Recognition Search mode because the same frequency is used for the mono IF carrier.*

### AUTOSTD\_STANDARD\_DETECT    Auto standard check standard

7	6	5	4	3	2	1	0
0	NICAM_C4_OFF	NICAM_GAP_M ODE	NICAM_MONO_ IN	LDK_SCK	I_SCK	BG_SCK	MN_SCK
R/W							

**Address:**        0x8B

**Type:**            R/W

**Reset:**            0x2F

[7] Reserved.

[6] 0: Autostandard considers the C4 bit for MONO backup  
1: Autostandard ignores the C4 bit for MONO backup

[5] 0: NICAM, fast search  
1: NICAM, slow search (no perturbations on LEFT channel in search mode)

[4] 0: The MONO backup for NICAM comes from the internal demodulator  
1: The MONO backup for NICAM comes from the MONO input

[3] L/L' or D/K mono standard enable:  
0: Disabled  
1: Enabled

[2] I mono standard enable:  
0: Disabled  
1: Enabled

[1] B/G mono standard enable:  
0: Disabled  
1: Enabled

[0] M/N mono standard enable:  
0: Disabled  
1: Enabled

**Note:** *Autostandard is off when all mono standards are disabled (LDK\_SCK = 0, I\_SCK = 0, BG\_SCK = 0 and MN\_SCK = 0).*



**AUTOSTD\_STEREO\_DETECT    Auto standard check stereo**

7	6	5	4	3	2	1	0
LDK_ZWT3	LDK_ZWT2	LDK_ZWT1	LDK_NIC	I_NIC	BG_ZWT	BG_NIC	MN_ZWT
R/W							

**Address:** 0x8C**Type:** R/W**Reset:** 0x1F

- [7] D/K3 Zweiton (A2\*) stereo standard enable:  
0: Disabled  
1: Enabled
- [6] D/K2 Zweiton (A2\*) stereo standard enable:  
0: Disabled  
1: Enabled
- [5] D/K1 Zweiton (A2\*) stereo standard enable:  
0: Disabled  
1: Enabled
- [4] D/K NICAM stereo standard enable:  
0: Disabled  
1: Enabled
- [3] I NICAM stereo standard enable:  
0: Disabled  
1: Enabled
- [2] B/G Zweiton (A2) standard enable:  
0: Disabled  
1: Enabled
- [1] B/G NICAM standard enable:  
0: Disabled  
1: Enabled
- [0] M/N Zweiton (A2+) standard enable:  
0: Disabled  
1: Enabled

**Note:** *Stereo standard covers all transmission modes (stereo or multilanguage) of the NICAM or Zweiton (A2, A2\* or A2+) system.*

**AUTOSTD\_TIMERS****Detection time-out**

7	6	5	4	3	2	1	0
FM_TIME[1:0]		NICAM_TIME[2:0]			ZWEITON_TIME[2:0]		
R/W							

**Address:** 0x8D**Type:** R/W**Reset:** 0xA4

[7:6] FM/AM detection time-out:

00 : 16 ms  
 01 : 32 ms  
 10 : 48 ms (default)  
 11 : 64 ms

[5:3] NICAM detection time-out:

000: 96 ms  
 001: 128 ms  
 010: 160 ms  
 011: 192 ms  
 100: 224 ms (default)  
 101: 256 ms  
 110: 288 ms  
 111: 320 ms

[2:0] Zweiton detection time-out:

000: forbidens  
 001: 512 ms  
 010: 768 ms  
 011: 1024 ms  
 100: 1280 ms (default)  
 101: 1536 ms  
 110: 1792 ms  
 111: 2040 ms

**Note:** *The time-out default value is optimum and does not normally need to be changed.*

**AUTOSTD\_STATUS                      Detection standard status**

7	6	5	4	3	2	1	0
STEREO_ID	STEREO_OK	MONO_OK	AUTOSTD_ON	STEREO_SID[1:0]		MONO_SID[1:0]	
R							

**Address:**            0x8E

**Type:**                R

**Reset:**                0x00

- [7] Stereo mode detection flag activated when all of the following conditions are true:
  - 1. Stereo standard coming from the demodulator is selected on the Loudspeakers output
  - 2. Stereo transmission modes are:
    - Zweiton stereo carrier and stereo modulation (indifferently German or Korean standard)
    - NICAM stereo with backup (CBI = 1000)
    - NICAM stereo with no backup (CBI = 0000)
  - 3. Stereo is selected for loudspeaker output (bit LS\_LANGUAGE[1:0])
- [6] Stereo standard recognition status:
  - 0: Stereo standard not detected
  - 1: Stereo standard detected
- [5] Mono standard recognition status:
  - 0: Mono standard not detected
  - 1: Mono standard detected
- [4] Automatic Standard Recognition System Status
  - 0: Automatic Standard Recognition System is OFF
  - 1: Automatic Standard Recognition System is ON
- [3:0] Identification of the detected TV sound standard. See [Table 19](#).

**Table 19. TV sound standards**

System	Mono sound (MHz)	MONO_SID [1:0]	LDK_SW	DK_DEV [1:0]	Stereo sound (MHz)	STEREO_SID [1:0]
M/N	4.5 (FM 27k)	00	X	XX	4.724 (Zweiton A2+)	00
B/G	5.5 (FM 50k)	01	X	XX	5.85 (NICAM 40%)	00
			X	XX	5.742 (Zweiton A2)	01
I	6.0 (FM 50k)	10	X	XX	6.552 (NICAM 100%)	00

Table 19. TV sound standards (continued)

System	Mono sound (MHz)	MONO_SID [1:0]	LDK_SW	DK_DEV [1:0]	Stereo sound (MHz)	STEREO_SID [1:0]	
L	6.5 (AM)	11	1	XX	5.85 (NICAM 40%)	00	
D/K	6.5 (FM 50k)		0		00	5.85 (NICAM 40%)	00
	6.5 (FM 200k)				01		
	6.5 (FM 350k)				10		
	6.5 (FM 500k)				11		
D/K1/K2/K3	6.5 (FM 50k)		0	XX	5.85 (NICAM 40%)	00	
			0	XX	6.258 (Zweiton A2*)	01	
			0	XX	6.742 (Zweiton A2*)	10	
			0	XX	5.742 (Zweiton A2*)	11	

Note: X means not important.

## 12.12 Audio preprocessing and selection

### DC\_REMOVAL\_INPUT DC removal

7	6	5	4	3	2	1	0
0	0	0	0	0	DC_SCART	DC_NICAM	DC_DEMOD
R/W							

**Address:** 0x90

**Type:** R/W

**Reset:** 0x07

[7:3] Reserved.

[2] 0: SCART input, DC removal inactive

1: SCART input, DC removal active

[1] 0: NICAM input, DC removal inactive

1: NICAM input, DC removal active

[0] 0: FM input, DC removal inactive

1: FM input, DC removal active

**DC\_REMOVAL\_L** **FM DC offset left**

7	6	5	4	3	2	1	0
DC_REMOVAL_L[7:0]							
R							

**Address:** 0x91**Type:** R**Reset:** 0x00

[7:0] Displays (in two's complement format) the FM (or AM) DC offset level after demodulation on channel 1 (and removed automatically).

In FM mode, the DC offset value gives a direct value of the carrier frequency offset which is used to compensate the DCO with the CAROFFSET1 value in the event of an out-of-standard offset. The range and the resolution depend upon the FM bandwidth programmed defined in register BCOEFF1. See [Table 20](#).

**DC\_REMOVAL\_R** **FM DC offset right**

7	6	5	4	3	2	1	0
DC_REMOVAL_R[7:0]							
R							

**Address:** 0x92**Type:** R**Reset:** 0x00

[7:0] Displays (in two's complement format) the FM (or AM) DC offset level after demodulation on channel 2 (and removed automatically).

In FM mode, the DC offset value gives a direct value of the carrier frequency offset which is used to compensate the DCO with the CAROFFSET2 value in the event of an out-of-standard offset. The range and the resolution depend upon the FM bandwidth programmed defined in register BCOEFF2. See [Table 20](#).

**Table 20. DC\_REMOVAL\_L/R range and resolution**

FM mode	Range (kHz)	Resolution (kHz)
Small	± 96	0.750
Standard & A2 standard	± 192	1.5
Medium	± 384	3
Large	± 768	6

**PRESCALE\_SELECT****AM/FM prescaling select**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	AM_FM_SELECT
R/W							

**Address:** 0x93**Type:** R/W**Reset:** 0x00

[7:1] Reserved.

*Note: The following register bit is controlled by Autostandard and is forced by default to read-only mode.*

[0] 0: FM prescale is applied to demodulator channels

1: AM prescale is applied to demodulator channels

**PRESCALE\_AM****AM prescaling**

7	6	5	4	3	2	1	0
0	PRESCALE_AM						
R/W							

**Address:** 0x94**Type:** R/W**Reset:** 0x00

[7] Reserved.

[6:0] -12 to + 24 dB AM prescaling to normalize the AM demodulated signal level before audio processing. Auto level control can be implemented by I<sup>2</sup>C software using the peak level detector. (Default value = 0 dB)

	<u>G (dB)</u>		<u>G (dB)</u>
0110000	+24	1101100	-10
0101111	+23.5	1101011	-10.5
0101110	+23	1101010	-11
0101101	+22.5	1101001	-11.5
0101100	+22	1101000	-12
	and so on.		

**PRESCALE\_FM** **FM prescaling**

7	6	5	4	3	2	1	0
0	PRESCALE_FM						
R/W							

**Address:** 0x95  
**Type:** R/W  
**Reset:** 0x0C

[7] Reserved.

[6:0] -12 to + 24 dB FM prescaling to normalize the FM demodulated signal level before audio processing. Auto level control can be implemented by I<sup>2</sup>C software using the peak level detector. (Default value = +6 dB)

	<u>G (dB)</u>		<u>G (dB)</u>
0110000	+24	1101100	-10
0101111	+23.5	1101011	-10.5
0101110	+23	1101010	-11
0101101	+22.5	1101001	-11.5
0101100	+22	1101000	-12
	and so on.		

**PRESCALE\_NICAM** **NICAM prescaling**

7	6	5	4	3	2	1	0
0	PRESCALE_NICAM						
R/W							

**Address:** 0x96  
**Type:** R/W  
**Reset:** 0x00

[7] Reserved.

[6:0] -6 to + 24 dB NICAM prescaling to normalize the NICAM demodulated signal level before audio processing. Auto level control can be implemented by I<sup>2</sup>C software using the peak level detector. (Default value = +13 dB)

	<u>G (dB)</u>		<u>G (dB)</u>
0110000	+24	1111000	-4
0101111	+23.5	1110111	-4.5
0101110	+23	1110110	-5
0101101	+22.5	1110101	-5.5
0101100	+22	1110100	-6
	and so on.		

**PRESCALE\_SCART**                      **SCART prescaling**

7	6	5	4	3	2	1	0
0	0	PRESCALE_SCART					
R/W							

**Address:** 0x97**Type:** R/W**Reset:** 0x00

[7:6] Reserved.

[5:0] -12 to +12 dB SCART prescaling to normalize the SCART signal level before audio processing. Auto level control can be implemented by I<sup>2</sup>C software using the peak level detector. (Default value = 0 dB)

	<u>G (dB)</u>		<u>G (dB)</u>
011000	+12	101100	-10
010111	+11.5	101011	-10.5
010110	+11	101010	-11
010101	+10.5	101001	-11.5
010100	+10	101000	-12
	and so on.		

**PRESCALE\_I2S\_0**                      **I2S\_0 prescaling**

7	6	5	4	3	2	1	0
0	0	PRESCALE_I2S_0[5:0]					
R/W							

**Address:** 0x98**Type:** R/W**Reset:** 0x00

[7:6] Reserved.

[5:0] -12 to +12 dB I2S\_0 prescaling to normalize the I2S\_0 signal level before audio processing. Auto level control can be implemented by I<sup>2</sup>C software using the peak level detector. (Default value = 0 dB)

	<u>G (dB)</u>		<u>G (dB)</u>
011000	+12	101100	-10
010111	+11.5	101011	-10.5
010110	+11	101010	-11
010101	+10.5	101001	-11.5
010100	+10	101000	-12
	and so on.		



**PRESCALE\_I2S\_1** **I<sup>2</sup>S1 prescaling**

7	6	5	4	3	2	1	0
0	0	PRESCALE_I2S_1[5:0]					
R/W							

**Address:** 0x99  
**Type:** R/W  
**Reset:** 0x00

[7] Reserved.

[6] -12 to + 12 dB I2S\_1 prescaling to normalize the I2S\_1 signal level before audio processing. Auto level control can be implemented by I<sup>2</sup>C software using the peak level detector. (Default value = 0 dB)

	<u>G (dB)</u>		<u>G (dB)</u>
011000	+12	101100	-10
010111	+11.5	101011	-10.5
010110	+11	101010	-11
010101	+10.5	101001	-11.5
010100	+10	101000	-12

and so on.

**PRESCALE\_I2S\_2** **I<sup>2</sup>S2 prescaling**

7	6	5	4	3	2	1	0
0	0	PRESCALE_I2S_2[5:0]					
R/W							

**Address:** 0x9A  
**Type:** R/W  
**Reset:** 0x00

[7:6] Reserved.

[5:0] -12 to + 12 dB I2S\_2 prescaling to normalize the I2S\_2 signal level before audio processing. Auto level control can be implemented by I<sup>2</sup>C software using the peak level detector. (Default value = 0 dB)

	<u>G (dB)</u>		<u>G (dB)</u>
011000	+12	101100	-10
010111	+11.5	101011	-10.5
010110	+11	101010	-11
010101	+10.5	101001	-11.5
010100	+10	101000	-12

etc.

**DEEMPHASIS\_DEMATRIX**    **De-emphasis-dematrix**

7	6	5	4	3	2	1	0
0	0	NICAM_ DEMATRIX	NICAM_ DEEMPH_B YPASS	FM_DEMATRIX		FM_DEEMP H_BYPASS	FM_DEEMP H_SW
R/W							

**Address:**        0x9B**Type:**            R/W**Reset:**            0x00

[7:6] Reserved.

[5] Dematrixing for NICAM demodulator input:

00: L=ch0, R=ch1

01: L=ch1, R=ch0

[4] 0: NICAM de-emphasis is not bypassed.

1: NICAM de-epmhasis is bypassed.

*Note: The following register bits are controlled by Autostandard and are forced by default to read-only mode.*

[3:2] Dematrixing for FM demodulator input:

00: L=ch0, R=ch1

01: L=ch0+ch1, R=ch0-ch1

10: L=2ch0-ch1, R=ch1

11: L=(ch0+ch1)/2, R=(ch0-ch1)/2

[1] 0: FM de-emphasis is not bypassed.

1: FM de-epmhasis is bypassed.

[0] 0: 50  $\mu$ s FM de-emphasis.1: 75  $\mu$ s FM de-epmhasis.

**PEAK\_DET\_INPUT****Peak detector input source**

7	6	5	4	3	2	1	0
PEAK_LOCATIO N	0	PEAK_L_R_RANGE				PEAK_DET_INPUT[1:0]	
R/W							

**Address:** 0xD9**Type:** R/W**Reset:** 0x00

[7] Peak detector location:

0: Peak detector placed between FM/NICAM dematrix and audio matrix or between I<sup>2</sup>S Prescale and DownMix

1: Peak detector placed before DC removal (for input saturation detection)

[6] Reserved.

[5:2] Peak L-R range:

0000 : 0 dBFS to -42 dBFS

0001 : -6 dBFS to -48 dBFS

0010 : -12 dBFS to -54 dBFS

0011 : -18 dBFS to -60 dBFS

...

[1:0] Peak level detector source selection:

00: AM/FM or I<sup>2</sup>S 001: NICAM or I<sup>2</sup>S 110: SCART or I<sup>2</sup>S 2**PEAK\_DET\_L****Peak level detector status (L channel)**

7	6	5	4	3	2	1	0
OVERLOAD_L	PEAK_L[6:0]						
R							

**Address:** 0x9E**Type:** R**Reset:** 0x00

[7] Memorize overload on the peak detection. This field can be reset.

[6:0] Displays the **absolute peak level** of the audio source selected. The measured value is updated continuously every 64 ms. The range varies linearly from the full scale (0 dB) down to 1/256 of the full scale (-48 dB).

In AM/FM mono mode, only the PEAK\_L[7:0] value must be taken into account.

In FM mono mode, the audio peak level range depends upon the programmed FM bandwidth. The unique difference is that the measurement is done after sound pre-processing (DC offset removal, prescaling, de-emphasis and dematrixing).

In FM stereo mode, the maximum value may be used to check if the incoming signal level is correctly adjusted by the prescaling factor or if there are no FM overmodulation problems (clipping).

Programmable values are listed in [Table 20](#).

**PEAK\_DET\_R****Peak level detector status (R channel)**

7	6	5	4	3	2	1	0
OVERLOAD_R	PEAK_R[6:0]						
R/W							

**Address:** 0X9F

**Type:** R/W

**Reset:** 0x00

[7] Memorize overload on the peak detection. This field can be reset.

[6:0] Displays the **Absolute Peak Level** of the audio source selected. The measured value is updated continuously every 64 ms. The range varies linearly from the full scale (0 dB) down to 1/256 of the full scale (-48 dB).

For more information, refer to register [PEAK\\_DET\\_L](#)

**PEAK\_DET\_L\_R****Peak level detector status (L - R)**

7	6	5	4	3	2	1	0
OVERLOAD_L_R	PEAK_L_R[6:0]						
R							

**Address:** 0xA0

**Type:** R

**Reset:** 0x00

[7] Memorize overload on the peak detection. This field can be reset.

[6:0] Displays the **Difference between L and R (L - R) channels** for the audio source selected.

For more information, refer to register [PEAK\\_DET\\_L](#).

## 12.13 Matrixing

### AUDIO\_MATRIX\_INPUT      Audio matrix input selection

7	6	5	4	3	2	1	0
0	0	0	0	0	SCART_ INPUT_ SOURCE	HP_INPUT_ SOURCE	LS_INPUT_ SOURCE
R/W							

**Address:**      0xA2

**Type:**        R/W

**Reset:**        0x00

[7:3] Reserved.

[2] Select input source for SCART output:

0: Demod  
1: SCART input

[1] Select input source for HP output:

0: Demod  
1: SCART input

[0] Select input source for LS output:

0: Demod  
1: SCART input

### AUDIO\_MATRIX\_CONFIG      Audio matrix configuration

7	6	5	4	3	2	1	0
0	0	0	SCART_ MATRIX	DEMOM_MATRIX[3:0]			
R/W							

**Address:**      0xA3

**Type:**        R/W

**Reset:**        0x00

[7:5] Reserved.

[4] Indicates the SCART input signal matrixing (see [Table 22](#)).

*Note:* The following register bits are controlled by Autostandard and are forced by default to read-only mode.

[3:0] Indicates the demod input signal matrixing (see [Table 21](#).)

Table 21. Demod matrix

Input mode	Language -> demod_m x	Stereo		Mono A		Mono B		Mono C		Backup mode
		L	R	L	R	L	R	L	R	
<b>Mono AM/FM with backup</b>	0000	FM		FM		FM		FM		
<b>Mono AM/FM no backup</b>	0001	-		-		-		FM		
<b>Zwt St</b>	0100	FM_L	FM_R	$(FM\_L + FM\_R)/2$		$(FM\_L + FM\_R)/2$		$(FM\_L + FM\_R)/2$		
<b>Zwt Dual</b>	0101	FM_M1	FM_M2	FM_M1		FM_M2		$(FM\_M1 + FM\_M2)/2$		
<b>NICAM Mn, backup</b>	1000	NIC_M1		NIC_M1		NIC_M1		FM		Mono AM/FM with backup
<b>NICAM Dual backup</b>	1001	NIC_M1	NIC_M2	NIC_M1		NIC_M2		FM		Mono AM/FM with backup
<b>NICAM St, backup</b>	1010	NIC_L	NIC_R	$(NIC\_L + NIC\_R)/2$		$(NIC\_L + NIC\_R)/2$		FM		Mono AM/FM with backup
<b>NICAM Mn, no backup</b>	1100	NIC_M1		NIC_M1		NIC_M1		FM		Mono AM/FM no backup
<b>NICAM Dual, no backup</b>	1101	NIC_M1	NIC_M2	NIC_M1		NIC_M2		FM		Mono AM/FM no backup
<b>NICAM St, no backup</b>	1110	NIC_L	NIC_R	$(NIC\_L + NIC\_R)/2$		$(NIC\_L + NIC\_R)/2$		FM		Mono AM/FM no backup

Note: Switching between Stereo and Forced Mono modes can be done using  $(FM\_L + FM\_R)/2$  or  $(NIC\_L + NIC\_R)/2$  configurations.

**Table 22. SCART Matrix**

SCART_M X	Stereo		Mono A		Mono B		Mono C	SCART_M X
	Left	Right	Left	Right	Left	Right	Left	
0	SCART_L	SCART_R	SCART_L		SCART_R		(SCART_L + SCART_R) / 2	0
1	SCART_R	SCART_L	SCART_R		SCART_L		(SCART_L + SCART_R) / 2	1

**AUDIO\_MATRIX\_LANGUAGE      Audio matrix language selection**

7	6	5	4	3	2	1	0
MUTE_STEREO	MUTE_ALL	SCART_LANGUAGE[1:0]		HP_LANGUAGE[1:0]		LS_LANGUAGE[1:0]	
R/W							

**Address:**      0xA4

**Type:**      R/W

**Reset:**      0x00

- [7] Mute outputs with stereo signal input
- [6] Mute all outputs
- [5:4] Select language for SCART output
- [3:2] Select language for HP output
- [1:0] Select language for LS output
  - 00: stereo
  - 01: mono A
  - 10: mono B
  - 11: mono C

**DOWNMIX\_IN\_MODE      DownMix in mode**

7	6	5	4	3	2	1	0
0	0	0	0	LFE_IN	MIX_IN_MODE[2:0]		
R/W							

**Address:**      0xA6

**Type:**      R/W

**Reset:**      0x02

- [7:4] Reserved
- [3] 0: LFE signal is not inputted throught the DownMix block  
1: LFE signal is inputted throught the DownMix block

[2:0] see [Table 23](#)

**Table 23. DownMix IN modes**

Parameter coding (decimal format)	Parameter field label	Function
0	MODE11	Mode not used in STV82x7
1	MODE10	1/0 (C)
2	MODE20	2/0 (L,R)
3	MODE30	3/0 (L,R,C)
4	MODE21	2/1 (L,R,S)
5	MODE31	3/1 (L,R,C,S)
6	MODE22	2/2 (L,R,Ls,Rs)
7	MODE32	3/2 (L,R,C,Ls,Rs)

**DOWNMIX\_OUT\_MODE DownMix out mode**

7	6	5	4	3	2	1	0
0	HP_MODE[1:0]		SCART_MODE[1:0]		LS_OUT_MODE[2:0]		
R/W							

**Address:** 0xA7

**Type:** R/W

**Reset:** 0x4A

[7] Reserved.

[6:5] See [Table 24](#).

[4:3] See [Table 25](#).

[2:0] See [Table 25](#).

**Table 24. DownMix SCART/HP modes**

Parameter coding (decimal format)	Parameter field label	Function
0	MIX_VCR_OFF	Switch off the VCR table setup
1	MIX_VCR_PROLOGIC	VCR table setup for Tape outputs (for later decoding by a Dolby Prologic decoder - Lt,Rt)
2	MIX_VCR_STEREO	VCR table setup for Stereo and headphone listening (Lo,Ro)
3	MIX_COSTOM	reserved



Table 25. DownMix LS OUT modes

Parameter coding (decimal format)	Parameter field label	Function
0	MODE20t	2/0 Dolby Surround (Lt,Rt)
1	MODE10	1/0 (C)
2	MODE20	2/0 (L,R)
3	MODE30	3/0 (L,R,C)
4	MODE21	2/1 (L,R,S)
5	MODE31	3/1 (L,R,C,S)
6	MODE22	2/2 (L,R,Ls,Rs)
7	MODE32	3/2 (L,R,C,Ls,Rs)

### DOWNMIX\_DUAL\_MODE      DownMix dual mode configuration

7	6	5	4	3	2	1	0
0	DUAL_ON	LS_DUAL_SELECT[1:0]	SCART_DUAL_SELECT[1:0]			HP_DUAL_SELECT[1:0]	
R/W							

**Address:**      0xA8

**Type:**        R/W

**Reset:**        0x00

[7] Reserved.

[6] 0: Dual mode disable  
1: Dual mode enable

[5:4] Dual mono mode on LS output:  
00: LS dual stereo  
01: LS dual left mono  
10: LS dual right mono  
11: LS dual mixed

[3:2] Dual mono mode on SCART output:  
00: SCART dual stereo  
01: SCART dual left mono  
10: SCART dual right mono  
11: SCART dual mixed

[1:0] Dual mono mode on HP output:  
00: HP dual stereo  
01: HP dual left mono  
10: HP dual right mono  
11: HP dual mixed

**DOWNMIX\_CONFIG****DownMix configuration**

7	6	5	4	3	2	1	0
0	0	SRND_FACTOR[1:0]	CENTER_FACTOR[1:0]	LR_UPMIX	NORMALIZE		
R/W							

**Address:** 0xA9**Type:** R/W**Reset:** 0x01

[7:6] Reserved

[5:4] 00: -3 dB  
 01: -4.5 dB  
 10: -6 dB  
 11: -6 dB

[3:2] 00: -3 dB  
 01: -4.5 dB  
 10: -6 dB  
 11: -4.5 dB

[1] 0: Disable upmixing  
 1: Enable upmixing (DTS specified)

[0] 0: Disable normalization  
 1: Enable normalization

**12.14 Audio processing****PRO\_LOGIC2\_CONTROL****Dolby Pro Logic 2 mode configuration**

7	6	5	4	3	2	1	0
PL2_LFE	PL2_OUTPUT_DOWNMIX[2:0]	PL2_MODES[2:0]					PL2_ACTIVE
R/W							

**Address:** 0xA4**Type:** R/W**Reset:** 0x00

[7] 0: Reset the LFE channel  
 1: Bypass the LFE channel

[6:4] 000: Not applicable  
 001: Not applicable  
 010: Not applicable  
 011: 3/0 output mode (L,R,C)  
 100: 2/1 output mode (L,R,Ls - phantom)  
 101: 3/1 output mode (L,R,C,Ls)  
 110: 2/2 output mode (L,R,Ls,Rs - phantom)  
 111: 3/2 output mode (L,R,C,Ls,Rs)

- [3:1] 000: Pro Logic 1 emulation (forced if DPL version)
- 001: Virtual (DPL2 version only)
- 010: Music (DPL2 version only)
- 011: Movie (standard) (DPL2 version only)
- 100: Matrix (DPL2 version only)
- 101: Custom (DPL2 version only)
- 110: Not applicable (DPL2 version only)
- 111: Not applicable (DPL2 version only)
  
- [0] 0: Dolby Prologic 2 is not active
- 1: Dolby Prologic 2 is active

**Table 26. Prologic II decode mode configuration**

PL2 Mode	Decode mode	Dimension	Center width	Auto-balance	Panorama	Surround coherence	SUR filtering
0	Pro Logic emulation	3	0	1	0	0	2
1	Virtual	3	0	1	0	1	0
2	Music	x	x	0	x	1	1
3	Movie/Standard	3	0	1	0	0	0
4	Matrix	3	0	0	0	1	1
5	Custom	x	x	x	x	x	x

(x = user defined parameter)

**PCM\_SRND\_DELAY**

**Dolby surround delay**

7	6	5	4	3	2	1	0
0	0	0	SNRD_DELAY[4:0]				
R/W							

**Address:** 0xAB  
**Type:** R/W  
**Reset:** 0x00

- [7:5] Reserved.
- [4:0] Surround channel delay  
range: 0 to 30 (in ms)

*Note:* See [Table 18](#) for audio/video delay configuration.

**PCM\_CENTER\_DELAY**      **Dolby center delay**

7	6	5	4	3	2	1	0
0	0	0	0	CENTER_DELAY[3:0]			
R/W							

**Address:** 0xAC**Type:** R/W**Reset:** 0x00

[7] Reserved.

[6] Center channel delay  
range: 0 to 10 (in ms)*Note:* See [Table 18](#) for audio/video delay configuration.**PRO\_LOGIC2\_CONFIG**      **Dolby Pro Logic 2 configuration**

7	6	5	4	3	2	1	0
PL2_LFE	0	0	PL2_SRND_FILTER[1:0]	PL2_RS_POLARITY	PL2_PANORAMA	PL2_AUTOBALANCE	
R/W							

**Address:** 0xAD**Type:** R/W**Reset:** 0x00[7] 0: Reset the LFE channel  
1: Bypass the LFE channel

[6:5] Reserved.

[4:3] 00: 0: Off  
01: 1: Shelf filter (for music and matrix modes)  
10: 2: 7 kHz LP  
11: 3: not applicable[2] 0: Rs polarity normal  
1: Rs polarity inverted[1] 0: Panorama Off  
1: Panorama On[0] 0: Autobalance Off  
1: Autobalance On*Note:* See [Table 26](#) for programming of these bits depending on the decode mode.

**PRO\_LOGIC2\_DIMENSION    Dolby Pro Logic 2 dimension**

7	6	5	4	3	2	1	0
0	PL2_C_WIDTH			0	PL2_DIMENSION		
R/W							

**Address:**        0xAE

**Type:**            R/W

**Reset:**            0x00

- [7] Reserved.
- [6:4] Pro Logic 2 center width:
  - 000: 0, no Spread = OFF
  - 001: 20
  - 010: 28
  - 011: 36
  - 100: 54
  - 101: 62
  - 110: 69
  - 111: 90, phantom

- [3] Reserved.
- [2:0] 000: -3, most surround
  - 001: -2
  - 010: -1
  - 011: 0, neutral = OFF
  - 100: 1
  - 101: 2
  - 110: 3, most center
  - 111: Not applicable

*Note:*        See [Table 26](#) for programming of these bits depending on the decode mode.

**PRO\_LOGIC2\_LEVEL        Dolby Pro Logic 2 input level**

7	6	5	4	3	2	1	0
PL2_LEVEL							
R/W							

**Address:**        0xAF

**Type:**            R/W

**Reset:**            0x00

- [7:0] Input gain attenuation:
  - 0000 0000: 0 dB
  - 0000 0001: -0.5 dB
  - ...
  - 1111 1111: -127.5 dB

**NOISE\_GENERATOR****Pink noise generator**

7	6	5	4	3	2	1	0
10_DB_ ATTENUATE	SRIGHT_ NOISE	SLEFT_ NOISE	SUB_ NOISE	CENTER_ NOISE	RIGHT_ NOISE	LEFT_ NOISE	NOISE_ON
R/W							

**Address:** 0xB0**Type:** R/W**Reset:** 0x00

- [7] 0: Noise is output with full range  
1: Noise is output with a 10 dB attenuation
- [6] 1: Generates noise on LS right surround output
- [5] 1: Generates noise on LS left surround output
- [4] 1: Generates noise on LS subwoofer output
- [3] 1: Generates noise on LS center output
- [2] 1: Generates noise on LS right output
- [1] 1: Generates noise on LS left output
- [0] 0: Noise generation not active  
1: Noise generation is active

**TRUSRND\_CONTROL****SRS TruSurround control**

7	6	5	4	3	2	1	0
0	TRUSRND_ MONO_SRND	TRUSRND_INPUT_MODE[3:0]				TRUSRND_ MODE	TRUSRND_ ON
R/W							

**Address:** 0xB1**Type:** R/W**Reset:** 0x00

- [7] Reserved.
- [6] 0: Left mono Srnd mode  
1: Right mono Srnd mode
- [5:2] 0000: Mono  
0001: L/R stereo (SRS mode)  
0010: L/R/S (SRS mode, Prologic 1 Process)  
0011: L/R/Ls/Rs (SRS mode)  
0100: L/R/C (TruSurround mode)  
0101: L/R/C/S (TruSurround mode, Prologic 1 Process)  
0110: L/R/C/Ls/Rs (TruSurround mode)  
0111: Lt/Rt (TruSurround mode)  
1000: L/R/C/Ls/Rs (SRS mode, BS Digital Broadcast)  
1001: L/R/C/Ls/Rs (TruSurround, Prologic 2 Music mode)

- [1] 0: TruSurround mode  
1: Bypass mode
- [0] 0: TruSurround OFF  
1: TruSurround ON

Note: Using TruSurround XT:

- Implementation of TruSurround XT is done by setting the TRUSRND\_ON bit to 1.
- TruSurround XT mode must be selected by TRUSRND\_INPUT\_MODE[3:0] bits.
- Activation or non-activation of TruSurround XT must be done by using the TRUSRND\_MODE bit.

**TRUSRND\_INPUT\_GAIN      TruSurround input gain**

7	6	5	4	3	2	1	0
TRUSRND_INPUT_GAIN[7:0]							
R/W							

**Address:**      0xB6  
**Type:**        R/W  
**Reset:**        0x00

- [7:0] Input gain attenuation:  
 0000 0000: 0 dB  
 0000 0001: -0.5 dB  
 ...  
 1111 1111: -127.5 dB

**TRUSRND\_HP\_DCL      TruSurround HP dialog clarity**

7	6	5	4	3	2	1	0
0	0	0	0	0	DIALOG_CLARITY_ON	HEADPHONE_ON	0
R/W							

**Address:**      0xB7  
**Type:**        R/W  
**Reset:**        0x00

- [7:3] Reserved.
- [2] 0: Dialog clarity OFF  
1: Dialog clarity ON
- [1] Activate HP mode in TruSurround XT:  
0: HP mode OFF  
1: HP mode ON
- [0] Reserved.

**TRUSRND\_DC\_ELEVATION** TruSurround dialog clarity level

7	6	5	4	3	2	1	0
TRUSRND_DC_ELEVATION[7:0]							
R/W							

**Address:** 0xB8**Type:** R/W**Reset:** 0x0C

[7:0] Dialog clarity elevation:

0000 0000: 0 dB

0000 0001: -0.5 dB

...

1111 1111: -127.5 dB

**TRUBASS\_LS\_CONTROL** SRS TruBass LS configuration

7	6	5	4	3	2	1	0
0	0	0	0	TRUBASS_LS_SIZE[2:0]			TRUBASS_LS_ON
R/W							

**Address:** 0xBA**Type:** R/W**Reset:** 0x06

[7:4] Reserved.

[3:1] 000: LF response at 40 Hz  
 001: LF response at 60 Hz  
 010: LF response at 100 Hz  
 011: LF response at 150 Hz  
 100: LF response at 200 Hz  
 101: LF response at 250 Hz  
 110: LF response at 300 Hz  
 111: LF response at 400 Hz

[0] 0: LS TruBass OFF  
 1: LS TruBass ON



**TRUBASS\_LS\_LEVEL      SRS TruBass LS level**

7	6	5	4	3	2	1	0
TRUBASS_LS_LEVEL[7:0]							
R/W							

**Address:**      0xBB

**Type:**        R/W

**Reset:**        0x09

[7:0] Define the amount of SRS TruBass effect for LS outputs:

0000 0000: 0 dB

0000 0001: -0.5 dB

...

1111 1111: -127.5 dB

**TRUBASS\_HP\_CONTROL      SRS TruBass HP configuration**

7	6	5	4	3	2	1	0
0	0	0	0	TRUBASS_HP_SIZE[2:0]		TRUBASS_HP_ON	
R/W							

**Address:**      0xBC

**Type:**        R/W

**Reset:**        0x06

[7:4] Reserved.

- [3:1] 000: LF response at 40 Hz
- 001: LF response at 60 Hz
- 010: LF response at 100 Hz
- 011: LF response at 150 Hz
- 100: LF response at 200 Hz
- 101: LF response at 250 Hz
- 110: LF response at 300 Hz
- 111: LF response at 400 Hz

- [0] 0: HP TruBass OFF
- 1: HP TruBass ON

**TRUBASS\_HP\_LEVEL****SRS TruBass HP level**

7	6	5	4	3	2	1	0
TRUBASS_HP_LEVEL[7:0]							
R/W							

**Address:** 0xBD**Type:** R/W**Reset:** 0x09

[7:0] Defines the amount of SRS TruBass effect for HP outputs:

0000 0000: 0 dB

0000 0001: -0.5 dB

...

1111 1111: -127.5 dB

**SVC\_LS\_CONTROL****Smart volume control for LS**

7	6	5	4	3	2	1	0
0	0	0	0	SVC_LS_INPUT[1:0]	SVC_LS_AMP	SVC_LS_ON	
R/W							

**Address:** 0xBE**Type:** R/W**Reset:** 0x02

[7:4] Reserved.

[3:2] Select input for peak detection in multi-channel mode:

00: Left/Right

01: Center

10: Left/Right/Center

[1] 0: 0 dB amplification in auto-mode

1: +6 dB amplification in auto-mode

[0] 0: Manual mode(simple prescaler)

1: Automatic mode

**SVC\_LS\_TIME\_TH****Smart volume control parameters for LS**

7	6	5	4	3	2	1	0
SVC_LS_TIME[2:0]				SVC_LS_THRESHOLD[4:0] (S)			
R/W							

**Address:** 0xBF**Type:** R/W**Reset:** 0x98

[7:5] Time constant for the amplification (6 dB gain step) in automatic mode:

- 000: 30 ms
- 001: 200 ms
- 010: 500 ms
- 011: 1 s
- 100: 16 s
- 101: 32 s
- 110: 64 s
- 111: 128 s

[4:0] See [Table 27](#) and [Table 28](#).

**Table 27. Gain (threshold field) values in manual mode**

Manual mode	Gain (dB)	Manual mode	Gain (dB)
00101	+15.5	11101	-8.5
00100	+12	11100	-12
00011	+9.5	11011	-14.5
00010	+6	11010	-18
00001	+3.5	11001	-20.5
00000	0	11000	-24
11111	-2.5	10111	-26.5
11110	-6	10110	-30

**Table 28. Threshold values in automatic mode**

Automatic mode	Threshold (dB)	Automatic mode	Threshold (dB)
11111	-2.5	11010	-18
11110	-6	11001	-20.5
11101	-8.5	11000	-24
11100	-12	10111	-26.5
11011	-14.5	10110	-30

**SVC\_HP\_CONTROL**

**Smart volume control for HP**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SVC_ LHP_AMP	SVC_HP_ON
R/W							

**Address:** 0xC0

**Type:** R/W

**Reset:** 0x02

[7:2] Reserved.

[1] 0: 0 dB amplification in auto-mode  
1: +6 dB amplification in auto-mode

[0] 0: Manual mode (simple prescaler)  
1: Automatic mode

### SVC\_HP\_TIME\_TH Smart volume control parameters for HP

	7	6	5	4	3	2	1	0
	SVC_HP_TIME[2:0]			SVC_HP_THRESHOLD[4:0] (S)				
	R/W							

**Address:** 0xC1

**Type:** R/W

**Reset:** 0x98

[7:5] Time constant for the amplification (6 dB gain step) in automatic mode:

000: 30 ms  
001: 200 ms  
010: 500 ms  
011: 1 s  
100: 16 s  
101: 32 s  
110: 64 s  
111: 128 s

[4:0] See [Table 27](#) and [Table 28](#).

### SVC\_LS\_GAIN Make-up gain for SVC LS

	7	6	5	4	3	2	1	0
	0	SVC_LS_GAIN[6:0]						
	R/W							

**Address:** 0xC2

**Type:** R/W

**Reset:** 0x00

[7] Reserved.

[6:0] Set “make-up” gain applied at SVC LS output:

0000000: +0 dB  
0000001: +0.5 dB  
...  
0101110: +23 dB  
0101111: +23.5 dB  
0110000: +24 dB

**SVC\_HP\_GAIN** **Make-up gain for SVC HP**

7	6	5	4	3	2	1	0
0	SVC_HP_GAIN[6:0]						
R/W							

**Address:** 0xC3

**Type:** R/W

**Reset:** 0x00

[7] Reserved.

[6:0] Set "make-up" gain applied at SVC HP output:

- 0000000: +0 dB
- 0000001: +0.5 dB
- ...
- 0101110: +23 dB
- 0101111: +23.5 dB
- 0110000: +24 dB

**STSRND\_CONTROL** **ST WideSurround control**

7	6	5	4	3	2	1	0
0	0	0	0	0	STSRND_ STEREO	STSRND_ MODE	STSRND_ON
R/W							

**Address:** 0xC4

**Type:** R/W

**Reset:** 0x00

[7:3] Reserved.

[2] ST WideSurround mode

- 0: ST WideSurround sound in mono mode (default)
- 1: ST WideSurround sound in stereo mode

[1] ST WideSurround sound stereo mode

- 0: Movie Mode
- 1: Music Mode

[0] ST WideSurround sound enable

- 0: ST WideSurround sound is disabled
- 1: ST WideSurround sound is enabled

**STSRND\_FREQ****ST WideSurround sound frequency**

7	6	5	4	3	2	1	0
0	0	STSRND_BASS[1:0]		STSRND_MEDIUM[1:0]		STSRND_TREBLE[1:0]	
R/W							

**Address:** 0xC5**Type:** R/W**Reset:** 0x15

[7:6] Reserved.

[5:4] Defines the bass frequency effect for ST WideSurround sound. Programmable values are listed in [Table 29](#).[3:2] Defines the medium frequency effect for ST WideSurround sound in movie or mono mode (no effect in music mode). Programmable values are listed in [Table 29](#).[1:0] Defines the treble frequency effect for ST WideSurround sound in movie or mono mode (no effect in music mode). Programmable values are listed in [Table 29](#).**Table 29. Phase shifter center frequencies**

	Phase shifter center frequency		
	BASS_FREQ[1:0]	MEDIUM_FREQ[1:0]	TREBLE_FREQ[1:0]
00	40 Hz	202 Hz	2 kHz
01 (default)	90 Hz	416 Hz	4 kHz
10	120 Hz	500 Hz	5 kHz
11	160 Hz	588 Hz	6 kHz

**STSRND\_LEVEL****ST WideSurround gain**

7	6	5	4	3	2	1	0
STSRND_GAIN[7:0]							
R/W							

**Address:** 0xC6**Type:** R/W**Reset:** 0x80

[7:0] Defines the ST WideSurround Sound component gain in linear scale.

	<u>Level (%)</u>		<u>Level (%)</u>
1000 0000 (default)	100%	0000 0100	3.1%
0111 1111	99.2%	0000 0011	2.3%
0111 1110	98.4%	0000 0010	1.6%
0111 1101	97.6%	0000 0001	0.8%
.....		0000 0000	0%

**OMNISURROUND\_CONTROL      ST OmniSurround configuration**

7	6	5	4	3	2	1	0
LFE	ST_VOICE[1:0]		FRONT_ BYPASS	OMNI_SURND_INPUT_MODE[3:0]			OMNISRND_ON
R/W							

**Address:**      0xC7

**Type:**          R/W

**Reset:**         0x00

[7] 0: Do not use LFE channel  
 1: Generate LFE channel

[6:5] 00: OFF  
 01: Low  
 10: Mid  
 11: High

[4] Forced to 0

[3:1] 000: Mono  
 001: L/R stereo  
 010: L/R/S  
 110: L/R/C/Ls/Rs  
 011: L/R/Ls/Rs  
 100: L/R/C  
 101: L/R/C/S  
 111: Lt/Rt (passive matrix)

[0] 0: OmniSurround OFF  
 1: OmniSurround ON

**ST\_DYNAMIC\_BASS      ST Dynamic Bass congiguration**

7	6	5	4	3	2	1	0
BASS_LEVEL[4:0]					BASS_FREQ[1:0]		DYN_BASS_ ON
R/W							

**Address:**      0xC8

**Type:**          R/W

**Reset:**         0x00

[7:3] Set ST Dynamic Bass effect level:  
 00000: +0 dB  
 00001: +0.5 dB  
 ...  
 11101: +14.5 dB  
 11110: +15 dB  
 11111: +15.5 dB

[2:1] 00: 100 Hz cut-off frequency  
 01: 150 Hz cut-off frequency  
 10: 200 Hz cut-off frequency  
 11: Reserved

[0] 0: ST Dynamic Bass OFF  
 1: ST Dynamic Bass ON

## 12.15 5-band equalizer/bass-treble for loudspeakers

### LS\_EQ\_BT\_CTRL

### Loudspeakers equalizer control

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_EQ_BT_SW	LS_EQ_ON
R/W							

**Address:** 0xC9

**Type:** R/W

**Reset:** 0x01

[7:2] Reserved.

[1] 5-band equalizer or bass-treble selection  
 0: 5-band equalizer is selected for loudspeakers.  
 1: Bass-treble is selected for loudspeakers.

[0] 5-band equalizer/bass-treble for loudspeakers enable  
 0: 5-band equalizer/bass-teble is disabled  
 1: 5-band equalizer/bass-teble is enabled (default)

### EQ\_BANDX\_GAIN

### Loudspeakers equalizer gain for band X

7	6	5	4	3	2	1	0
EQ_BANDX							
R/W							

**Address:** 0xCA to 0xCE

**Type:** R/W

**Reset:** 0x00

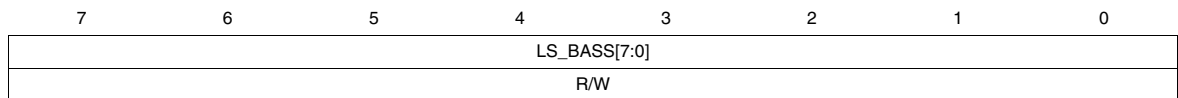
[7:0] BandX gain adjustment within a range from -12 dB to +12 dB in steps of 0.25 dB.  
 Band1: 100 Hz, Band2: 330 Hz, Band3: 1 kHz, Band4: 3.3 kHz, Band5: 10 kHz, see [Table 30](#).



**Table 30. Loudspeakers equalizer/bass-treble gain values (and headphone bass-treble gain values)**

Value	Gain G (dB)
00110000	+12
00101111	+11.75
00101110	+11.50
.....	....
00000000 (default)	0
.....	....
11010010	-11.50
11010001	-11.75
11010000	-12

**LS\_BASS\_GAIN Loudspeakers bass gain**

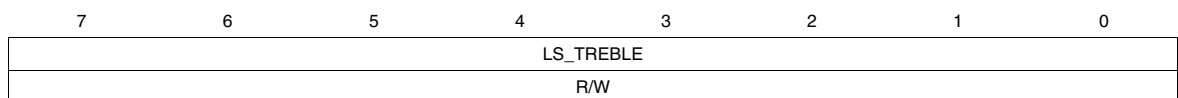


**Address:** 0xCF  
**Type:** R/W  
**Reset:** 0x00

[7:0] Bass gain adjustment within a range from -12 dB to +12 dB in steps of 0.25 dB.

*Note:* With positive bass/treble settings, internal clipping may occur even with an overall volume of less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass/treble bands to a value that, in conjunction with volume, would result in an overall positive gain.

**LS\_TREBLE\_GAIN Loudspeakers treble gain**



**Address:** 0xD0  
**Type:** R/W  
**Reset:** 0x00

[7:0] Treble gain adjustment within a range from -12 dB to +12 dB in steps of 0.25 dB.

*Note:* With positive bass/treble settings, internal clipping may occur even with an overall volume of less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to

set bass/treble bands to a value that, in conjunction with volume, would result in an overall positive gain.

## 12.16 Headphone bass-treble

### HP\_BT\_CONTROL Headphone bass-treble control

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HP_BT_ON
R/W							

**Address:** 0xD1

**Type:** R/W

**Reset:** 0x01

[7:1] Reserved.

[0] Bass-treble for headphone enable

0: Bass-treble is disabled

1: Bass-treble is enabled (default)

### HP\_BASS\_GAIN Headphone bass gain

7	6	5	4	3	2	1	0
HP_BASS_GAIN[7:0]							
R/W							

**Address:** 0xD2

**Type:** R/W

**Reset:** 0x00

[7] Gain tuning of headphone bass frequency

Gain may be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB.

Programmable values are listed in [Table 30](#).

**Note:** With positive bass/treble settings, internal clipping may occur even with an overall volume of less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass/treble bands to a value that, in conjunction with volume, would result in an overall positive gain.

**HP\_TREBLE\_GAIN**      **Headphone treble gain**

7	6	5	4	3	2	1	0
HP_TREBLE_GAIN[4:0]							
R/W							

**Address:** 0xD3**Type:** R/W**Reset:** 0x00

[7:0] Gain tuning of headphone treble frequency  
 Gain may be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB.  
 Programmable values are listed in [Table 30](#).

*Note:* With positive bass/treble settings, internal clipping may occur even with an overall volume of less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass/treble bands to a value that, in conjunction with volume, would result in an overall positive gain.

**OUTPUT\_BASS\_MNGT**      **Bass redirection**

7	6	5	4	3	2	1	0
BASS_MANAGE_ON	0	SUB_ACTIVE	GAIN_SWITCH	0	OCFG_NUM[2:0]		
R/W							

**Address:** 0xD4**Type:** R/W**Reset:** 0x80

[7] 0: BassManagement disables  
 1: BassManagement enabled

[6] Reserved.

[5] 0: Subwoofer output is disabled (only in config 2,3,4)  
 1: Subwoofer output is active

[4] 0: Level adjustment ON  
 1: Level adjustment OFF

[3] Reserved

[2:0] Select bass management configuration:  
 000: Bass management configuration 0 (refer to [Figure 9](#))  
 001: Bass management configuration 1 (refer to [Figure 10](#))  
 010: Bass management configuration 2 (refer to [Figure 11](#))  
 011: Bass management configuration 3 (refer to [Figure 12](#))  
 100: Bass management configuration 4 (refer to [Figure 13](#))

**LS\_LOUDNESS****Loudness configuration for LS**

7	6	5	4	3	2	1	0
0	LS_LOUD_THRESHOLD[2:0]			LS_LOUD_GAIN_HR[2:0]			LS_LOUD_ON
R/W							

**Address:** 0xD5**Type:** R/W**Reset:** 0x00

[7] Reserved.

[6:4] Define the volume threshold level since which loudness effect is applied :

000: 0 dB  
 001: -6 dB  
 010: -12 dB  
 011: -18 dB  
 100: -24 dB  
 101: -32 dB  
 110: -36 dB  
 111: -42 dB

[3:1] Define the amount of treble added by loudness effect:

000: 0 dB  
 001: 3 dB  
 010: 6 dB  
 011: 9 dB  
 100: 12 dB  
 101: 15 dB  
 110: 18 dB  
 111: 21 dB

[0] 0: Loudness is not active on LS output

1: Loudness is active on LS output

**HP\_LOUDNESS****Loudness configuration for HP**

7	6	5	4	3	2	1	0
0	HP_LOUD_THRESHOLD[2:0]			HP_LOUD_GAIN_HR[2:0]			HP_LOUD_ON
R/W							

**Address:** 0xD6**Type:** R/W**Reset:** 0x04

[7] Reserved.

[6:4] Define the volume threshold level since which loudness effect is applied :

- 000: 0 dB
- 001: -6 dB
- 010: -12 dB
- 011: -18 dB
- 100: -24 dB
- 101: -32 dB
- 110: -36 dB
- 111: -42 dB

[3:1] Define the amount of treble added by loudness effect:

- 000: 0 dB
- 001: 3 dB
- 010: 6 dB
- 011: 9 dB
- 100: 12 dB
- 101: 15 dB
- 110: 18 dB
- 111: 21 dB

- [0] 0: Loudness is not active on HP output
- 1: Loudness is active on HP output

## 12.17 Volume

### VOLUME\_MODES

### Set the volume modes

7	6	5	4	3	2	1	0
ANTICLIP_HP_V OL_CLAMP	ANTICLIP_LS_V OL_CLAMP	0	0	SCART_ VOLUME_ MODE	SRND_ VOLUME_ MODE	HP_ VOLUME_ MODE	LS_ VOLUME_ MODE
R/W							

**Address:** 0xD7

**Type:** R/W

**Reset:** 0xC7

[7] The output level is clamped depending on the HP bass-treble value to avoid any possible signal clipping on HP output.

- 0: Volume clamp on HP output is not active
- 1: Volume clamp on HP output is active

[6] The output level is clamped depending on the LS equalizer or LS bass-treble value to avoid any possible signal clipping on LS output.

- 0: Volume clamp on LS output is not active
- 1: Volume clamp on LS output is active

[5:4] Reserved

[3] Volume mode for SCART output:

- 0: Independent
- 1: Differential

[2] Volume mode for headphone output:

- 0: Independent
- 1: Differential

[1] Volume mode for surround output:

- 0: Independent
- 1: Differential

[0] Volume mode for LS output:

- 0: Independent
- 1: Differential

Note: 1 For the use of volume and balance control refer to [Figure 15](#) and [Figure 16](#).

2 In differential mode the left register is used for volume control and the right register is used for balance control.

### LS\_L\_VOLUME\_MSB

### Loudspeaker left volume MSB

7	6	5	4	3	2	1	0
LS_L_VOLUME_MSB							
R/W							

**Address:** 0xD8

**Type:** R/W

**Reset:** 0x98

[7] LS 10 bits volume left channel 8 MSB in independent mode or LS 10 bits volume left and right channels 8 MSB in differential mode.

See [Figure 15](#) for range values.

### LS\_L\_VOLUME\_LSB

### Loudspeaker left volume LSB

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_L_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xD9

**Type:** R/W

**Reset:** 0x00

[7:2] Reserved.

[1:0] LS 10 bits volume left channel 2 LSB in independent mode or LS 10 bits volume left and right channels 2 LSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

Note: The volume value is defined by the following formula:  
 $Vol (dB) = \text{Decimal value of } LS\_L\_VOLUME\_MSB \times 0.5 + \text{Decimal value of } LS\_L\_VOLUME\_LSB \times 0.125 - 116 \text{ dB}$  (each step is 0.125 dB).

**LS\_R\_VOLUME\_MSB****Loudspeaker right volume MSB**

7	6	5	4	3	2	1	0
LS_R_VOLUME_MSB[7:0]							
R/W							

**Address:** 0xDA**Type:** R/W**Reset:** 0x00

[7] LS 10 bits volume right channel 8 MSB in independent mode or LS 10 bits left and right balance 8 MSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

**LS\_R\_VOLUME\_LSB****Loudspeaker right volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_R_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xDB**Type:** R/W**Reset:** 0x00

[7:2] Reserved.

[1:0] LS 10 bits volume right channel 2 LSB in independent mode or LS 10 bits left and right balance 2 LSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

**LS\_C\_VOLUME\_MSB****Loudspeaker center volume MSB**

7	6	5	4	3	2	1	0
LS_C_VOLUME_MSB[7:0]							
R/W							

**Address:** 0xDC**Type:** R/W**Reset:** 0x98

[7:0] LS 10 bits volume center channel 8 MSB

See [Figure 15](#) for range values.

**LS\_C\_VOLUME\_LSB****Loudspeaker center volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_C_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xDD**Type:** R/W**Reset:** 0x00

[7] Reserved.

[6] LS 10 bits volume center channel 2 LSB

See [Figure 15](#) for range values.

*Note:* The volume value is defined by the following formula:  
 $Vol (dB) = \text{Decimal value of } LS\_C\_VOLUME\_MSB \times 0.5 + \text{decimal value of } LS\_C\_VOLUME\_LSB \times 0.125 - 116 \text{ dB}$  (each step is 0.125 dB).

**LS\_SUB\_VOLUME\_MSB****Loudspeaker subwoofer volume MSB**

7	6	5	4	3	2	1	0
LS_SUB_VOLUME_MSB[7:0]							
R/W							

**Address:** 0xDE**Type:** R/W**Reset:** 0x98

[7:0] LS 10 bits volume subwoofer channel 8 MSB

See [Figure 15](#) for range values.**LS\_SUB\_VOLUME\_LSB****Loudspeaker subwoofer volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_SUB_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xDF**Type:** R/W**Reset:** 0x00

[7:2] Reserved.

[1:0] LS 10 bits volume subwoofer channel 2 LSB

See [Figure 15](#) for range values.



*Note:* The volume value is defined by the following formula:  
 $Vol (dB) = \text{Decimal value of } LS\_SUB\_VOLUME\_MSB \times 0.5 + \text{decimal value of } LS\_SUB\_VOLUME\_LSB \times 0.125 - 116 \text{ dB}$  (each step is 0.125 dB).

### LS\_SL\_VOLUME\_MSB Loudspeaker left surround volume MSB

7	6	5	4	3	2	1	0
LS_SL_VOLUME_MSB[7:0]							
R/W							

**Address:** 0xE0

**Type:** R/W

**Reset:** 0x98

[7:0] LS 10 bits volume left surround channel 8 MSB in independent mode or LS 10 bits left and right surround volume 8 MSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

### LS\_SL\_VOLUME\_LSB Loudspeaker left surround volume LSB

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_LS_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xE1

**Type:** R/W

**Reset:** 0x00

[7:2] Reserved.

[1:0] LS 10 bits volume left surround channel 2 LSB in independent mode or LS 10 bits left and right surround volume 2 LSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

*Note:* The volume value is defined by the following formula:  
 $Vol (dB) = \text{Decimal value of } LS\_SL\_VOLUME\_MSB \times 0.5 + \text{Decimal value of } LS\_SL\_VOLUME\_LSB \times 0.125 - 116 \text{ dB}$  (each step is 0.125 dB).

### LS\_SR\_VOLUME\_MSB Loudspeaker right surround volume MSB

7	6	5	4	3	2	1	0
LS_SR_VOLUME_MSB[7:0]							
R/W							

**Address:** 0xE2

**Type:** R/W

**Reset:** 0x00

[7:0] LS 10 bits volume right channel 8 MSB in independent mode or LS 10 bits surround left and right balance 8 MSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

### LS\_SR\_VOLUME\_LSB Loudspeaker right surround volume LSB?

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_SR_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xE3

**Type:** R/W

**Reset:** 0x00

[7] Reserved.

[6] LS 10 bits volume Right channel 8 MSB in independent mode or LS 10 bits surround Left and Right balance 2 LSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

*Note:* The volume value is defined by the following formula:  
 $Vol (dB) = \text{Decimal value of } LS\_SR\_VOLUME\_MSB \times 0.5 + \text{Decimal value of } LS\_SR\_VOLUME\_LSB \times 0.125 - 116 \text{ dB}$  (each step is 0.125 dB).

### LS\_MASTER\_VOLUME\_MSB Loudspeaker master volume MSB

7	6	5	4	3	2	1	0
LS_MASTER_VOLUME_MSB[7:0]							
R/W							

**Address:** 0xE4

**Type:** R/W

**Reset:** 0xE8

[7] LS 10 bits volume Master channel 8 MSB

See [Figure 15](#) for range values.

### LS\_MASTER\_VOLUME\_LSB Loudspeaker master volume LSB

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_MASTER_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xE5

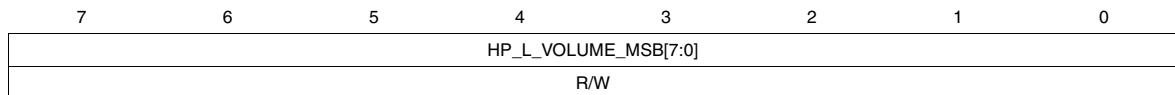
**Type:** R/W

**Reset:** 0x00

- [7] Reserved.
- [6] LS 10 bits volume master channel 2 LSB  
See [Figure 15](#) for range values.

**Note:** *The volume value is defined by the following formula:  
 $Vol (dB) = \text{Decimal value of } LS\_MASTER\_VOLUME\_MSB \times 0.5 + \text{Decimal value of } LS\_MASTER\_VOLUME\_LSB \times 0.125 - 116 \text{ dB (each step is } 0.125 \text{ dB)}$ .*

**HP\_L\_VOLUME\_MSB                      Headphone left volume MSB**

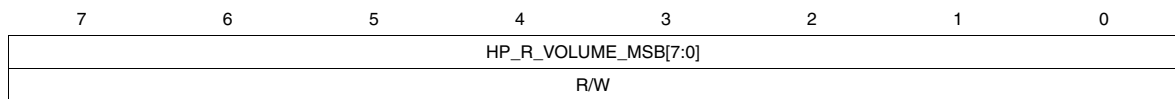


**Address:**            0xE6  
**Type:**                R/W  
**Reset:**                0x98

- [7] HP 10 bits volume left channel 8 MSB in independent mode or HP 10 bits left and right volume 8 MSB in differential mode.  
See [Figure 15](#) or [Figure 16](#).

**Note:** *The volume value is defined by the following formula:  
 $Vol (dB) = \text{Decimal value of } HP\_L\_VOLUME\_MSB \times 0.5 + \text{Decimal value of } HP\_L\_VOLUME\_LSB \times 0.125 - 116 \text{ dB (each step is } 0.125 \text{ dB)}$ .*

**HP\_L\_VOLUME\_LSB                      Headphone left volume LSB**



**Address:**            0xE7  
**Type:**                R/W  
**Reset:**                0x00

- [7:2] Reserved
- [7:0] HP 10 bits volume left channel 2 LSB in independent mode or HP 10 bits left and right volume 2 LSB in differential mode.  
See [Figure 15](#) or [Figure 16](#).

**Note:** *The volume value is defined by the following formula:  
 $Vol (dB) = \text{decimal value of } HP\_L\_VOLUME\_MSB \times 0.5 + \text{decimal value of } HP\_L\_VOLUME\_LSB \times 0.125 - 116 \text{ dB (each step is } 0.125 \text{ dB)}$ .*

**HP\_R\_VOLUME\_LSB****Headphone right volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HP_R_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xE9**Type:** R/W**Reset:** 0x00

[7:2] Reserved.

[1:0] HP 10 bits volume right channel 2 LSB in independent mode or HP 10 bits left and right balance 2LSB in differential mode.

See [Figure 15](#) or [Figure 16](#).**HP\_R\_VOLUME\_MSB****Headphone right volume MSB****Address:** 0xE8**Type:** R/W**Reset:** 0000 0000

7	6	5	4	3	2	1	0
HP_R_VOLUME_MSB[7:0]							
R/W							

[7:0] 8 MSBs of the 10-bit right headphone volume

**SCART\_L\_VOLUME\_MSB****Headphone left volume MSB**

7	6	5	4	3	2	1	0
SCART_L_VOLUME_MSB[7:0]							
R/W							

**Address:** 0xEA**Type:** R/W**Reset:** 0xDD

[7:0] SCART 10 bits volume left channel 8 MSB in independent mode or SCART10 bits left and right volume 8 MSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

**SCART\_L\_VOLUME\_LSB      tHeadphone left volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SCART_L_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xEB**Type:** R/W**Reset:** 0x00

[7:2] Reserved.

[1:0] SCART 10 bits volume left channel 2 LSB in independent mode or SCART10 bits left and right volume 2 LSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

*Note:*      *The volume value is defined by the following formula:*  
*Vol (dB) = Decimal value of SCART\_L\_VOLUME\_MSB x 0.5 + decimal value of*  
*SCART\_L\_VOLUME\_LSB x 0.125 - 116 dB (each step is 0.125 dB).*

**SCART\_R\_VOLUME\_MSB      SCART right volume MSB**

7	6	5	4	3	2	1	0
SCART_R_VOLUME_MSB[7:0]							
R/W							

**Address:** 0xEC**Type:** R/W**Reset:** 0xDD

[7:0] SCART 10 bits volume Right channel 8 MSB in independent mode or SCART10 bits Left and Right balance 8 MSB in differential mode.

See [Figure 15](#) or [Figure 16](#).**SCART\_R\_VOLUME\_LSB      SCART right volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SCART_R_VOLUME_LSB[1:0]	
R/W							

**Address:** 0xED**Type:** R/W**Reset:** 0x00

[7:2] Reserved.

[1:0] SCART 10 bits volume Right channel 2 LSB in independent mode or SCART10 bits Left and Right balance 2 LSB in differential mode.

See [Figure 15](#) or [Figure 16](#).

## 12.18 Beeper

### BEEPER\_ON Beeper activation

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	BEEPER_ON
R/W							

**Address:** 0xEE

**Type:** R/W

**Reset:** 0x00

[7:1] Reserved.

[0] Beeper enable:

0: Beeper muted (default.)

1: Beeper enabled.

### BEEPER\_MODE Beeper control

7	6	5	4	3	2	1	0
0	0	0	BEEPER_DURATION	BEEPER_PULSE	BEEPER_PATH		
R/W							

**Address:** 0xEF

**Type:** R/W

**Reset:** 0x03

[7:5] Reserved.

[4:3] Define beeper duration when set to pulse mode.

[2] Set beeper pulse mode:

0: Pulse mode selected.

1: Continuous mode selected.

[1:0] Set the output channels when beeper is active:

00: no channels.

01: Loudspeakers only.

10: Headphone only.

11: Loudspeakers and Headphone selected.

**BEEPER\_FREQ\_VOL**                      **Beeper frequency and volume settings**

	7	6	5	4	3	2	1	0
BEEP_FREQ[2:0]				BEEP_VOL[4:0]				
R/W								

**Address:**        0xF0  
**Type:**            R/W  
**Reset:**           0x70

[7:5] Defines the frequency of the beeper tone from 62.5 Hz to 8 kHz in octaves:

- 000: 62.5 Hz
- 001: 125 Hz
- 010: 250 Hz
- 011: 500 Hz (default)
- 100: 1 kHz
- 101: 2 kHz
- 110: 4 kHz
- 111: 8 kHz

[4:0] Defines the beeper volume from 0 to -93 dB in steps of 3 dB:

- 11111: 0 dB (1 V<sub>RMS</sub>)     ...
- 11110: -3 dB                00011: -84 dB
- 11101: -6 dB                00010: -87 dB
- ...                            00001: -90 dB
- 10000: -48 dB (default) 00000: -93 dB

**12.19 Mute**

**MUTE\_DIGITAL**                      **Digital mute configuration**

	7	6	5	4	3	2	1	0
AUTOSTD_MUTE_ON	0	0	SCART_D_MUTE	SRND_HP_D_MUTE	SUB_D_MUTE	C_D_MUTE	LS_D_MUTE	
R/W								

**Address:**        0xF1  
**Type:**            R/W  
**Reset:**           0x9F

[7] 0: Autostandard can not mute outputs  
 1: Autostandard can mute outputs when no signal is detected

[6:5] Reserved

[4] SCART left/right digital soft mute  
 0: Signal un-muted  
 1: Signal muted

[3] LS surround/HP left/right digital soft mute

- 0: Signal un-muted
- 1: Signal muted

[2] LS subwoofer digital soft mute

- 0: Signal un-muted
- 1: Signal muted

[1] LS center digital soft mute

- 0: Signal un-muted
- 1: Signal muted

[0] LS left/right digital soft mute

- 0: Signal un-muted
- 1: Signal muted

## 12.20 S/PDIF

### S/PDIF\_OUT\_CONFIG

### S/PDIF output configuration

7	6	5	4	3	2	1	0
0	0	0	0	0	S/PDIF_OUT_MUTE	S/PDIF_OUT_SELECT	
R/W							

**Address:** 0xF2

**Type:** R/W

**Reset:** 0x04

[7:3] Reserved.

[2] S/PDIF output mute:

- 0: S/PDIF output unmuted.
- 1: S/PDIF output muted.

[1:0] S/PDIF output channel selection:

- 00: Output SCART signal
- 01: Output LS L-R signal
- 10: Output C/SUB signal
- 11: Output Sur/HP signal



## 12.21 Headphone configuration

### HEADPHONE\_CONFIG Headphone configuration register

7	6	5	4	3	2	1	0
0	0	0	0	HP_FORCE	HP_LS_MUTE	HP_DET_ACTIVE	HP_DETECTED
R/W							

**Address:** 0xF3

**Type:** R/W

**Reset:** 0x02

[7:4] Reserved.

[3] 1: Force output of the HP signal (bypass surround)

[2] 0: When HP is detected and active, LS are not muted  
1: When HP is detected and active, LS are muted

[1] 0: HP detection is not active

1: HP detection is active, when HP detected, Surround signal is bypassed and HP signal is output on HP

[0] 1: When a signal is detected on HP\_DET pin (STATUS)

## 12.22 DAC control

### DAC\_CONTROL DAC control

7	6	5	4	3	2	1	0
0	0	S/PDIF_MUX	DAC_SCART_MUTE	DAC_SHP_MUTE	DAC_CSUB_MUTE	DAC_LSLR_MUTE	POWER_UP
R/W							

**Address:** 0xF4

**Type:** R/W

**Reset:** 0x1F

[7:6] Reserved.

[5] Redirect external or internal S/PDIF source to S/PDIF output :  
0: Internal S/PDIF  
1: External S/PDIF

[4] SCART left/right analog soft mute

0: Signal un-muted  
1: Signal muted

- [3] Surround/HP left/right analog soft mute
  - 0: Signal un-muted
  - 1: Signal muted
- [2] Center/Subwoofer analog soft mute
  - 0: Signal un-muted
  - 1: Signal muted
- [1] LS left/right analog soft mute
  - 0: Signal un-muted
  - 1: Signal muted
- [0] 0: DACs Power OFF
  - 1: Power ON

**DAC\_SW\_CHANNELS**

**DAC switch channels**

	7	6	5	4	3	2	1	0
	SUR_HP_SW		C_SUB_SW		LS_L_R_SW		SCART_SW	
R/W								

**Address:** 0xF5  
**Type:** R/W  
**Reset:** 0x00

- [7:6] HP/Surround DAC:
  - 00: Left/Right channels non inverted
  - 11: Left/Right channels inverted
- [5:4] Center/SubDAC:
  - 00: Left/Right channels non inverted
  - 11: Left/Right channels inverted
- [3:2] LS Left-Right DAC:
  - 00: Left/Right channels non inverted
  - 11: Left/Right channels inverted
- [1:0] SCART DAC:
  - 00: Left/Right channels non inverted
  - 11: Left/Right channels inverted

**SPDIF\_SW\_CHANNELS**

**SPDIF switch channels**

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	SPDIF_SW	
R/W								

**Address:** 0xF6  
**Type:** R/W  
**Reset:** 0x00

- [7:2] Reserved.

[1:0] SPDIF output:  
 00: Left/Right channels non inverted  
 11: Left/Right channels inverted

**SPDIF\_CHANNEL\_STATUS    Status of SPDIF channel**

7	6	5	4	3	2	1	0
CHANNEL_STATUS		EMPHASIS			COPYRIGHT	NON_AUDIO	PRO_CON
R/W							

**Address:**        0xF9  
**Type:**            R/W  
**Reset:**            0x00

[7:6] Channel status mode:  
 00: Mode zero  
 other values: reserved

[5:3] Emphasis: according to IEC60958 specification

[2] Copyright:  
 0: Asserted  
 1: Not asserted

[1] Non-audio:  
 0: Linear PCM  
 1: Non-audio signal

[0] Select professional or consumer modes:  
 0: Consumer  
 1: Professional

**12.23    AutoStandard coefficients settings**

**AUTOSTD\_COEFF\_CTRL    Autostandard coefficients control**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	AUTOSTD_COEFF_CTRL[1:0]	
R/W							

**Address:**        0xFB  
**Type:**            R/W  
**Reset:**            0x01

[7:2] Reserved.

[1:0] Control the Demod filter coeff table settings  
 00: No action  
 01: Init coefficients to ROM values  
 10: Update coefficients with I<sup>2</sup>C values (set to 0 by DSP to acknowledge)

**AUTOSTD\_COEFF\_INDEX\_MSB    Autostandard coefficients index MSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	AUTOSTD_COEFF_INDEX_MSB
R/W							

**Address:**        0xFC  
**Type:**            R/W  
**Reset:**            0x00

[7:1] Reserved.  
 [0] FIR coefficients table index (MSB)

**AUTOSTD\_COEFF\_INDEX\_LSB    Autostandard coefficients index LSB**

7	6	5	4	3	2	1	0
AUTOSTD_COEFF_INDEX_LSB[7:0]							
R/W							

**Address:**        0xFD  
**Type:**            R/W  
**Reset:**            0x00

[7:0] FIR coefficients table index (LSB)

**AUTOSTD\_COEFF\_VALUE    Autostandard coefficient value**

7	6	5	4	3	2	1	0
AUTOSTD_COEFF_VALUE[7:0]							
R/W							

**Address:**        0xFE  
**Type:**            R/W  
**Reset:**            0x00

[7:0] FIR coefficients table value to update

*Note: These four registers (AUTOSTD\_COEFF\_CTRL, AUTOSTD\_COEFF\_INDEX\_MSB, AUTOSTD\_COEFF\_INDEX\_LSB and AUTOSTD\_COEFF\_VALUE) can be used to change parameter settings for the following parts of channel 1 or channel 2:*

- Channel carrier DCO frequency (register CARFQxx)
- Channel filter coefficients (registers FIRxCx)
- PLL baseband AM/FM demodulators proportional and integral coefficients (registers ACOEFFx or BCOEFFx)
- Demodulator mode selection (register DEMOD\_CTRL)
- IF AGC control (AGC\_CTRL)
- Channel 2 symbol tracking loop parameters (register SCOEFF)
- Zweiton control (register ZWT\_CTRL)

*While keeping the AUTOSTANDARD function always active.*

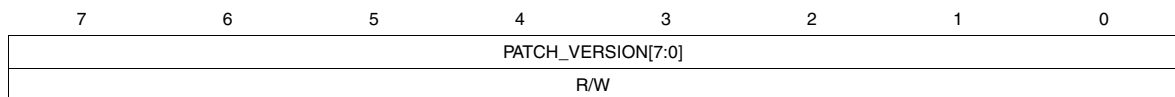
*New values for all parameters mentioned above are kept instead of the values automatically sent by the AUTOSTANDARD function.*

One application is for example to implement OVERMODULATION recovery mode for any sound standard supported by the device (B/G, I, M/N, DK1, DK2, or DK3).

See Technical Note for instructions on how to update the coefficient table settings.

**PATCH\_VERSION**

**Patch version**



**Address:** 0xFF  
**Type:** R/W  
**Reset:** 0x00

[7:0] Indicate the patch version which has been loaded in the device (can be used to check if the patch has been correctly loaded)

## 13 Pin descriptions

- AP = Analog power
- DP = Digital power
- I = Input
- O = Output
- OD = Open-drain
- B = Bidirectional
- A = Analog

**Table 31. TQFP80 pin description**

Pin no.	STV82x7 pin name	Type (STV82x7)	Function for STV82x7 (function for STV82x6 in <i>italics</i> )	STV82x6 Pin Name
1	SC1_OUT_L	A	SCART1 audio output left	AO1L
2	SC1_OUT_R	A	SCART1 audio output right	AO1R
3	VCC_H	AP	8 V power for audio I/O & ESD	Not connected
4	GND_H	AP	High current ground for audio outputs	CgGround
5	SC3_OUT_L	A	SCART3 audio output left	Not connected
6	SC3_OUT_R	A	SCART3 audio output right	Not connected
7	VCC33_SC	AP	3.3 V power for audio buffers & DAC / ADC	VDDC
8	GND33_SC	AP	Ground for audio buffers & DAC / ADC	GNDC
9	SC1_IN_L	A	SCART1 audio input left	AI1L
10	SC1_IN_R	A	SCART1 audio input right	AI1R
11	VREFA	A	Audio bias voltage decoupling 1.55 V ( <i>Switched <math>V_{REF}</math> decoupling pin for audio converters (VMCP)</i> )	VMC1
12	GND_SA	AP	Ground for DACs	Connected to ground
13	VBG	A	Bandgap voltage reference decoupling 1.2 V ( <i><math>V_{REF}</math> decoupling pin for audio converters (VMC)</i> )	VMC2
14	SC2_IN_L	A	SCART2 audio input left	AI2L
15	SC2_IN_R	A	SCART2 audio input right	AI2R
16	VCC33_LS	AP	3.3 V power for audio DACs ( <i>3.3 V power supply for audio buffers and SCART</i> )	VDDA
17	GND33_LS	AP	Ground for audio DACs ( <i>Ground for audio buffers and SCART</i> )	GNDAH
18	SC2_OUT_L	A	SCART2 audio output left	AO2L
19	SC2_OUT_R	A	SCART2 audio output right	AO2R
20	VCC_NISO	AP	Polarization of the NISO (connected to <i>audio buffers</i> )	VDDH
21	VSS33_CONV	AP	Ground for DAC 1.8 to 3.3 V converters	Connected to ground

Table 31. TQFP80 pin description (continued)

Pin no.	STV82x7 pin name	Type (STV82x7)	Function for STV82x7 (function for STV82x6 in italics)	STV82x6 Pin Name
22	VDD33_CONV	AP	3.3 V power for DAC 1.8 to 3.3 V converters ( <i>Voltage rference for audio buffers</i> )	VREFA
23	SC3_IN_L	A	SCART3 audio input left	AI3L
24	SC3_IN_R	A	SCART3 audio input right	AI3R
25	SCL_FLT	A	SCART filtering left	Not connected
26	SCR_FLT	A	SCART filtering right ( <i>Bandgap voltage source decoupling</i> )	BGAP
27	LS_C	A	Center output	Not connected
28	LS_L	A	Left loudspeaker output	LSL
29	LS_R	A	Right loudspeaker output	LSR
30	LS_SUB	A	Subwoofer output	SW
31	HP_LSS_L	A	Left headphone output or left surround output	HPL
32	HP_LSS_R	A	Right headphone output or right surround output	HPR
33	VSS18_CONV	DP	Ground for digital part of the DAC/ADC ( <i>Substrate analog/digital shield</i> )	GNDSA
34	VDD18_CONV	DP	1.8 V power for digital part of the DAC/ADC	Not connected
35	HP_DET	I	Headphone detection	HPD
36	ADR_SEL	I	Hardware address selection for I <sup>2</sup> C Bus	ADR
37	VSS18	DP	Ground for ddigital part	Connected to ground
38	VDD18	DP	1.8 V power for digital part	Not connected
39	SCL	OD	I <sup>2</sup> C clock input	SCL
40	SDA	OD	I <sup>2</sup> C data I/O	SDA
41	VSS18	DP	Ground for digital part	Connected to Ground
42	VDD18	DP	1.8 V power for digital part ( <i>5 V power regulator control</i> )	REG
43	RST	I	Main reset input	RESET
44	S/PDIF_IN	I	Serial audio data input ( <i>System Clock output</i> )	SYSCK
45	S/PDIF_OUT	O	Serial audio data output ( <i>I<sup>2</sup>S master clock output</i> )	MCK
46	VDD33_IO1	DP	3.3 V power for digital part	VDD1
47	VSS33_IO1	DP	Ground for digital part	GND1
48	CK_TST_CTRL	D	To be grounded	Not connected
49	VSS18	DP	Ground for digital part	GNDSP
50	VDD18	DP	1.8 V power for digital part	Not connected
51	CLK_SEL	I	Clock input format selection	Not connected

Table 31. TQFP80 pin description (continued)

Pin no.	STV82x7 pin name	Type (STV82x7)	Function for STV82x7 (function for STV82x6 in italics)	STV82x6 Pin Name
52	XTALIN_CLKXTP	I	Crystal oscillator input or differential input positive <i>(Crystal oscillator input)</i>	XTI
53	XTALOUT_CLKXTM	O	Crystal oscillator output or differential input negative <i>(Crystal oscillator output)</i>	XTO
54	VCC18_CLK1	AP	1.8 V power for clock PLL analog & crystal oscillator 1/2 <i>(3.3 V Power supply for Analog PLL Clock)</i>	VDDP
55	GND18_CLK1	AP	Ground for clock PLL analog & crystal oscillator 1/2	GNDP
56	GND18_CLK2	DP	Ground for clock PLL digital 1/2	GND2
57	VCC18_CLK2	DP	1.8 V power for clock PLL digital 1/2 <i>(3.3 V power supply for digital core, DSPs &amp; IO cells)</i>	VDD2
58	VSS33_IO2	DP	Ground for digital IO pins 60 to 69	Connected to ground
59	VDD33_IO2	DP	3.3 V power for digital IO pins 60 to 69	Not connected
60	I2S_PCM_CLK	I/O	I <sup>2</sup> S slave clock input/output channel 1, 2 & 3	Not connected
61	I2S_SCLK	I/O	I <sup>2</sup> S clock input/output channel 1, 2 & 3 (I <sup>2</sup> S bus data output)	SDO
62	I2S_LR_CLK	I/O	I <sup>2</sup> S word select input/output channel 1,2 & 3 <i>(Stereo detection output / I<sup>2</sup>S bus data input)</i>	ST/SDI
63	I2S_DATA0	I/O	I <sup>2</sup> S data input/output stereo channel 1 <i>(I<sup>2</sup>S bus word select output)</i>	WS
64	I2S_DATA1	I	I <sup>2</sup> S data input stereo channel 2 <i>(I<sup>2</sup>S bus clock output)</i>	SCK
65	I2S_DATA2	I	I <sup>2</sup> S data input stereo channel 3 <i>(Bus expander output 1)</i>	BUS1
66	VDD18	DP	1.8 V power for digital core & I/O cells pin	Not connected
67	VSS18	DP	Ground for digital core & I/O cells pin	Connected to Ground
68	BUS_EXP	O	Bus Expander Function <i>(Bus Expander Output 2)</i>	BUS0
69	IRQ	O	InterruptRequest to microprocessor	IRQ
70	GND_PSUB	AP	Ground substrate connection	Connected to Ground
71	VDD18_ADC	DP	VDD 1.8 V for ADC (digital part)	Not connected
72	VSS18_ADC	DP	Ground to complement 1.8 V VDD for ADC	Connected to ground
73	SIF_P	A	Sound IF input (positive)	SIF
74	SIF_N	A	Sound IF input (negative) (ADC V <sub>TOP</sub> decoupling pin)	VTOP
75	GNDPW_IF	AP	Polarization for the IF block <i>(Voltage reference for AGC decoupling pin)</i>	VREFIF



Table 31. TQFP80 pin description (continued)

Pin no.	STV82x7 pin name	Type (STV82x7)	Function for STV82x7 (function for STV82x6 in italics)	STV82x6 Pin Name
76	VCC18_IF	AP	1.8 V power for IF AGC & ADC	VDDIF
77	GND18_IF	AP	Ground for IF AGC & ADC	GNDIF
78	MONO_IN	A	Mono input (for AM mono)	MONOIN
79	SC4_IN_L	A	SCART4 audio input left	Not connected
80	SC4_IN_R	A	SCART4 audio Input right	Not connected

# 14 Application diagrams

Figure 29. STV82x7 application diagram

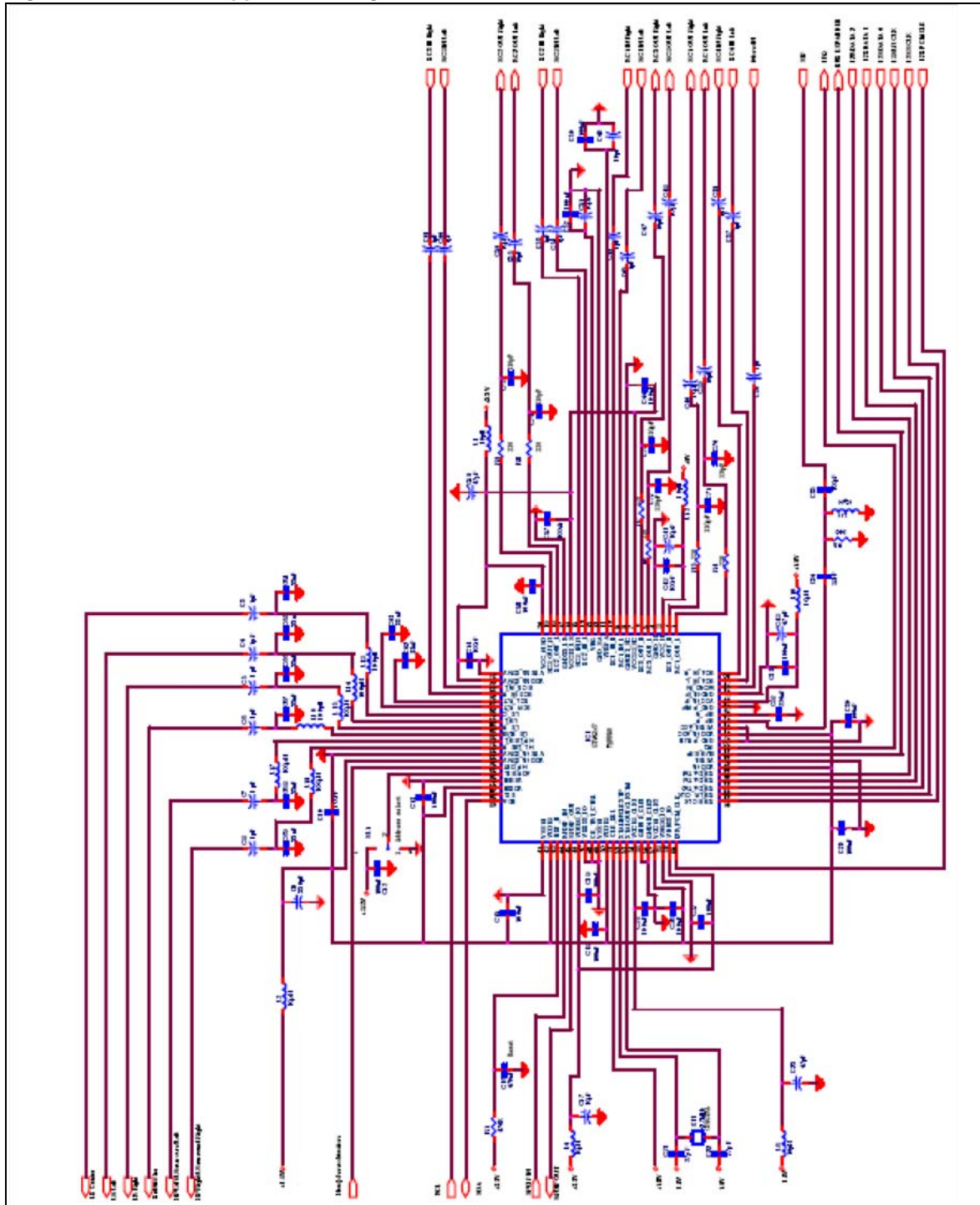


Figure 30. STV82x6/STV82x7 compatible application electrical diagram

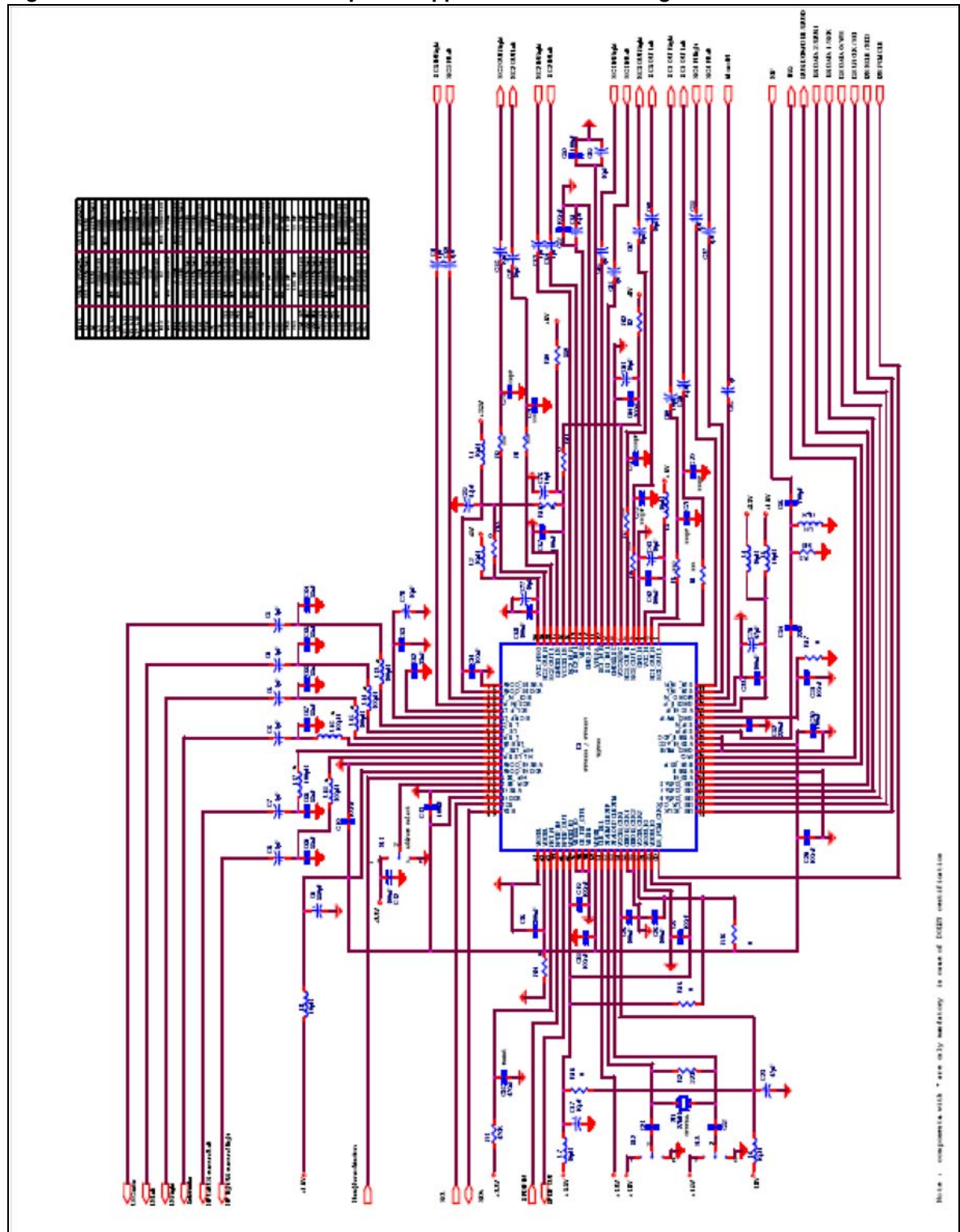
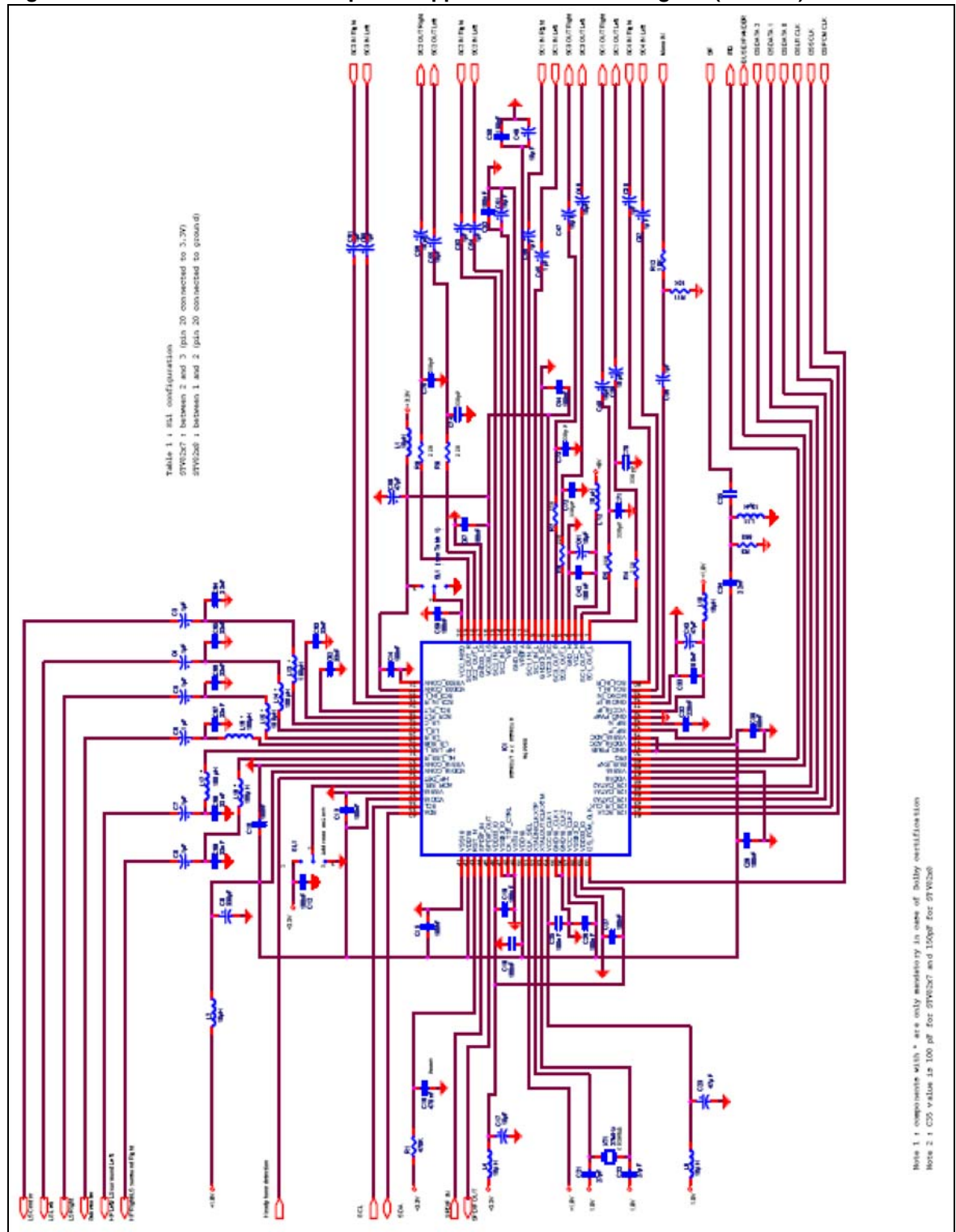


Figure 31. STV82x7/STV82x8 compatible application electrical diagram (TQFP80)



## 15 System clock

The system clock integrates 2 independent frequency synthesizers.

The first frequency synthesizer can be used in one of two modes:

- In mode 1, it is used by the demodulator, and the frequency is 49.152 MHz.
- In mode 2, it is used by the I<sup>2</sup>S input and is synchronous with the input frequency ( $f_S = 32, 44.1$  or  $48$  kHz) and the frequency is 49.152 MHz (for  $f_S = 32$  or  $48$  kHz) or 45.1584 MHz (for  $f_S = 44.1$  kHz).

The second frequency synthesizer is used by the DSP core and can be adjusted between 100 and 150 MHz depending on the application (around 106 MHz at reset value).

In I<sup>2</sup>S output mode, clocks are generated by synthesizer 1.

The default values are designed for a **standard 27 MHz reference frequency** provided by a stable single crystal or an external differential clock signal (for example, from the STV35x0) depending on the CLK\_SEL pin configuration (CLK\_SEL = 1 means a single crystal, 0 means an external differential clock). The 27 MHz value is the recommended frequency for minimizing potential RF interference in the application. The sinusoidal clock frequency, and any harmonic products, remain outside the TV picture and sound IFs (PIF/SIF) and Band-I RF.

*Note: A change in the reference frequency is compatible with other default I<sup>2</sup>C programming values, including those of the built-in Automatic Standard Recognition System.*

# 16 Input/Output groups

Pin numbers apply to SDIP package only

Figure 32. SIF\_P

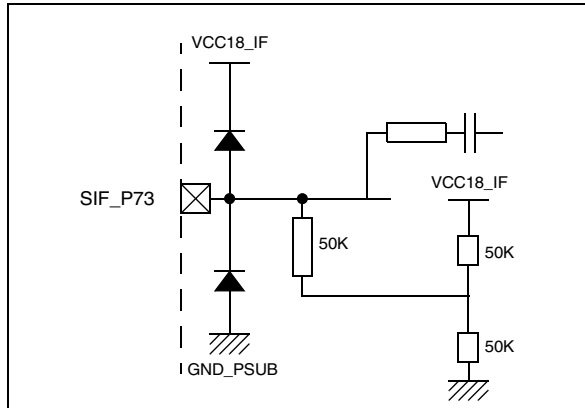


Figure 33. SC\_OUT

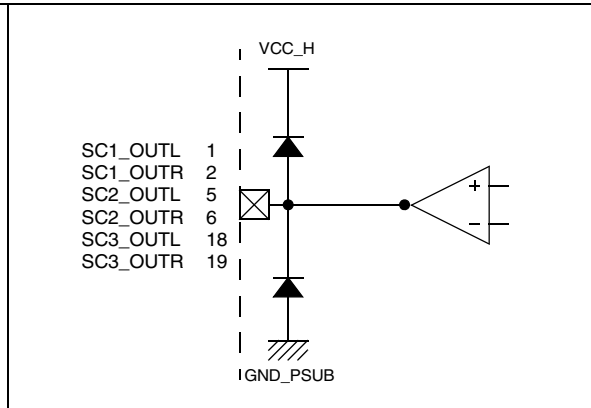


Figure 34. VCC33\_LS

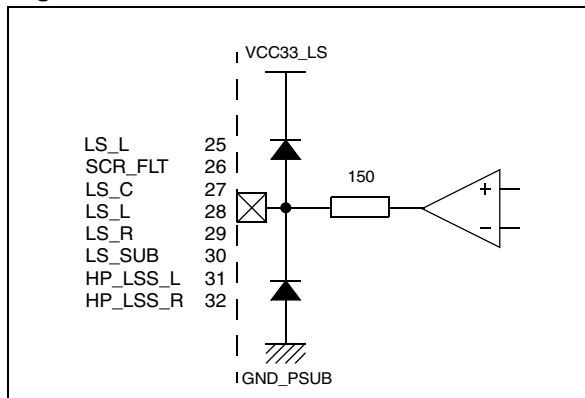


Figure 35. MONO\_IN

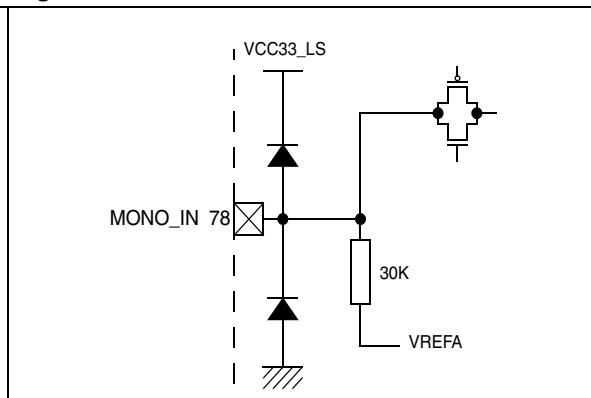


Figure 36. VCC18\_IF

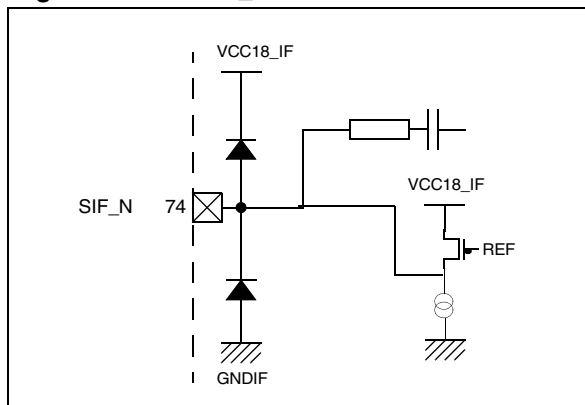


Figure 37. SC\_IN

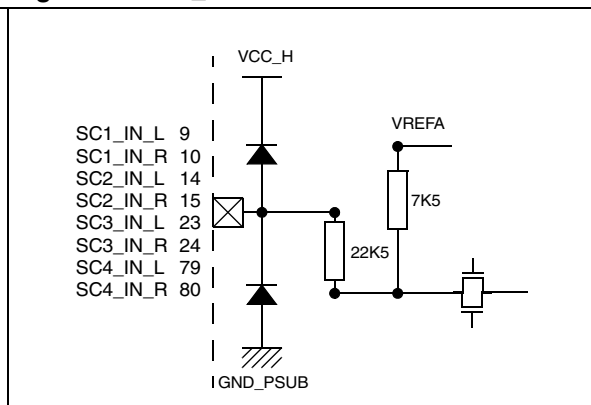


Figure 38. VREFA

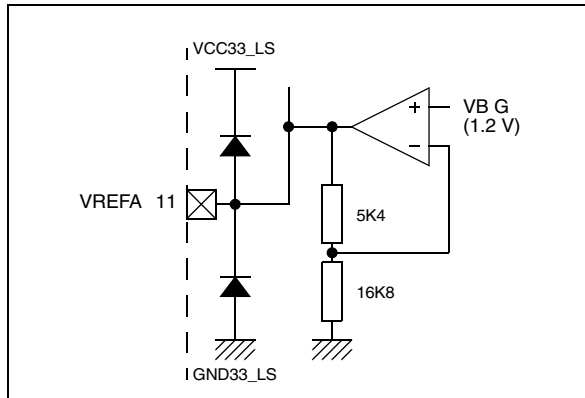


Figure 39. VBG

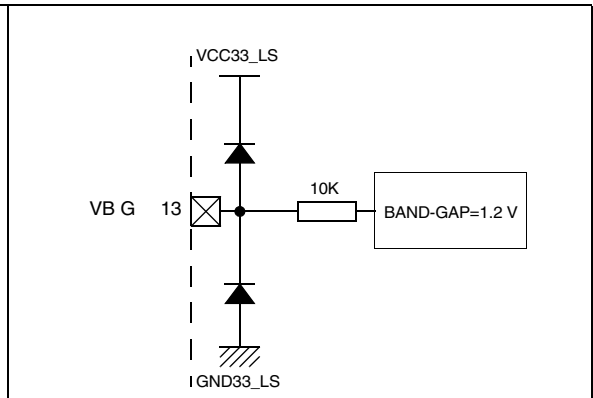


Figure 40. VDD33\_I01

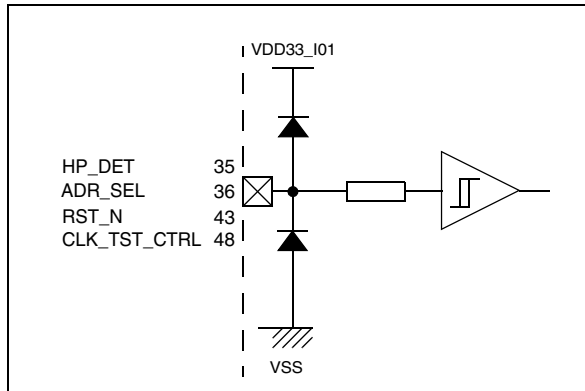


Figure 41. S/PDIF\_OUT

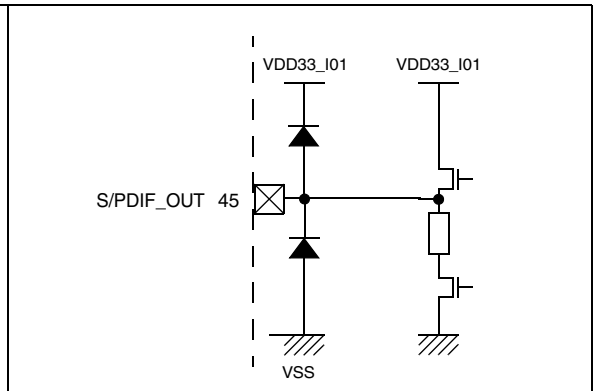


Figure 42. BUS\_EXDIRQ

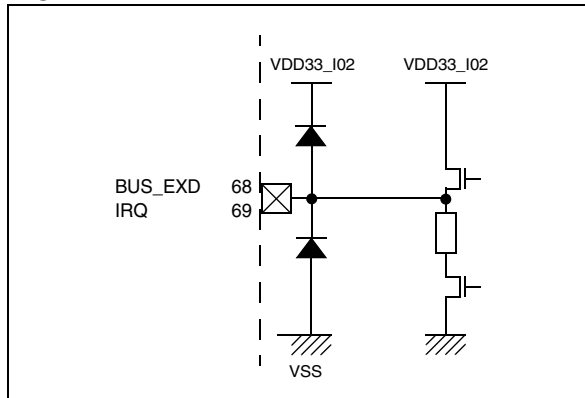


Figure 43. S/PDIF\_IN

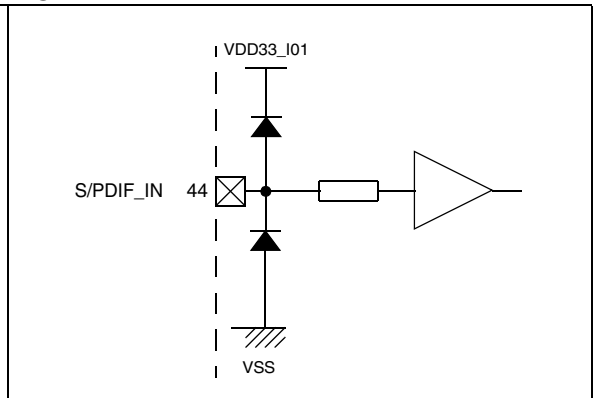


Figure 44. I<sup>2</sup>S

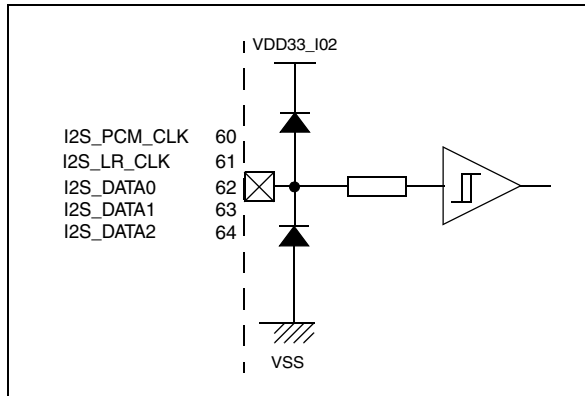


Figure 45. CLK\_SEL

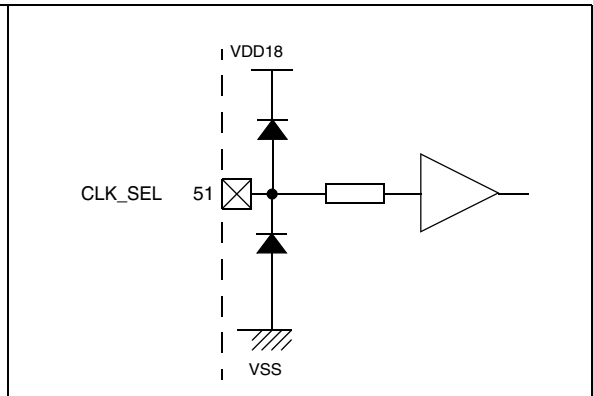


Figure 46. SCL

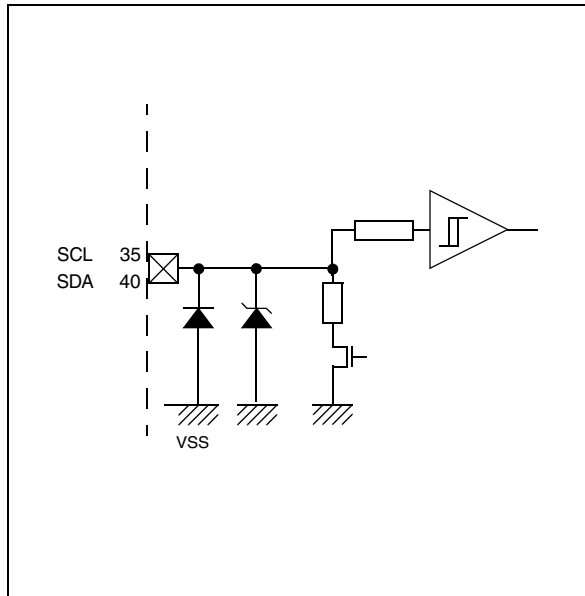


Figure 47. VC18\_CLK1

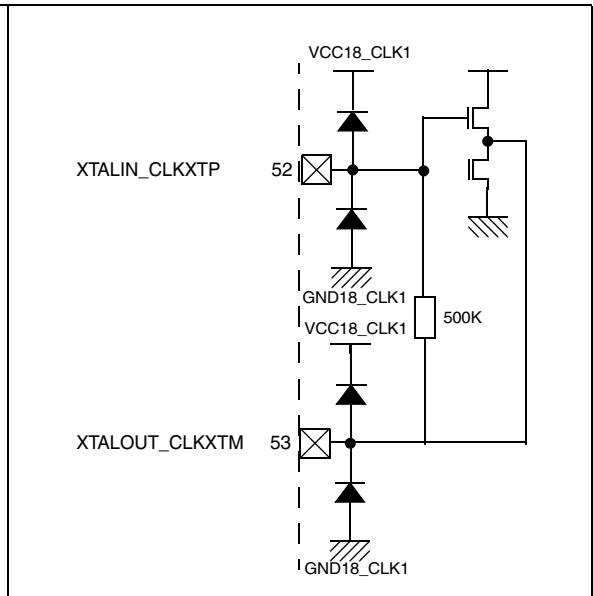
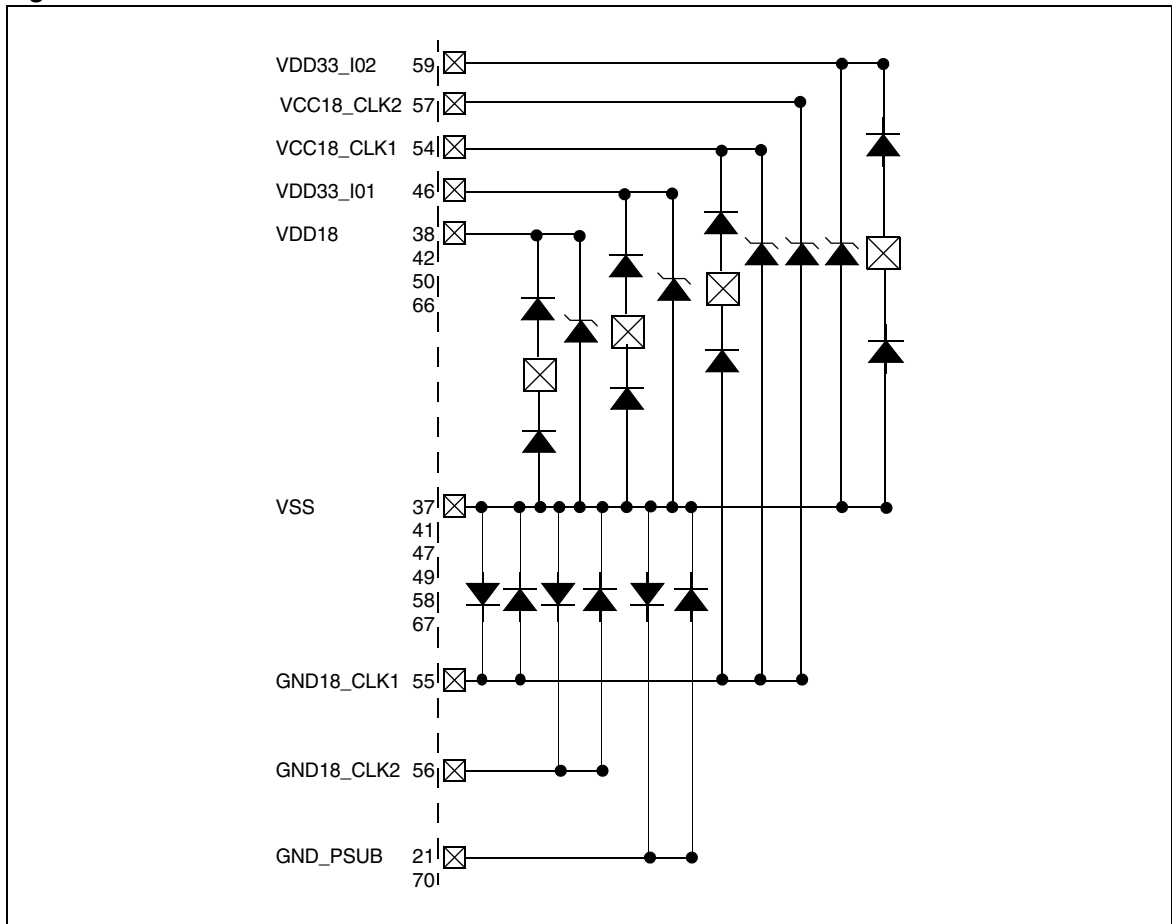




Figure 48. VSS



## 17 Electrical characteristics

Test conditions:  $T_{\text{OPER}} = 25^{\circ}\text{C}$ ,  $V_{\text{CC}_H} = 8\text{V}$ ,  $V_{\text{XX}_{18}} = 1.8\text{V}$ ,  $V_{\text{XX}_{33}} = 3.3\text{V}$ , oscillator at 27 MHz, default register values for synthesizer, otherwise specified.

### 17.1 Absolute maximum ratings

**Table 32. Absolute maximum ratings**

Symbol	Parameter	Value	Units
$V_{\text{XX}_{18}}$	Analog and digital 1.8 V supply voltage ( $V_{\text{CC18\_CLK1}}$ , $V_{\text{CC18\_CLK2}}$ , $V_{\text{CC18\_IF}}$ , $V_{\text{DD18}}$ , $V_{\text{DD18\_CONV}}$ , $V_{\text{DD18\_ADC}}$ )	2.5	V
$V_{\text{XX}_{33}}$	Analog and digital 3.3 V supply voltage ( $V_{\text{CC33\_SC}}$ , $V_{\text{CC33\_LS}}$ , $V_{\text{DD33\_IO1}}$ , $V_{\text{DD33\_IO2}}$ , $V_{\text{DD33\_CONV}}$ , $V_{\text{CC\_NISO}}$ )	4.0	V
$HV_{\text{CC}}$	Analog supply high voltage ( $V_{\text{CC}_H}$ )	8.8	V
$V_{\text{ESD}}$	Capacitor 100 pF discharged via 1.5 k $\Omega$ serial resistor (human body model)	4	kV
$T_{\text{OPER}}$	Operating ambient temperature	0, +70	$^{\circ}\text{C}$
$T_{\text{STG}}$	Storage temperature	-55 to +150	$^{\circ}\text{C}$

### 17.2 Thermal data

**Table 33. Thermal data**

Symbol	Parameter	Value	Units
$R_{\text{thJA}}$	Junction-to-ambient thermal resistance	42	$^{\circ}\text{C/W}$

### 17.3 Power supply data

**Table 34. Power supply data**

Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{\text{XX}_{18}}$	Analog and digital 1.8 V supply voltage ( $V_{\text{CC18\_CLK1}}$ , $V_{\text{CC18\_CLK2}}$ , $V_{\text{CC18\_IF}}$ , $V_{\text{DD18}}$ , $V_{\text{DD18\_CONV}}$ , $V_{\text{DD18\_ADC}}$ )	1.70	1.80	1.90	V
$V_{\text{XX}_{33}}$	Analog and digital 3.3 V supply voltage ( $V_{\text{CC33\_SC}}$ , $V_{\text{CC33\_LS}}$ , $V_{\text{DD33\_IO1}}$ , $V_{\text{DD33\_IO2}}$ , $V_{\text{DD33\_CONV}}$ , $V_{\text{CC\_NISO}}$ )	3.13	3.30	3.47	V
$HV_{\text{CC}}$	Analog supply high voltage ( $V_{\text{CC}_H}$ )	7.6	8.0	8.4	V
$I_{\text{VDD18}}$	Current consumption for digital 1.8 V supply ( $V_{\text{CC18\_CLK2}}$ , $V_{\text{DD18}}$ , $V_{\text{DD18\_CONV}}$ , $V_{\text{DD18\_ADC}}$ )		230	280	mA

**Table 34. Power supply data (continued)**

Symbol	Parameter	Min.	Typ.	Max.	Units
I <sub>VDD33</sub>	Current consumption for digital 3.3 V supply (V <sub>DD33_IO1</sub> , V <sub>DD33_IO2</sub> )		10	12	mA
I <sub>VCC18</sub>	Current consumption for analog 1.8 V supply (V <sub>CC18_CLK1</sub> , V <sub>CC18_IF</sub> )		50	60	mA
I <sub>VCC33</sub>	Current consumption for analog 3.3 V supply (V <sub>CC33_SC</sub> , V <sub>CC33_LS</sub> , V <sub>DD33_CONV</sub> , V <sub>CC_NISO</sub> )		65	78	mA
I <sub>VCC_H</sub>	Current consumption for analog supply high voltage (8 V)		4	7	mA
P <sub>DTOT</sub>	Total power dissipation		780	965	mW

## 17.4 Crystal oscillator

**Table 35. Crystal oscillator**

Symbol	Parameter	Min.	Typ.	Max.	Units
f <sub>P</sub>	Crystal series resonance frequency (at C21 = C22 = 27 pF load capacitor)		27		MHz
DF/F <sub>P</sub>	Frequency tolerance at 25 °C	-30		+30	ppm
DF/F <sub>T</sub>	Frequency stability versus temperature within a range from 0 to 70 °C	-30		+30	ppm
C1	Motional capacitor			15	fF
R <sub>S</sub>	Serial resistance			30	Ω
C <sub>S</sub>	Shunt capacitance			7	pF

## 17.5 Analog sound IF signal

**Table 36. Analog sound IF signal**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.
BAND <sub>SIF</sub>	SIF frequency flatness	AGC_ERR at 0, frequency range from 4 to 7 MHz		0.6	3
R <sub>INSIF</sub>	SIF input resistance		60	72	85
DC <sub>INSIF</sub>	SIF input DC level			0.9	
C <sub>INSIF</sub>	SIF input capacitance			3	
FM carrier					
VSIF <sub>FM</sub>	SIF input sensitivity	SNR 40dB RMS unweighted, 20 Hz-15 kHz, Standard B/G 27 kHz FM deviation, 1 kHz	350		

Table 36. Analog sound IF signal (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	
DEV <sub>FM</sub>	FM maximum deviation	FM50k (standard)	Signal lost, DK mode, FM prescale at 0	±15	±50	±115
		FM200k		±200	±320	
		FM350k		±350	±560	
		FM500k		±500	±700	
DFSIF <sub>FM</sub>	SIF carrier accuracy for FM	Standard (FM50k)		±1	±5	
		Shifted standard (FM50k with DCO compensation)			±120	
R <sub>FM/QPSK</sub>	Carrier ratio FM/QPSK for NICAM system	NICAM mute, FAR_MODE is active, standard BG, 100 mV <sub>PP</sub> level for FM carrier			40	
AM carrier						
VSIF <sub>AM</sub>	SIF input sensitivity	Unmodulated, -3 dB at output amplitude AGC_ERR at 21d standard L, 54% AM depth, 1 kHz	19			
VMAX_SIF <sub>AM</sub>	SIF maximum input level	Unmodulated, THD at 1%, 54% AM depth, AGC_ERR at 0			1.3	
DEV <sub>AM</sub>	Modulation depth for AM	THD at 1%	0		100	
DFSIF <sub>AM</sub>	SIF carrier accuracy for AM			±1	±5	
R <sub>AM/QPSK</sub>	AM/QPSK carrier ratio for NICAM system	NICAM mute, 100 mV <sub>PP</sub> AM carrier			36	
AGC						
AGC <sub>step</sub>	IF AGC step		1.4	1.5	1.6	
AGC <sub>dyn</sub>	Relative maximum gain to step 0	Valid from step 21 to step 31	29	30	31	

## 17.6 SIF to I<sup>2</sup>S output path characteristics

Test conditions: SIF amplitude = 10 mVpp, otherwise specified, I<sup>2</sup>S output

**Table 37. SIF to I<sup>2</sup>S output path characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
FM demodulation						
BAND <sub>FM</sub>	Frequency response	20 Hz - 15 kHz			±0.7	dB
SNR <sub>FM</sub>	Signal to noise	RMS unweighted, 20 Hz-15k Hz, Standard B/G 27 kHz FM Deviation, 1 kHz	66			dB
THD <sub>FM</sub>	Total harmonic distortion				0.05	%
SEP <sub>FM</sub>	Stereo channel separation	Standard B/G stereo A2, 27 kHz FM deviation, 1 kHz	48			dB
NICAM demodulation						
BAND <sub>NIC</sub>	Frequency response	20 Hz - 15 kHz			±0.2	dB
SNR <sub>NIC</sub>	Signal to noise	200 Hz - 60 dBFS, trap filter 200 Hz RMS unweighted, 20 Hz-15 kHz, standard B/G mono NICAM, 1 kHz	74			dB
THD <sub>NIC</sub>	Total Harmonic Distortion				0.04	%
AM demodulation						
BAND <sub>AM</sub>	Frequency response	20 Hz - 15 kHz			±0.5	dB
SNR <sub>AM</sub>	Signal to noise	RMS unweighted 20 Hz-15 kHz, standard L, 54% AM depth, 1 kHz AGC: 13d	60			dB
THD <sub>AM</sub>	Total harmonic distortion				0.4	%

## 17.7 SCART to SCART analog path characteristics

Test conditions:  $R_{load\_MAX} = 10k\Omega$ ,  $C_{load\_MAX} = 330pF$ , MONO\_IN voltage =  $0.5 V_{RMS}$

**Table 38. SCART to SCART analog path characteristics**

Symbol	Parameter		Test conditions	Min.	Typ.	Max.	Units
<b>Analog-to-analog STEREO and MONO</b>							
$R_{INSCART}$	SCART input resistance			29	34	39	$k\Omega$
$R_{OUTSCART}$	Output resistance for SCARTs				40	75	W
$VDC_{INSCART}$	SCART input DC level			1.45	1.57	1.65	V
$VDC_{OUTSCART}$	SCART output DC level			3.4	3.64	3.8	V
$CLIP_{SCART}$	Clipping SCART	Clipping input level from SCART input	At 1 kHz 1% THD	2.0			$V_{RMS}$
		Clipping input level from MONO_IN input		0.5			$V_{RMS}$
$THD_{SCART}$	THD SCART	THD from SCART input	$1 V_{RMS}$ , at 1 kHz		0.02	0.05	%
		THD from MONO_IN input	$0.25 V_{RMS}$ , at 1 kHz		0.02	0.05	%
$SNR_{SCART}$	Signal to noise ratio	SCART input	$1 V_{RMS}$ , 20 Hz to 20 kHz Bandwidth, RMS unweighted	82	90		dB
		MONO_IN input	$0.25 V_{RMS}$ , 20 Hz to 20 kHz Bandwidth, RMS unweighted	82	90		dB
$BAND_{SCART}$	Frequency flatness	SCART input	20 Hz to 20 kHz	-0.5	0	0.5	dB
		MONO_IN input	20 Hz to 20 kHz	11.5	12	12.5	dB
$XTALK_{L/R}$	Left/Right crosstalk		$1 V_{RMS}$ @ 1 kHz on ref signal, the other one grounded	80	90		dB
$XTALK_{IN}$	Audio crosstalk from input channel $n$ to input channel $m$		$1 V_{RMS}$ @ 1 kHz on ref signal, all other inputs grounded	80	90		dB
$XTALK_{OUT}$	Audio crosstalk from output channel $n$ to output channel $m$		$1 V_{RMS}$ @ 1 kHz on reference output, signal on a single input, all other inputs grounded	80	90		dB

## 17.8 SCART and MONO IN to I<sup>2</sup>S path characteristics

Test conditions: sampling frequency = 32 kHz, Maximum MONO\_IN voltage = 0.5 V<sub>RMS</sub>.

**Table 39. SCART to MONO IN to I<sup>2</sup>S path characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
THD <sub>ADC</sub>	THD ADC	THD from SCART input $V_{IN} = 2 V_{RMS}$ at 1 kHz		0.006	0.05	%
		THD from MONO_IN input $V_{IN} = 0.5 V_{RMS}$ at 1 kHz		0.006	0.05	%
SNR <sub>ADC</sub>	Signal to noise ratio	20 to 15 kHz bandwidth, RMS unweighted $V_{IN} = 200 mV_{RMS}$ SCART input	62			dB
BAND <sub>ADC</sub>	Frequency flatness	20 Hz to 15 kHz			±0.5	dB
XTALK <sub>ADC</sub>	Left right crosstalk	at 1 kHz, $V_{IN} = 1 V_{RMS}$	95			dB

## 17.9 I<sup>2</sup>S to LS/HP/SUB/C path characteristics

Test conditions: sampling frequency = 32 kHz, L<sub>LOAD</sub> = 100 μH, C<sub>LOAD</sub> = 33 nF, R<sub>LOAD</sub> = 30 KΩ

**Table 40. I<sup>2</sup>S to LS/HP/SUB/C path characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
R <sub>OUTDAC</sub>	Output resistance for main outputs	LS_L, LS_R, LS_SUB, LS_C, HP_LSS_R and HP_LSS_L pins		90	140	W
V <sub>DCOUTDAC</sub>	MAIN output DC Level		1.4	1.55	1.8	V
THD <sub>DAC</sub>	Total harmonic distortion	90% Full-scale Range at 1 kHz			0.06	%
SNR <sub>DAC</sub>	Signal to noise ratio	20 to 15 kHz Bandwidth, RMS unweighted, at -20 dB full range	75			dB
V <sub>OUTAMPDAC</sub>	MAIN output amplitude	100% full-scale range at 1 kHz	800	900	1050	mV <sub>RMS</sub>
XTALK <sub>DAC</sub>	Left right crosstalk	at 1 kHz, -20 dBFS	87			dB

## 17.10 I<sup>2</sup>S to SCART path characteristics

Test conditions: sampling frequency = 32 kHz, C<sub>LOAD</sub> = 33 nF on DAC SCART pins, DAC SCART prescale at -5.5 dB

**Table 41. I<sup>2</sup>S to SCART path characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
THD <sub>DACSCART</sub>	Total harmonic distortion	90% full-scale range at 1 kHz		0.08	0.12	%
SNR <sub>DACSCART</sub>	Signal to noise ratio	20 Hz to 15 kHz bandwidth unweighted, -20 dB full range	73			dB
V <sub>ODACSCART</sub>	MAIN output amplitude	100% full-scale range at 1 kHz	1.75	2	2.25	V <sub>RMS</sub>
XTALK <sub>DACSCART</sub>	Left right crosstalk	at 1 kHz, -20 dBFS	80			dB

## 17.11 MUTE characteristics

**Table 42. MUTE characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
MUTE <sub>DAC</sub>	DAC mute analog	I <sup>2</sup> S to DAC at 1 kHz	90			dB
MUTE <sub>SCART</sub>	SCART mute	2 V <sub>RMS</sub> @ 1 kHz on ref signal, all other inputs grounded	81			dB

## 17.12 Digital I/Os characteristics

**Table 43. Digital I/O characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
V <sub>IL</sub>	Low level input voltage	Except SDA, SCL and CLK_SEL, 3.3 V power supply			0.5	V
V <sub>IH</sub>	High level input voltage	Except SDA, SCL and CLK_SEL, 3.3 V power supply	2.0			V
I <sub>IN</sub>	Input current				1	μA
V <sub>ILCLK_SEL</sub>	CLK_SEL low level input voltage	1.8 V power supply			0.3	V
V <sub>IHCLK_SEL</sub>	CLK_SEL highlevel input voltage	1.8 V power supply	1.2			V
V <sub>OL</sub>	Low level output voltage	S/PDIF_OUT, IRQ, BUS_EXP			0.3	V
V <sub>OH</sub>	High level output voltage	S/PDIF_OUT, IRQ, BUS_EXP	3.0			V



## 17.13 I<sup>2</sup>C bus characteristics

Table 44. I<sup>2</sup>C bus characteristics

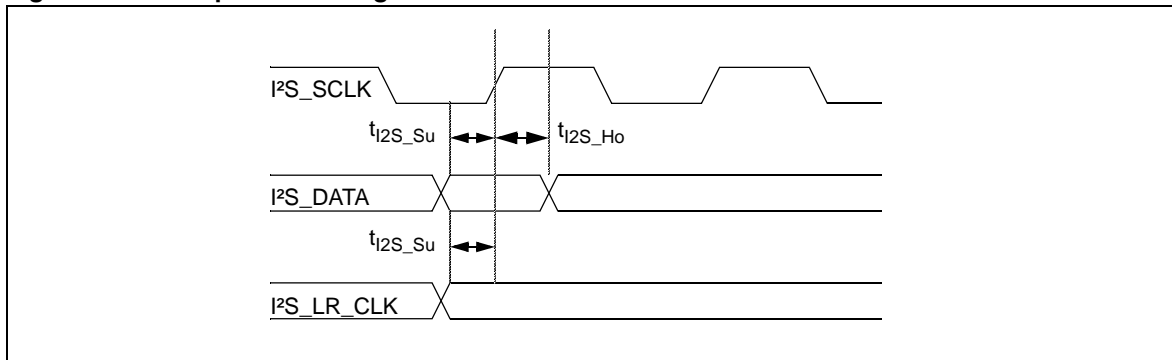
Symbol	Parameter	Test conditions	Min.	Typ	Max.	Units
<b>SCL</b>						
V <sub>IL</sub>	Low level input voltage		-0.3		1.5	V
V <sub>IH</sub>	High level input voltage		2.3		5.5	V
I <sub>IL</sub>	Input leakage current	V <sub>IN</sub> = 0 to 5.0 V	-10		10	μA
f <sub>SCL</sub>	Clock frequency				400	kHz
t <sub>R</sub>	Input rise time	1 V to 2 V			300	ns
t <sub>F</sub>	Input fall time	2 V to 1 V			300	ns
C <sub>I</sub>	Input capacitance				10	pF
<b>SDA</b>						
V <sub>IL</sub>	Low level input voltage		-0.3		1.5	V
V <sub>IH</sub>	High level input voltage		2.3		5.5	V
I <sub>IL</sub>	Input leakage current	V <sub>IN</sub> = 0 to 5.0 V	-10		10	μA
t <sub>R</sub>	Input rise time	1 V to 2 V			300	ns
t <sub>F</sub>	Input fall time	2 V to 1 V			300	ns
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 3 mA			0.4	V
t <sub>F</sub>	Output fall time	2 V to 1 V			250	ns
C <sub>L</sub>	Load capacitance				400	pF
C <sub>I</sub>	Input capacitance				10	pF
<b>I<sup>2</sup>C Timing</b>						
t <sub>LOW</sub>	Clock low period		1.3			μs
t <sub>HIGH</sub>	Clock high period		0.6			μs
t <sub>SU,DAT</sub>	Data set-up time		100			ns
t <sub>HD,DAT</sub>	Data hold time		0		900	ns
t <sub>SU,STO</sub>	Set-up time from clock high to stop		0.6			μs
t <sub>BUF</sub>	Start set-up time following a stop		1.3			μs
t <sub>HD,STA</sub>	Start hold time		0.6			μs
t <sub>SU,STA</sub>	Start set-up time following clock low to high transition		0.6			μs

## 17.14 I<sup>2</sup>S bus interface characteristics

See [Table 5](#) for I<sup>2</sup>S timing.

**Table 45. I<sup>2</sup>S bus interface characteristics**

Symbol	Parameter	Test conditions	Min.	Typ	Max.	Units
<b>I<sup>2</sup>S Input</b>						
V <sub>I2S_IL</sub>	Input I <sup>2</sup> S low level voltage				0.8	V
V <sub>I2S_IH</sub>	Input I <sup>2</sup> S high level voltage		2			V
Z <sub>I2S</sub>	Input I <sup>2</sup> S impedance				5	pF
I <sub>I2S_Leak</sub>	I <sup>2</sup> S leakage current		-1		1	μA
t <sub>I2S_Su</sub>	I <sup>2</sup> S input setup time before rising edge of clock	See <a href="#">Figure 49</a>	30			ns
t <sub>I2S_Ho</sub>	I <sup>2</sup> S input hold time after rising edge of clock	See <a href="#">Figure 49</a>	100			ns
f <sub>I2S_LR0</sub>	I <sup>2</sup> S left right strobe Input frequency (I <sup>2</sup> S_DATA0 only)	Deviation = ±250 ppm	8		48	kHz
f <sub>I2S_SCL0</sub>	I <sup>2</sup> S serial clock input frequency (I <sup>2</sup> S_DATA0 only)		0.512		3.072	MHz
f <sub>I2S_LR</sub>	I <sup>2</sup> S left right strobe Input frequency (I <sup>2</sup> S_DATA0,1,2)	Deviation = ±250 ppm	32		48	kHz
f <sub>I2S_SCL</sub>	I <sup>2</sup> S serial clock input frequency (I <sup>2</sup> S_DATA0,1,2)		2.048		3.072	MHz
R <sub>I2S_SCL</sub>	I <sup>2</sup> S Serial Clock Input Ratio		0.9		1.1	
<b>I<sup>2</sup>S Output (I<sup>2</sup>S_DATA0 only)</b>						
V <sub>I2SOL</sub>	Output I <sup>2</sup> S Low Level Voltage	IOL = 2 mA			0.4	V
V <sub>I2SOH</sub>	Output I <sup>2</sup> S high level voltage	IOH = 2 mA	2.4			V
f <sub>I2S_OLR</sub>	I <sup>2</sup> S left right strobe output frequency	Deviation = ±250 ppm	8		48	kHz
f <sub>I2S_OSCI</sub>	I <sup>2</sup> S serial clock output frequency		0.512		3.072	MHz
R <sub>I2S_SCL</sub>	I <sup>2</sup> S serial clock output ratio		0.9		1.1	
t <sub>I2S_DeI</sub>	I <sup>2</sup> S output delay after falling edge of clock	See <a href="#">Figure 49</a> , C <sub>LOAD</sub> = 30 pF			30	ns

Figure 49. I<sup>2</sup>S input bus timings

# 18 Package mechanical data

Figure 50. 80-pin thin plastic quad flat package

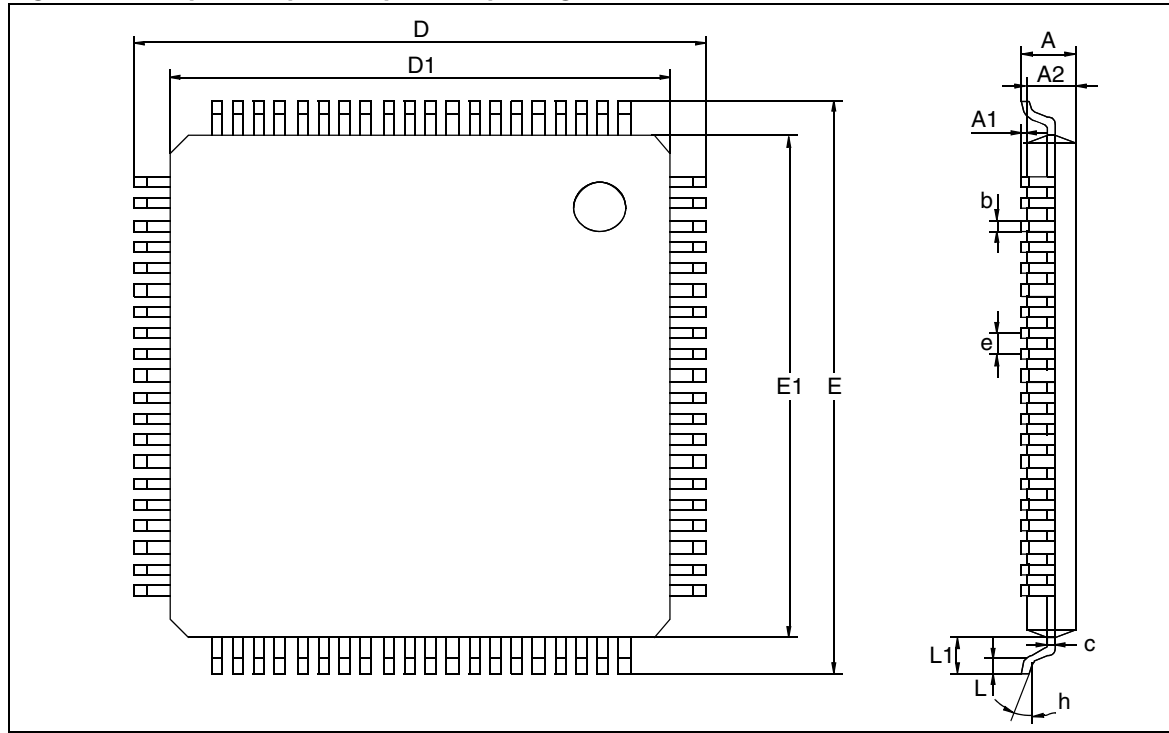


Table 46. Package mechanical dimensions

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.65			0.026	
K	0°	3.5°	0.75°	0°	3.5°	0.75°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	

## 18.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 19 Order information

**Table 47. Order codes**

Part number	Package	Conditioning
STV82x7	TQFP80	Tray
STV82x7/T	TQFP80	Tape & reel

*Note:* For example: STV8257DSX/T will be delivered in tape & reel conditioning

## 20 Revision history

**Table 48. Document revision history**

Date	Revision	Changes
24-Jan-2006	1	Initial release
01-Mar-2007	2	New template applied
08-Sep-2009	3	New template applied Specific part numbers added to cover page References to inactive products removed <i>Section 18.1: ECOPACK®</i> added

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