DB-54003L-512

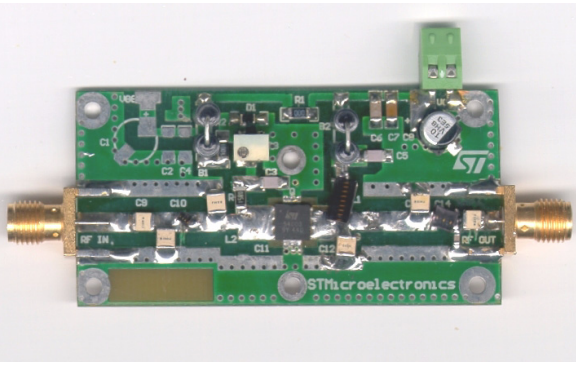
RF power amplifier using 1 x PD54003L N-channel enhancement-mode lateral MOSFETs

Features

- Excellent thermal stability
- Frequency: 380 - 512 MHz
- Supply voltage: 7.5 V
- Output power: 5 W
- Efficiency: 54 % - 63 %
- Load mismatch: 20:1
- BeO free amplifier

Description

The DB-54003L-512 is a common source N-channel enhancement-mode lateral field effect RF power amplifier designed for 2 ways comms UHF portable radio.



Mechanical specification:
L = 60 mm, W = 30 mm

Table 1. Device summary

Order code
DB-54003L-512

Contents

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	16	V
I_D	Drain current	1.6	A
P_{DISS}	Power dissipation	8	W
T_{CASE}	Operating case temperature	-20 to +85	°C
T_A	Max. ambient temperature	+55	°C

2 Electrical characteristics

T_A = +25 °C, V_{DD} = 7.5 V, I_{DQ} = 100 mA

Table 3. Electrical specification

Symbol	Test conditions	Min.	Typ.	Max.	Unit
Freq	Frequency range	380		512	MHz
P_{OUT}		4	5		W
Gain	@ P_{OUT} = 5W		12.6 ± 0.9		dB
ND	@ P_{OUT} = 5W		54 - 63		%
H2	2^{ND} Harmonic @ P_{OUT} = 5W			-50	dBc
H3	3^{RD} Harmonic @ P_{OUT} = 5W			-60	dBc
VSWR	Load mismatch all phases @ P_{OUT} = 5W			20:1	

3 Impedance

Figure 1. Impedance graphic

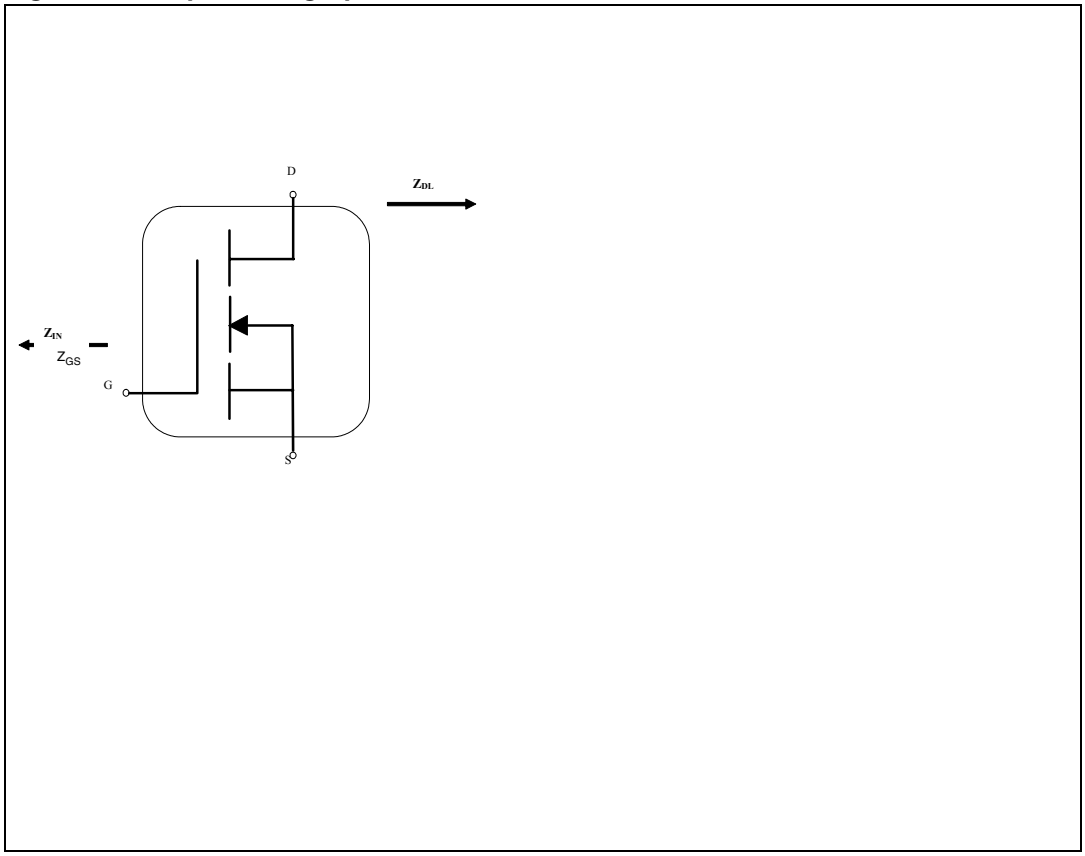


Table 4. Impedance data

F(MHz)	Z_{GS}	Z_{DL}
360	2.4 + j2.8	3.3 + j1.8
380	2.4 + j3.6	3.9 + j2.1
400	2.5 + j4.4	4.4 + j2.0
420	2.7 + j5.1	4.5 + j1.6
440	3.2 + j5.7	4.1 + j1.3
460	3.7 + j6.0	3.4 + j1.3
480	4.0 + j5.7	2.8 + j1.8
500	3.6 + j5.0	2.6 + j2.4
520	2.1 + j5.1	2.8 + j2.8

4 Typical performance

Figure 2. Output power vs input power

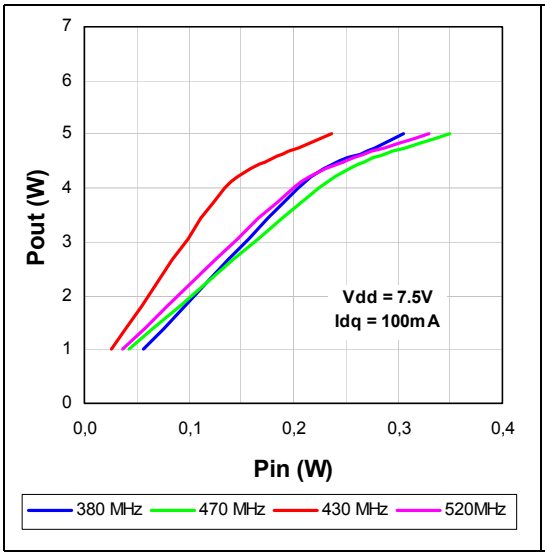


Figure 3. Gain and efficiency vs frequency

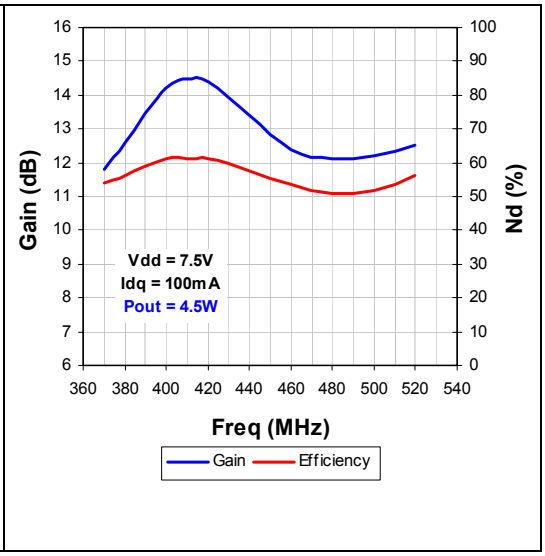


Figure 4. Gain and efficiency vs frequency

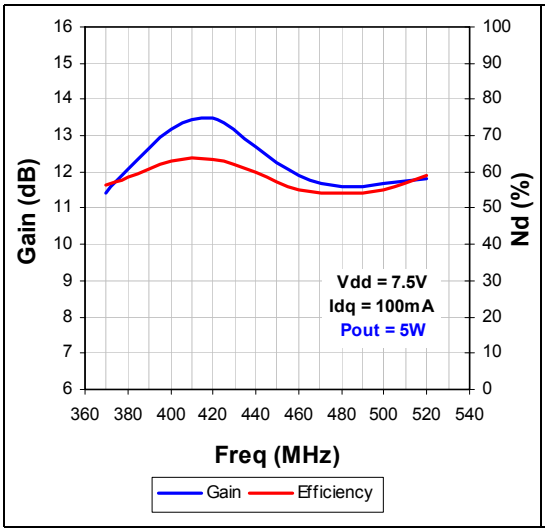


Figure 5. Gain and efficiency vs output power

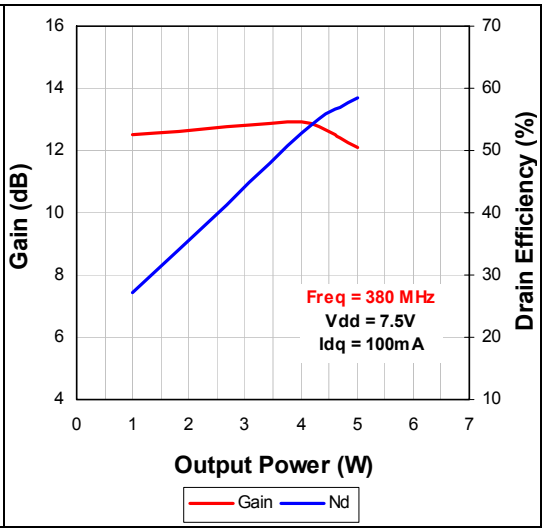


Figure 6. Power gain and efficiency vs output power

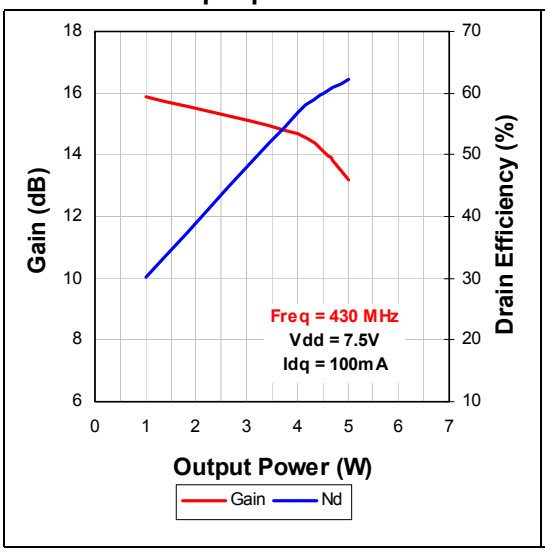


Figure 7. Power gain and efficiency vs. output power

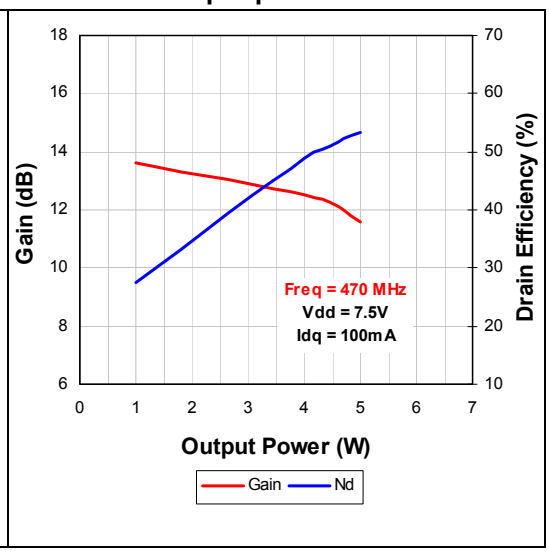


Figure 8. Power gain and efficiency vs output power

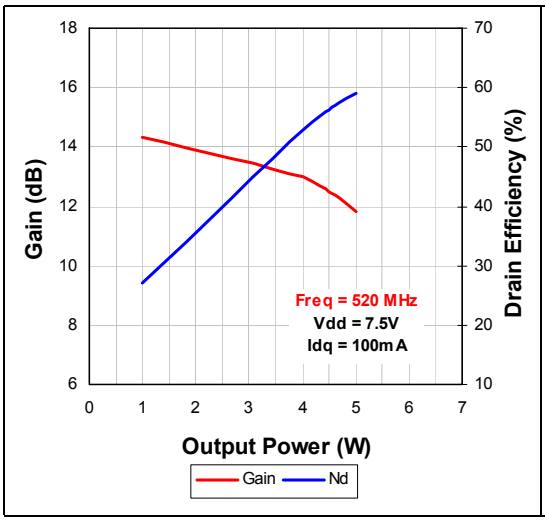


Figure 9. Input return loss vs frequency

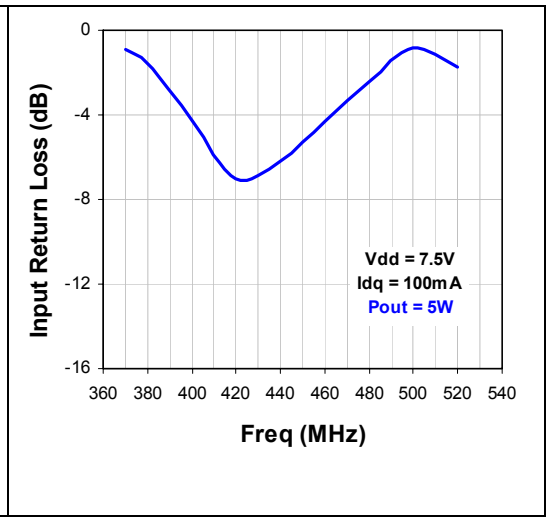


Figure 10. Output power vs drain voltage

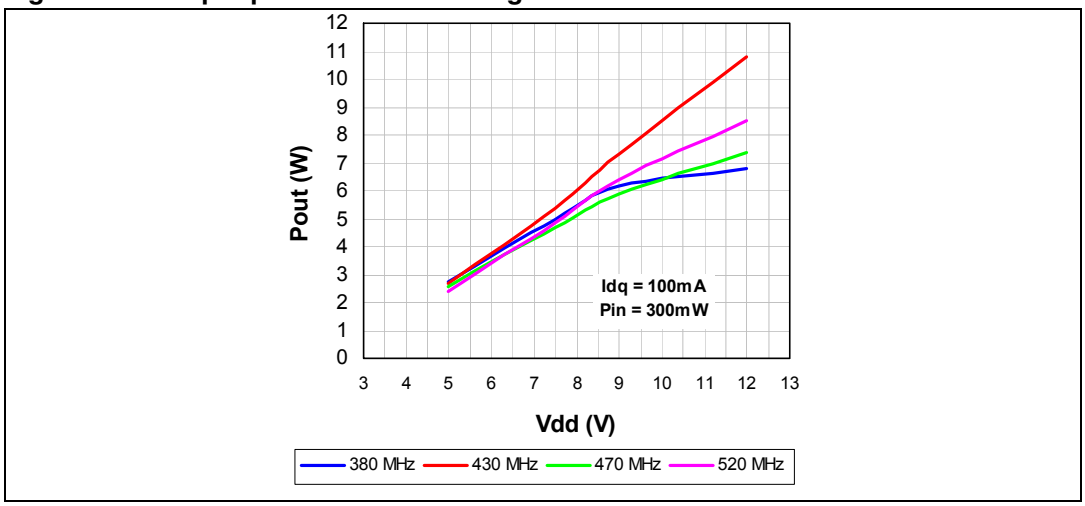
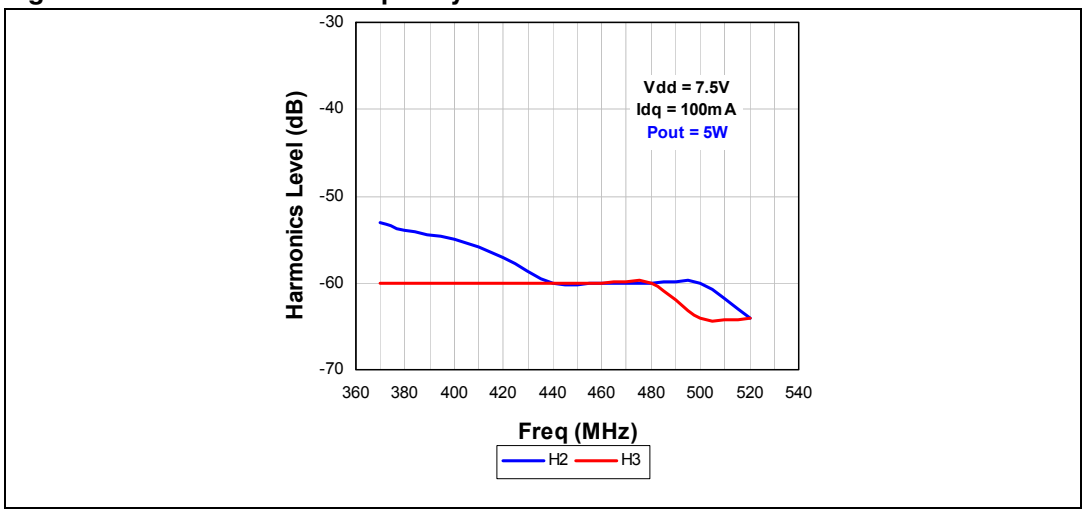


Figure 11. Harmonics vs frequency



5 Circuit layout

Figure 12. Schematic layout

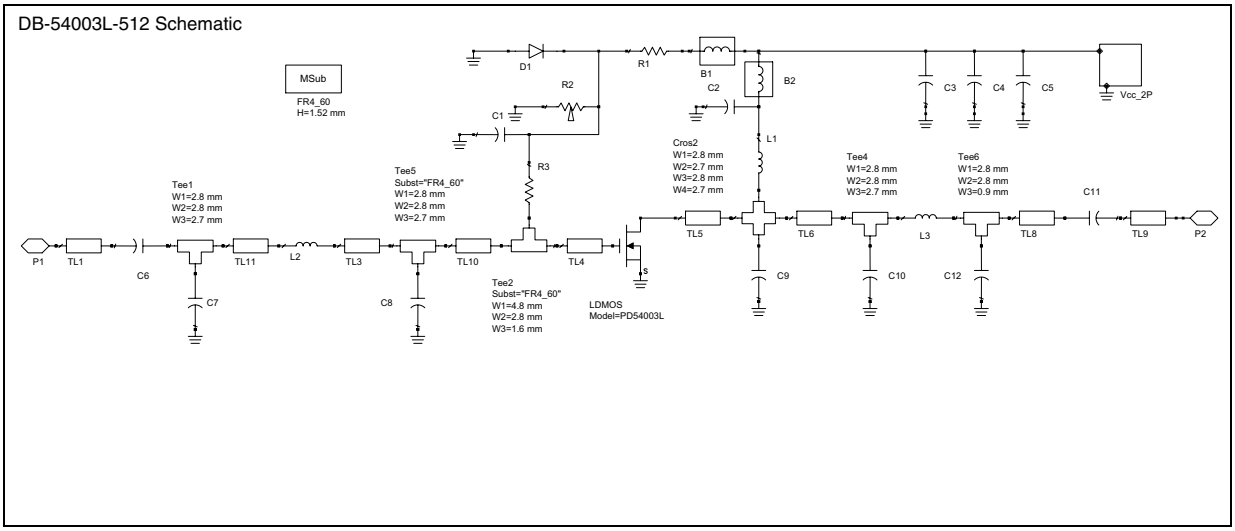


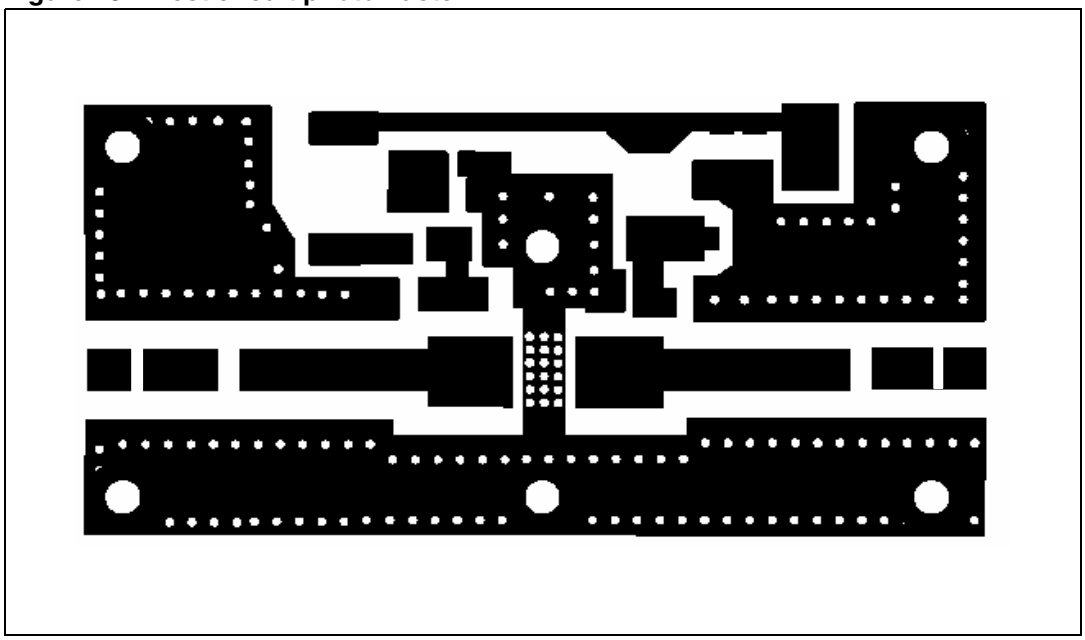
Table 5. Bill of materials

Component ID	Description	Value	Case size	Manufacturer	Part code
B1	Ferrite bead			Panasonic	EXCELDRC35C
B2	Ferrite bead			Panasonic	EXCELDRC35C
C1, C2	Capacitor	120 pF	1206	Murata	GRM42-6 COG 121J 50
C3	Capacitor	1 nF	1206	Murata	GRM42-6 COG 102J 50
C4	Capacitor	10 nF	1206	Murata	GRM42-6 X7R 103K 50
C5	Capacitor	10 uF	SMT	Panasonic	EEVHB1V100P
C6, C11	Capacitor	330 pF	100B	ATC	ATC 100B 331JW
C7	Capacitor	18 pF	100B	ATC	ATC 100B 180BW
C8,C10	Capacitor	33 pF	100B	ATC	ATC 100B 330JW
C9	Capacitor	43 pF	100B	ATC	ATC 100B 430JW
C12	Capacitor	12 pF	O6O3	Murata	CQM1885C1H120J
D1	Zener diode	5.1 V	SOD110	Philips	BZX284C5V1
L1	Inductor	35,5 nH	B0	Coilcraft	B09T
L2	Inductor	3,85 nH	0906	Coilcraft	0906-4JLB
L3	Inductor	8 nH	A0	Coilcraft	A03TJLB
R1	Resistor	1 KW	1206	Bourns electronics	SMT 1206-1 kOhm
R2	Potentiometer	10 KW		Bourns electronics	3214W-1-103E
R3	Resistor	15 W	1206	Bourns electronics	SMT 1206-15 Ohm
TL1	Transmission line	W=2.87 mm	L= 7,4 mm		

Table 5. Bill of materials (continued)

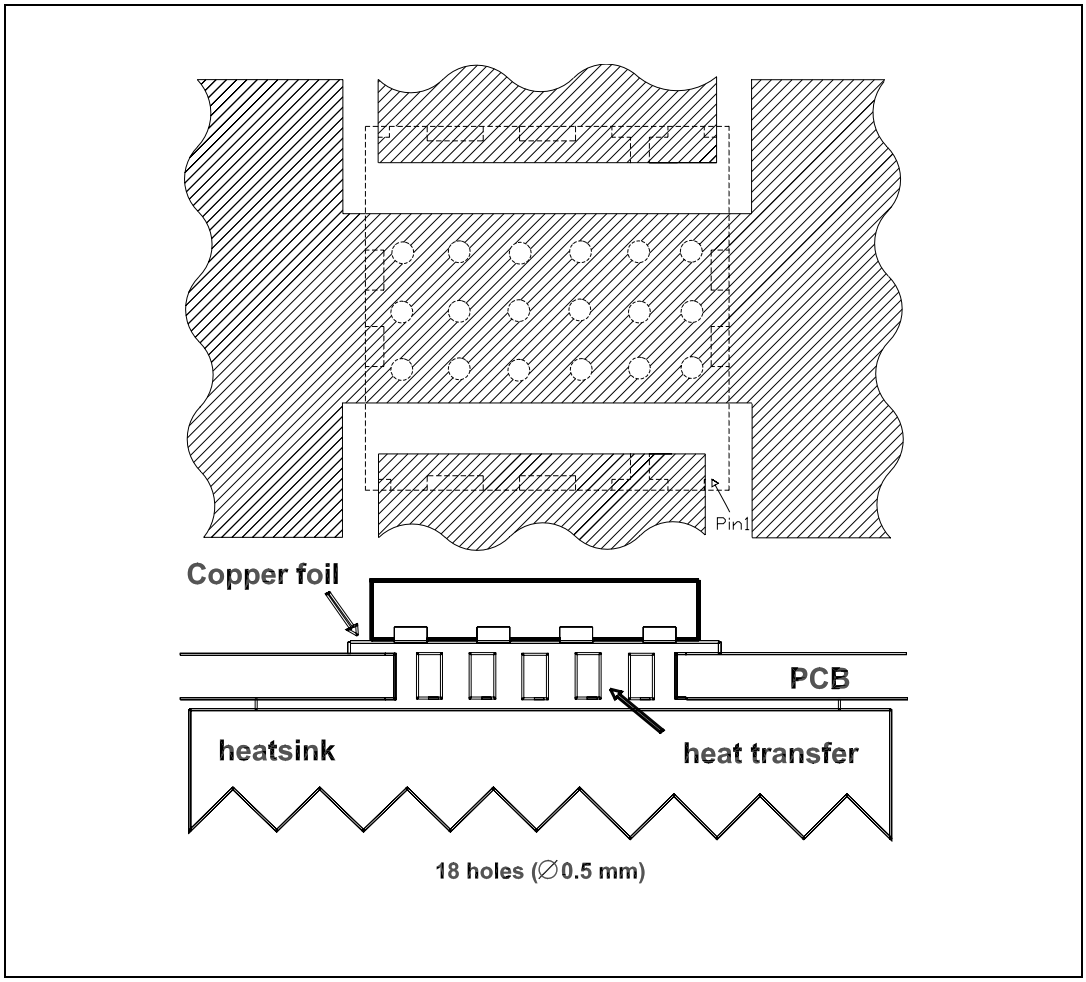
Component ID	Description	Value	Case size	Manufacturer	Part code
TL2	Transmission line	W=2.87 mm	L= 11,2 mm		
TL3	Transmission line	W=4.98 mm	L= 2.9 mm		
TL4	Transmission line	W=4.98 mm	L= 3.9 mm		
TL5	Transmission line	W=4.98 mm	L= 3.4 mm		
TL6	Transmission line	W=2.87 mm	L= 7.7 mm		
TL8	Transmission line	W=2.87 mm	L=1.7 mm		
TL9	Transmission line	W=2.87 mm	L=7.3 mm		
TL10	Transmission line	W=2.87 mm	L= 1.3 mm		
TL11	Transmission line	W=2.87 mm	L= 0.9 mm		
Vcc_2P	Connector DC	2 poli	2.54mm	Phoenix contact	1725656
P1_P2	RF Connector	SMA_Female	Flange solder		1.54mm
PD54003L-E	LDMOS			STMicroelectronics	PD54003L-E
Board	FR-4 THk=0.060" 2OZ Cu both sides_SnPb plated				

Figure 13. Test circuit photomaster



6 Mounting indications

Figure 14. Standard SMD mounting



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 6. PowerFLAT™ mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.24			0.009	
AA	0.15	0.25	0.35	0.006	0.01	0.014
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.64	0.71	0.79	0.025	0.028	0.031
D		5.00			0.197	
d		0.30			0.011	
E		5.00			0.197	
E2	2.49	2.57	2.64	0.098	0.101	0.104
e		1.27			0.050	
f		3.37			0.132	
g		0.74			0.03	
h		0.21			0.008	

Figure 15. PowerFLAT™ package dimensions

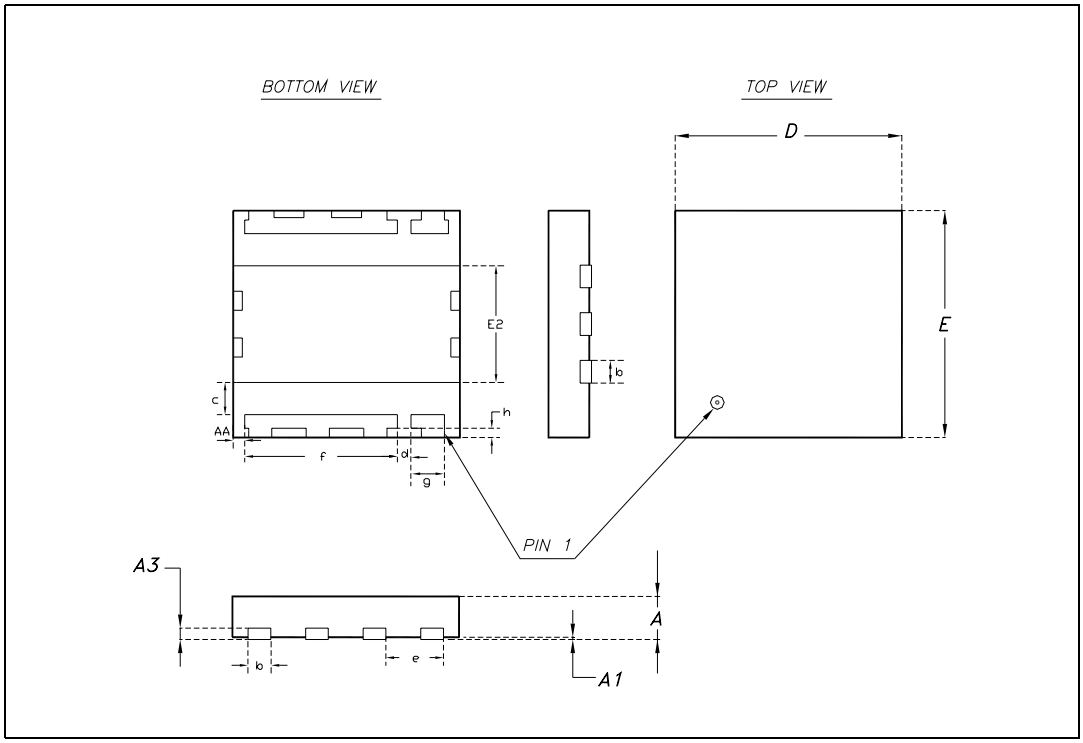
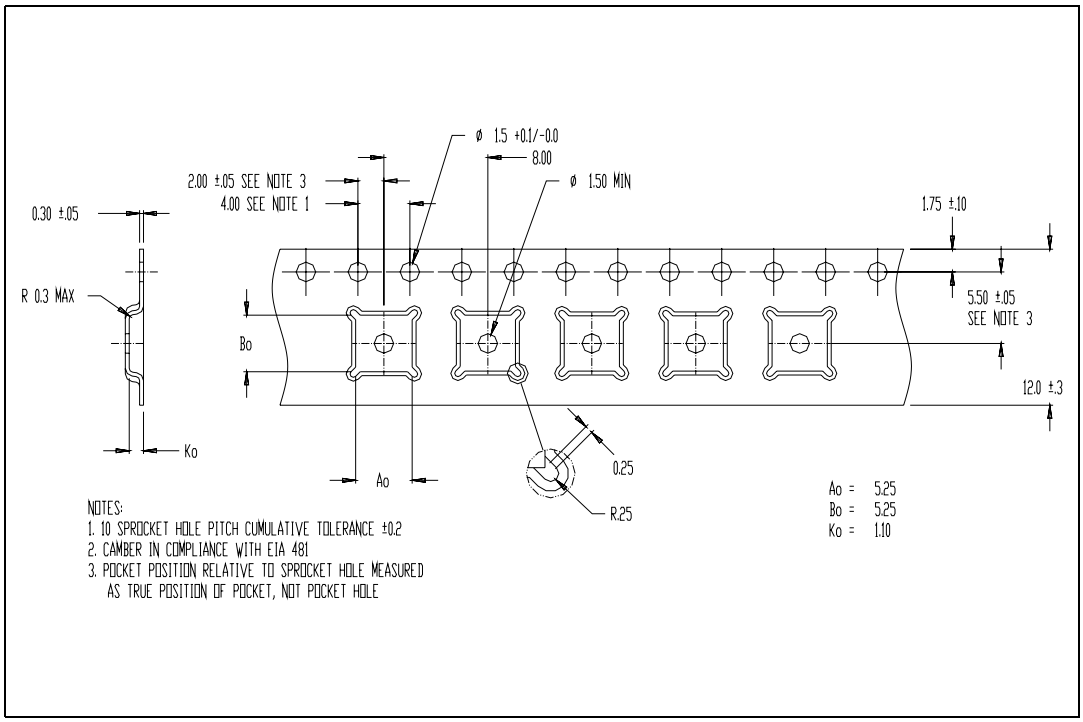


Table 7. PowerFLAT™ tape and reel dimensions

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
Ao	5.15	5.25	5.35	0.12	0.13	0.13
Bo	5.15	5.25	5.35	0.12	0.13	0.13
Ko	1.0	1.1	1.2	0.02	0.02	0.02

Figure 16. PowerFLAT™ tape and reel



8 Revision history

Table 8. Document revision history

Date	Revision	Changes
16-Mar-2006	1	Initial release.
10-Mar-2008	2	Updated: Cover page photo, *Section 5 on page 9*

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