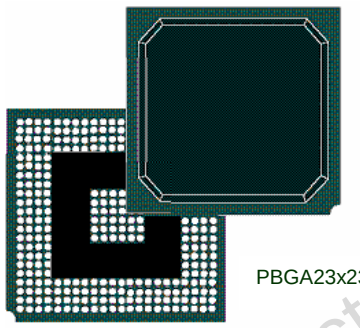
STE12PS

12 channel integrated PSE line manager

Preliminary Data

Features

- PSE power control device
- Supports up to 12 independent, 4[(a)]or 6[(b)] 30W “boosted” ports
- Wide operating range: up to 90V
- IEEE 802.3af compliant
- Open circuit detection: AC and DC methods
- Advanced power management algorithm
- Current sensing with as low as 500mΩ, external, series resistors
- No need for external FETs
- In-rush current control
- Short-circuit protection
- Adaptable signature detection capability
- On-chip 3.3V SMPS controller
- Low-noise, 12-bit ADC
- Standard I^2C interface
- Parallel monitor interface



Description

STE12PS is designed to supply power over multiple Ethernet channels in order to avoid different, individual power supply units for applications such as Web cams, IP Phones, Bluetooth access points and WLAN access points.

The equipment that provides the power to the twisted pair cabling is referred to as Power Sourcing Equipment (PSE).

The PSE’s main functions are: looking for links to a Powered Device (PD), classifying a PD, supplying power to the link, monitoring power on the link, and removing power from the link.

The STE12PS is fully programmable, supporting the detection and powering of IEEE802.3af as well as legacy PDs. The flexibility of the STE12PS allows the user to select a suitable system configuration: up to 12 ports as well as 4[(a)] or 6[(b)] “boosted” channels. If needed, the STE12PS can also efficiently manage cases or applications where a limited amount of power is available to the ports (smart-power capability) by means of integrated, power MOSFET devices. All operations are controlled via the I^2C bus also notifying externally some ports status condition via dedicated pins.

Ethernet port isolation can be easily maintained thanks to an integrated 3.3V SMPS power source and by means of optocouplers.

The STE12PS has five address selection inputs to choose up to 32 possible different addresses.

Power can be provided to the PD using either spare lines of the Ethernet cable or using the data wires, as specified by IEEE 802.3af.

a. In AUTO mode

b. In MANUAL mode

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1 Block diagram

Figure 1. STE12PS functional block diagram

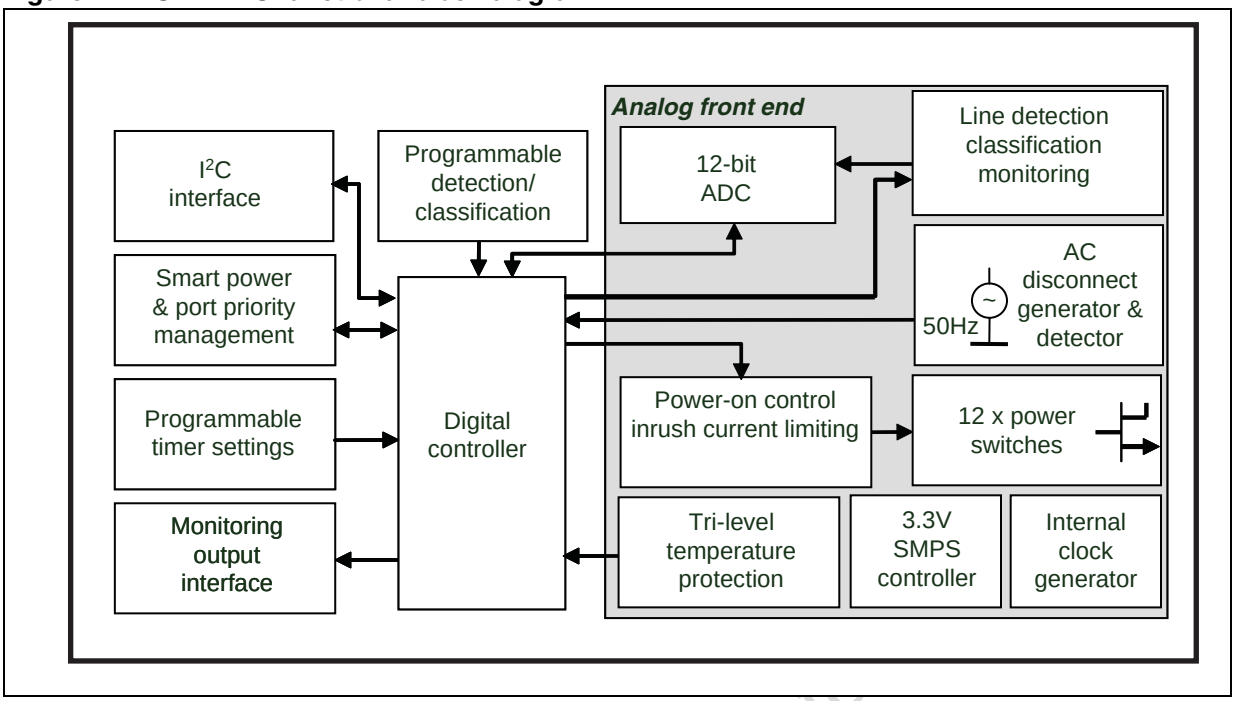
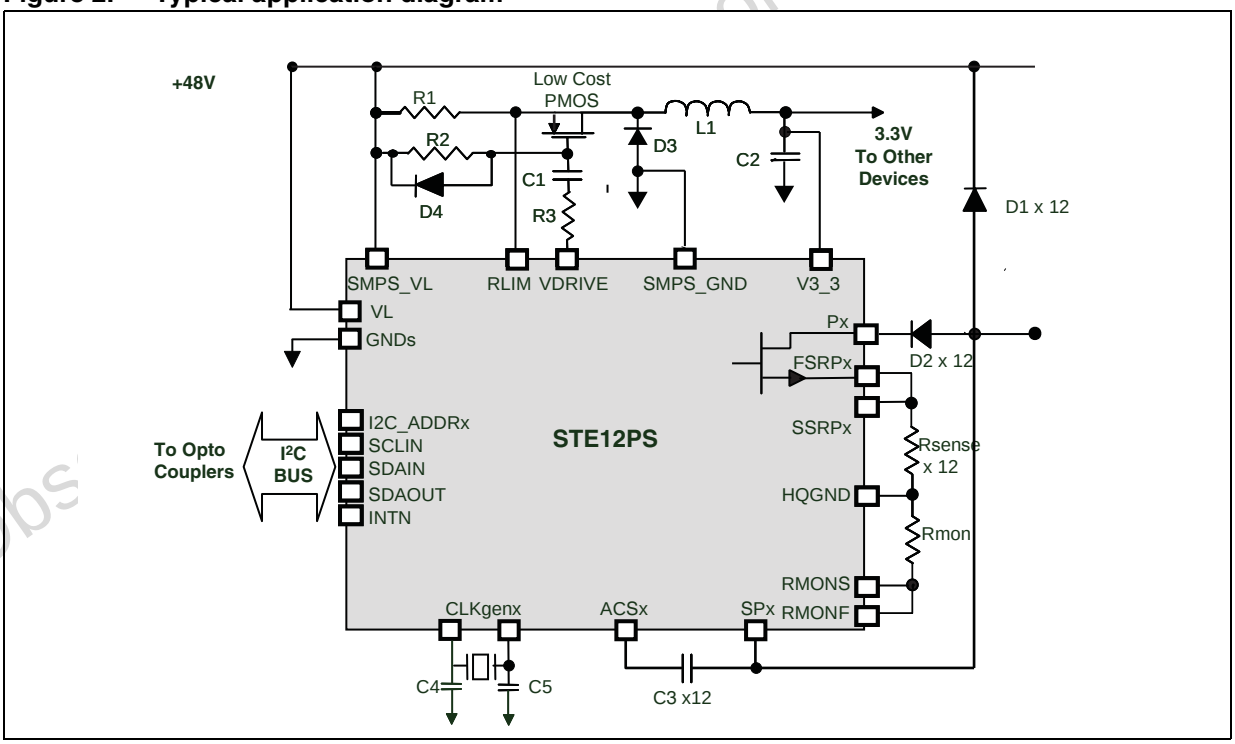


Figure 2. Typical application diagram



2 Pin description

Table 1. Analog pins description

Pin name	I/O	Function
IDET_HVLV	O	Anti-aliasing filter capacitor to be connected between the analog input and ground to improve ADC noise performance. C = 180pF.
IMON_HVLV	O	Anti-aliasing filter capacitor to be connected between the analog input and ground. C = 180pF.
Vbat_mon	O	Anti-aliasing filter capacitor to be connected between the analog input and ground. C = 100nF.
Vbatref	O	Anti-aliasing filter capacitor to be connected between the analog input and ground. C = 100nF.
I_REF	O	Anti-aliasing filter capacitor to be connected between the analog input and ground. C = 180pF.
CDETSLOW	O	Detection rise/fall time capacitor (up to 25nF). Tr/f can be set from 1ns to 4ms.
RSENSE	O	SMPS precision, external, current limiting reference resistor: 100mΩ
VDRIVE	O	External p-channel MOSFET gate driving voltage for SMPS. It provides a square wave with VL as upper limit and (VL-10V) as lower limit voltage.
SFTSTR	O	Switched Mode Power Supply (SMPS) soft start capacitor, 200nF.
FB	IO	SMPS feedback pin, Cfb = 2.2nF
Pn	O	Power DMOS device drain, if DMOS is turned-on, channel “n” where n = 1,…12 is activated.
ACSn	O	It provides a 50Hz AC disconnection signal for port “n”, n = 1, … 12.
SPn	I	Detection classification and AC disconnection sensing port “n”, n = 1, … 12.
SSRPn	I	Line current to the monitoring resistor for channel “n”, n = 1,… 12. Allowed values are 0.523, 1.05, 1.58 and 2.1ohms (see also SENSPROG preset pins). Sensing pin.
FSRPn	O	Source terminal for power DMOS connected to the sense resistor for channel “n”, n = 1,… 12, a “forcing” pin.
RMONF	O	Mirror monitoring resistance (500 × R_{sense}) pin to let internal ADC evaluate line currents. Forcing pin.
RMONS	O	Mirror monitoring resistance (500 × R_{sense}) pin to let internal ADC evaluate line currents. A “sensing” pin.
RREF	I	Reference bias resistor: 18.7kΩ
CLK_GEN1	I	Crystal oscillator pin1 for high performance clock generation.
CLK_GEN2	I	Crystal oscillator pin2 for high performance clock generation.
MCLK	O	Master clock output for multi device configuration.
CLK_GEN3	I	Low profile clock input pin or clock input pin in multi-device configuration.
ACin	I	50Hz sinusoidal input
ACout	O	50Hz sinusoidal output, internally generated

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Table 2. Digital pins description

Pin name	I/O	Function
Reset		
RESETN	I	Reset pin. Active LOW
Status flag interface		
CH_SELn	O	Channel identification “n”, where n = 1,… 12. Indicates the channel whose status flags (POK, …) are currently notified externally. CH_SEL is incremented every 60 * MCLK clock cycles. The status flag notification is enabled via the configuration register Global_cfg2, STATUS_FLAG_EN bit.
POK	O	Power OK flag. This flag indicates condition of the currently powered channel: ‘1’→power ON *and* NO faults are present ‘0’→power OFF *or* (power ON *and* faults present)
OVLD	O	Overload Alarm Flag for the currently powered channel. Current overload condition (Icut is over threshold): ‘1’→channel overload condition detected ‘0’→NO overload
OVCUR	O	Short circuit Alarm Flag for the currently powered channel. Current limiting condition: ‘1’→Overcurrent or detection failed condition detected ‘0’→ANY Short Circuit condition detected
AC_DC_DISCON	O	AC/DC Disconnection Alarm Flag for the currently powered channel: ‘1’→AC/DC disconnection detected ‘0’→ANY disconnection detected
DET_CLASS	O	Detection/Classification flag. ‘1’→Detection or Classification procedure is running ‘0’→Detection/Classification procedure is not running.
Por_N	O	‘1’ →VL, 10V and 3.3V supply Power ON succeeded
Thermal monitoring		
T_MONITOR*x*	O	Thermal monitoring (x = 0,1). These bits encode the internal temperature’s threshold measured in the following way: “00” →Temperature under 110°C “01” →Temperature between the 110°C to 130°C “11” →Temperature between the 130°C to 150°C “10” →Temperature is above 150°C

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Table 2. Digital pins description (continued)

Pin name	I/O	Function
Configuration signals		
A_BN_SEL	I	A or B alternative configuration mode select. '0'→Alternative B (Midspan-PSE) '1'→Alternative A (Endpoint-PSE)
CH_NUM*x*	I	12- or 4-boost channel select. x = 0,1. '00' →12 channels configuration '01' →NA '10' →NA '11' → 4-boost channel configuration
AUTO_START	I	AUTO Start Mode enable. '0'→Auto Start Mode disabled: all the ports are disabled after Reset, Neither detection nor power on is performed (MODE[1:0] register selected to Power Down at the reset event) '1'→Auto Start Mode enabled: all the ports are automatically enabled, detection, classification and power are performed (MODE[1:0] register selected to AUTO after the reset event)
S/UPIN	I	SMPS (Switch Mode Power Supply) mode selector bit (supplier / User). When Not connected the device works as DC-DC converter controller.
SENSEPROG*x*	I	Preset pins for sensing resistor programmability (x=0,1). The programmed value must match the mounted R_{sense} resistors. '00' →R_{sense} = 0.5Ω '01' →R_{sense} = 1Ω '10' →R_{sense} = 1.5Ω '11' →R_{sense} = 2Ω
Power ON controller signals		
POWER_EN*x*	I	Reserved. (x = 0, …11).
I^2C Signals		
I2C_ADDR*x*	I	This defines the device address for the I^2C interface. x = 0, … 4.
SCLIN	I	Serial clock input pin for the I^2C interface.
SDAIN	I	Serial data input pin for the I^2C interface. When "jumpered" with the SDAOUT pin, this connection becomes the standard bi-directional serial data line (SDA).
SDAOUT	O	Serial data output pin for the I^2C interface. When jumpered with the SDAIN pin, this connection becomes the standard bi-directional serial data line (SDA).
INTN	O	I^2C Open drain output that goes low when interrupt event is notified
Test mode signals		
TEST_MODE*x*	I	Test Mode Enable (x = 0,1). '00' →Functional mode '01' →Reserved '10' →Reserved '11' →Reserved
SCAN_EN	I	Reserved. Preset to '0'.

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Table 3. Power and ground pins description

Pin name	I/O	Function
GND, AGND	I	Analog grounds
SMPSGND	I	SMPS power ground
SMPS_VL	I	+48V battery voltage for SMPS
V3_3,Vdd,Vdde	I	3.3V supply
V10, Vdd10	I/O	10V supply to power-up the output DMOS and minimize its ON resistance
HQGND	I	Dedicated ground for Kelvin line current sense resistor (a high quality ground)
DGND, gnd, gnde	I	Digital grounds
VL	I	+48V battery voltage.

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3 Functional description

The STE12PS architecture provides a complete PSE interface and smart digital controller to efficiently manage the functions in a PoE system. All operations can be controlled through R/W registers via a standard I^2C bus interface.

The STE12PS is designed to control power delivery of up to 12 separate lines. This is performed by controlling 12 integrated, power MOS transistors connected to the low side of the line - monitoring the line voltage and sensing line current by means of external, series sensing resistors (one per port). Turning on a port means to switch the relative MOS transistor thus controlling the inrush current in order to rise the port voltage up to 48V (typical battery voltage) after a valid PD signature has been detected. The flexibility of the STE12PS allows the user to select a suitable system configuration: 12 "standard", 4 or 6 "boosted" 30W channels, by means of pins CH_NUMn. Also, one can select the type of architecture (Endpoint PSE/ Alternative A or Midspan PSE/Alternative B) for all channels via pin A_BN_SEL.

Some typical applications for the STE12PS include:

- Ethernet switches/routers
- Midspan power supplies
- IP-PBX
- WLAN access points

3.1 Operating modes

The digital controller can operate in one of five possible modes for all the channels, selectable through the Global Configuration registers: Stand-by, Auto, Semi Auto, Manual or Power Down.

When the reset condition is removed, the controller defaults to Power Down mode if the AUTO_START pin is tied low; if AUTO_START is tied HIGH the mode is configured in AUTO. The mode can be changed only during a limited amount of time (100ms), after the reset is released, accessing the Global Configuration registers before the detection procedure is started, or placing the device in STAND-BY mode via the I^2C interface.

The characteristics of the Five possible operating modes are described below:

- STAND-BY: the controller allows only the read write operations suitable for changing programmability. To enable this mode set the reset bit 1 of the REG0x05.
- AUTO: the controller autonomously performs detection, classification and Power ON command without the need of host commands. A subset of status flags stored in the channels monitor registers is reported externally through the Status Flag Notifies pins allowing operation without the presence of the host controller.
- SEMIAUTO: after a triggering command the controller autonomously performs detection and classification waiting a dedicated command from host processor for the power on. Based on the detection and classification results reported in the Channels Status registers, the host controller can decide to power on the selected channel. The disconnection of a channel is automatic as in the AUTO mode, unless disabled.
- MANUAL: any action is performed manually. The host controller has the responsibility to force any state transition in the FSM. Then based on the measures performed automatically by the ADC on several parameters, the host controller can decide to

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classify the channel and afterwards to issue the power on command. The STE12PS controller can also automatically disconnect a channel in fault condition (if not enabled, the STE12PS will notify automatically only a short circuit condition or an AC disconnection event. Overload or DC disconnection is responsibility of the host controller.) The host controller can also power on a channel skipping detection and/or classification procedures.

- POWER DOWN: the controller is put in power down state. No actions are performed until the power down mode is removed.

For all operating modes, except power-down and stand-by, the power ON/OFF condition of each channel can also be managed, directly, by the host processor or controller via a dedicated command.

Moreover, the power removal procedure is performed automatically (also in MANUAL mode) when a fault event has been detected (AC/DC disconnection, overload or overcurrent); this behavior can be changed configuring appropriately some dedicated enable/disable bits of channels event registers.

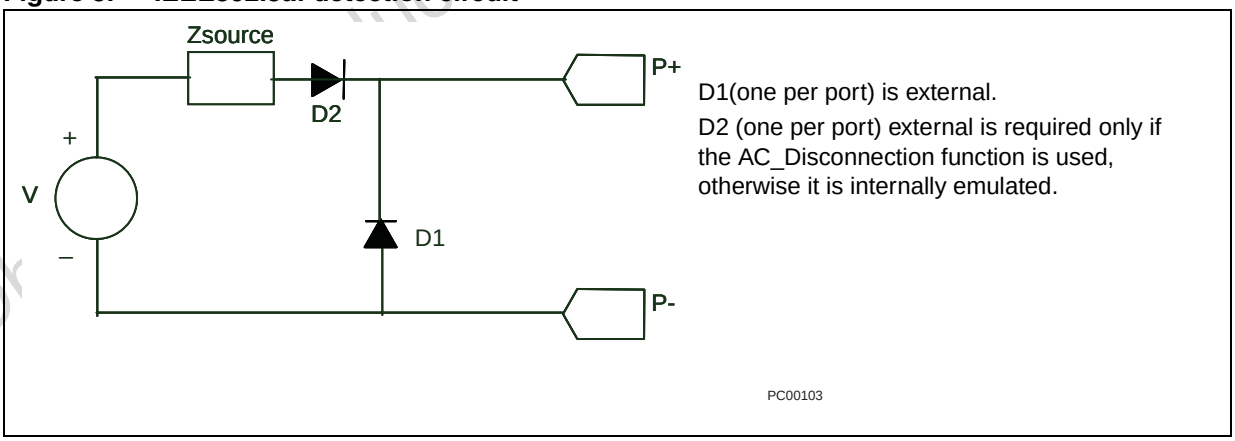
With Priority Management in AUTO mode and Smart-power management enabled, it is also possible to set different priorities for different channels. The STE12PS will probe channels starting from those with the highest priority. In case of a shortage of available power, it is also possible to disable powering of newly detected, lower priority ports until the highest detected ones are served.

3.2 Detection and classification

3.2.1 Detection

The STE12PS looks for, in turn on the free available ports (according to the priority list if enabled), for a valid PD signature (25kΩ slope characteristic) by driving two different voltage levels at the port (4V and 8V), and calculating the slope resistance/ conductance by monitoring the current difference. The equivalent circuit for the IEEE802.3af detection phase is shown in *Figure 3* below.

Figure 3. IEEE802.3af detection circuit



As detection is performed by multiplexing a common voltage generator. If more than one port is connected to several PDs, an extra delay in the detection start will be introduced. See *Table 12: Electrical characteristics*, parameter Tdetd.

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By default, the STE12PS will recognize a valid signature with the following characteristics:

– an inverse slope of the port current vs. voltage (I-V) characteristic measuring between 19 and 26.5kΩ (Rdl and Rdh),

– a port capacitance of less than 4µF.

If required, the STE12PS can also perform a custom, resistive detection search – modifying the acceptance window. This can be easily performed by changing the Rdh and Rdl limits or by changing Gdl and Gdh via the logic interface.

In Midspan applications, where power is applied via spare wires, when the PSE fails to detect a PD, the port remains in high-impedance (Hi-Z) for at least two seconds. If the signature resistance is greater than 500kΩ, then the two second wait is avoided.

Transition rates of the port voltage between the two probing levels can be adjusted with capacitance Cdetslow.

Table 4. PD power classification

Class	Usage	Maximum power level at PSE output (Pall)	Power level at PD input	I_{class}
0	Default	15.4W (programmable)	0.44 to 12.95W	I_{class} < Ithcl0
1	Optional	4W (programmable)	0.44 to 3.84W	Ithcl0 < I_{class} < Ithcl1
2	Optional	7W (programmable)	3.84 to 6.49W	Ithcl1< I_{class} < Ithcl2
3	Optional	15.4W (programmable)	6.49 to 12.95W	Ithcl2 < I_{class} < Ithcl3
4	Optional	-	Reserved	Ithcl3 < I_{class} < Ithcl4
0	Default	15.4W (programmable)	0.44 to 12.95W	Ithcl4 < I_{class}

3.2.2 Classification

Once a valid signature is detected, the port is probed for classification in order to perform smart-power management (if enabled).

Port probing is performed by forcing a DC voltage in the range of 16V to 18V (one DC generator multiplexed between the channels) and monitoring current I_{class}. The measurement is repeated and stored in the Channel Monitor Classification registers to ensure a coherent classification. The PD power class is defined as shown in *Table 4* above.

The detected class is then stored in the Channel Status registers.

Note: The power absorbed in a link is calculated considering the actual value of the battery voltage in order to arrive at a true power measurement result.

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3.2.3 Detection and classification FSM

This FSM manages all operations related to the detection and classification procedures.

For these two procedures, the following assumptions are made:

1. A channel is detected ONLY if:
   a) the channel has not yet been detected, *and* Channel Detection has been enabled, *and*
   b) the Backoff Detection timer *and* Subsequent Attempt timer are NOT running (after a corresponding fault detection or failed signature).
2. A channel is classified ONLY if:
   a) Channel Classification is enabled, *and*
   b) the previous related detection procedure has reported an Rgood/Ggood value (Auto and SemiAuto modes).

Three general macro operations can be performed:

- STARTUP: the following operations are related to the startup procedure:
  - RESET: reset and initialize all digital aspects of the STE12PS,
  - WAIT_POWER_UP: wait 100ms for completion of the power-up procedure. During this period, the I^2C bus is active - allowing the host to initialize registers while the detection procedure is waiting to start.
  - DETECTION START: all setting-up needed to start operations is performed in this state. The first battery voltage sample is latched in a dedicated register.
- DETECTION: the following operations are related to the detection procedure for the channel selected:
  - Low voltage detection command (4V) is issued via registers; detection timer is started to execute the command for a duration of ½Tdet ms.
  - Wait for 5ms to acquire a stable measurement.
  - Sampled sensing current values are acquired via A/D converter.
  - The samples previously acquired are averaged and the resulting value, reported into the Channels Monitor register, is compared against programmed min/max values. If the sensing current is higher than maximum allowed value, the detection procedure is considered as having FAILED: backoff timer is started (Alternative B) and an alarm flag raised according to the Channel Status registers.
  - If the sensing current results lower than the minimum allowed value the detection procedure is continued: the alarm flag is raised in the Channel Status registers.
  - The described operations are repeated for the High-Voltage detection command (8V).
  - Signature Resistance is calculated:
  - If 2µsec < Gmeas < Glow *or* Ghigh < Gmeas, then backoff timer is started (Alternative B) and detection result failure is reported in the Channel Status registers.
  - Else, Glow < Gmeas < Ghigh and the result of a successful detection is reported in the Channel Status registers.

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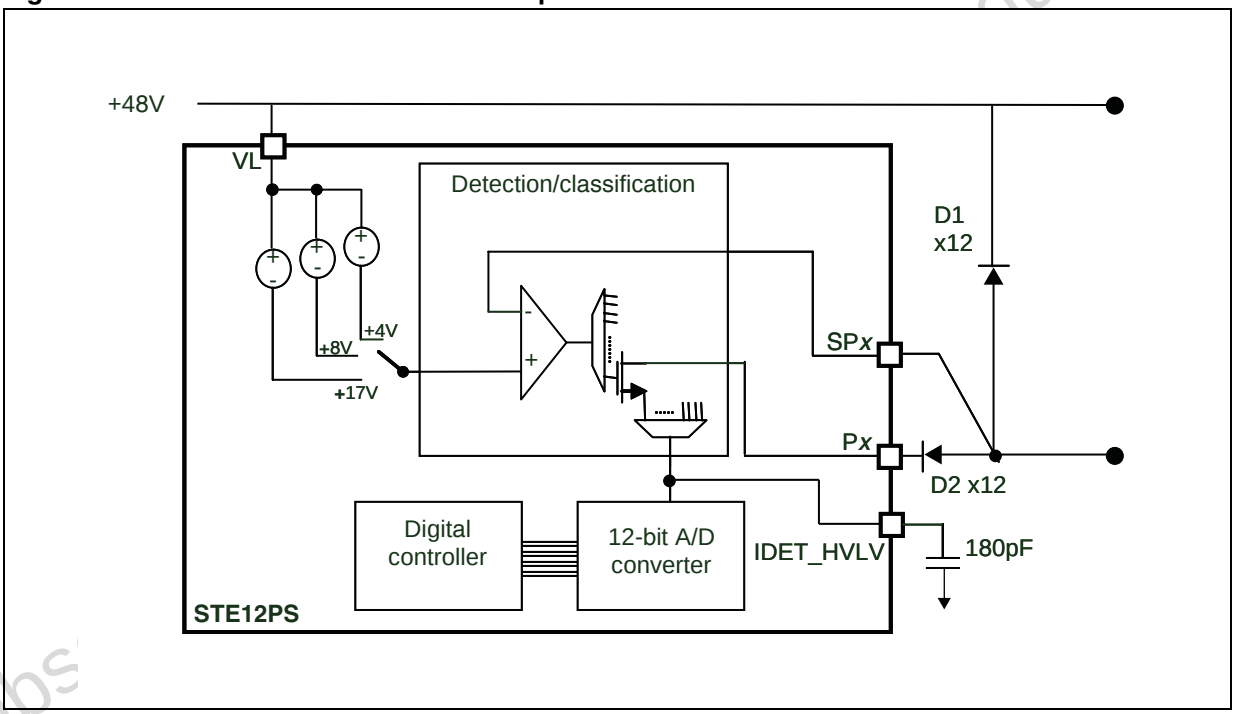
- CLASSIFICATION: The following operations are related to the classification procedure for the corresponding channel
  - If classification is not enabled, the default Class 0 is assigned.
  - High Voltage detection command (17V) is issued via registers; detection timer is started to execute the command for 15ms duration.
  - Wait for 5ms to acquire a stable measurement
  - Sampled sensing current values are acquired via A/D converter.
  - Average the previously acquired samples and report the resulting value in a dedicated register. The power class is identified and the result is reported in the Channel Status registers.
  - Channel is ready to be powered: if the smart-power algorithm is enabled (via the MISCELLANEOUS registers) the channel is powered only if the required power is within the remaining power budget; the channel can be powered regardless of the power-check availability via registers.

If the power availability check has a positive result (or it hasn't been performed), the channel is powered. Otherwise, it is rejected, and the alarm flag raised in the Channel Events register. The channel number is registered into a scheduler FIFO so that power will again be available when the channel is ready to be switched-on.

Figure 4. Detection and classification equivalent architecture



3.3 Power ON

After the classification phase the port will be powered.

Once activated, the power-on sequencer manages the channel's activation requests received through the signature detection circuitry. For the incoming channel, activation requests are stored in the power-on sequencer and then serviced, one at a time, only when the previously activated channel leaves the current limiting condition that normally occurs during power on due to the capacitive part of the load. (see also smart-power mode and special issues)

A port is turned-on by ramping-up the voltage and increasing the current limit to its upper limit. After a programmable time (T_{inrush}), if the port has reached full voltage and is out of current limitation, it is marked as powered. The related port power bit and the power class bits are set according to the class in the logic interface bit stream.

The active ports are continuously monitored in order to detect a fault condition such as Short Circuit, Disconnection or Excess Power (overload).

3.3.1 Under load (disconnection)

Detection of a disconnection, if enabled (default condition), can be performed via a DC and/or AC method - default is DC $\oplus$ AC (logical OR):

- DC method

  If this method is selected via the logic interface and if the port current drops under 7.5mA for more than 10ms, then the STE12PS will detect a DC disconnection. If this condition persist for Tmpdo (*Table 12*), then power is removed and the port is marked as free, enabling a new detection.

- AC method

  If this method is selected via the logic interface, the STE12PS probes the channels via coupling capacitors and detects when the AC load impedance, Z_{ac}, exceeds the maximum, 100kΩ limit for a time longer than 20ms. In this case, the PSE will detect an AC disconnection. If this condition persist for a time Tmpdo (*Table 12*), power is removed and the port is marked as free, enabling a new detection.

Disconnection modes are as following: Disabled, DC method only, AC method only, both AC and DC (combined in OR $\oplus$ logic or in AND $\otimes$ logic).

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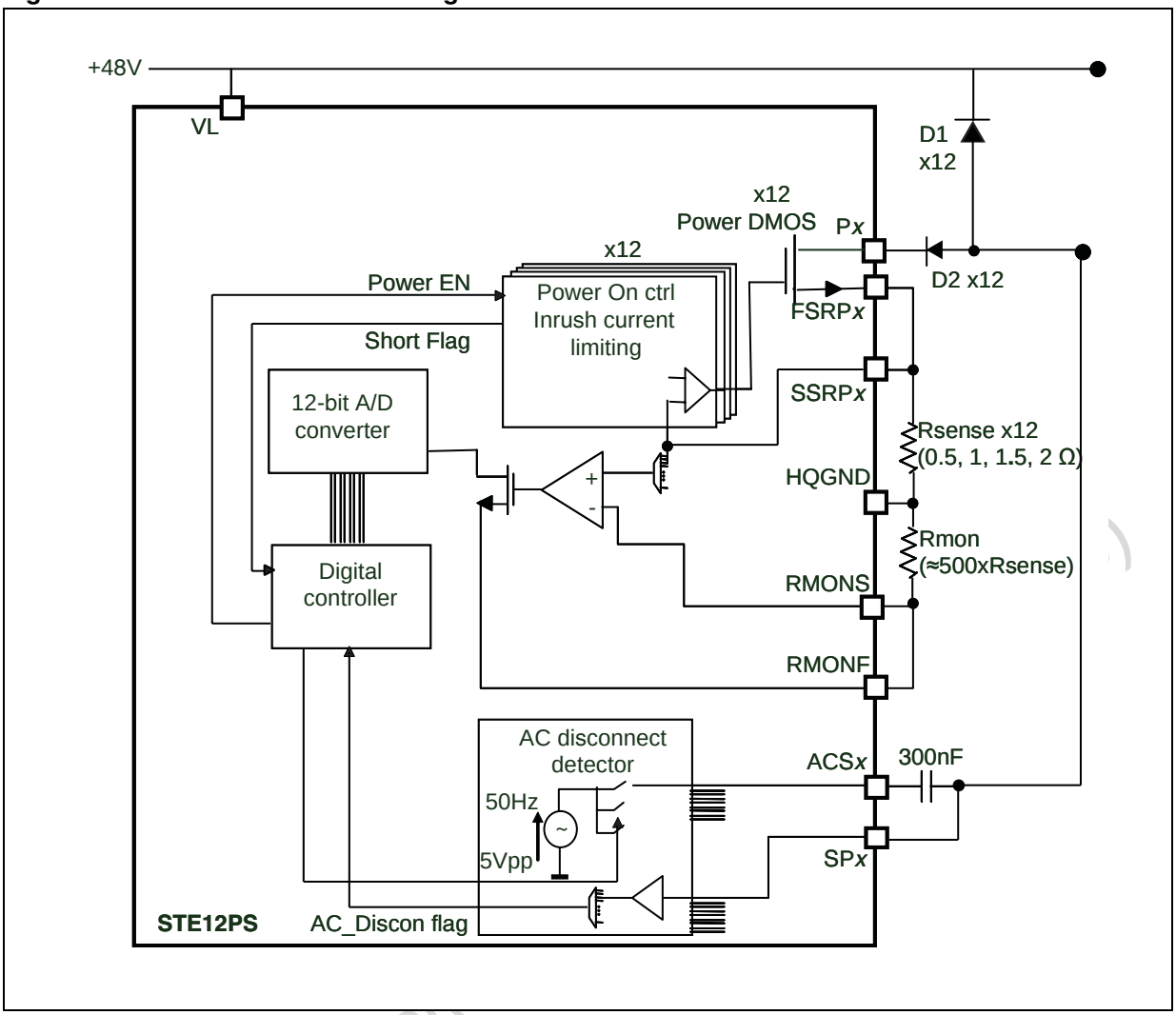
Figure 5. Power ON and monitoring



3.3.2 Short circuit, overload and overcurrent

A short circuit is defined when port current reaches 425mA, typ. Moreover, if port voltage drops below 25V, then maximum loop current is decreased, linearly, to limit power dissipation. A short condition is considered as a fault after a period of 65ms, typ. (see *Table 12: Electrical characteristics*, parameter Tshort).

When the above conditions are met, the port is disconnected, and the fault bit set HIGH in the Channel Event registers.

Overload or excess power is defined when port power consumption reaches 15.4W for longer than 65ms, typ. (see *Table 12: Electrical characteristics*, parameter Tovld).

If smart-power management is active, then the overload power limit is set instead - according to the power class.

When the above conditions are met, the port is disconnected, and the fault bit is set HIGH.

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Monitor overload FSM

This FSM manages all operations related to monitoring an overload event.

All operations described below are related to channels currently powered.

- STARTUP: the following operations are related to a startup procedure:
  - START: channel to be monitored is selected.
- POWER MEASUREMENT: the following operations are related to a power measurement procedure
  - SAMPLE Imeas: the current measurement is sampled and the next powered channel is prepared for the next monitor procedure.
  - MEASURE Power: the power is measured and its value is compared against the required Power class.
  - START MONITOR OVERLOAD: if the measured power exceeds the required power class the T_{ovld} timer and the averaging process are started.
  - COUNTER RESET: T_{ovld} timer is reset if the measured power doesn't exceed the required
- POWER REMOVAL: the following operations are related to a power removal procedure:
  - COUNTER CHECK: all T_{ovld} timers are checked, and those that have expired are identified.
  - POWER REMOVAL: all the channels whose timers have expired and whose average power exceeds the maximum are switched OFF through the POWER_EN(n) pins.
  - ALARM SET: for all the channels whose timers have expired, a corresponding alarm flag is raised in the Channel Event registers, and the related Ted timer is started.

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Monitor overcurrent FSM

This particular FSM manages all operations related to procedures that are able to monitor an overcurrent event.

All operations described below are related to channels currently powered.

- STARTUP:
  - START: the channel to be monitored is selected.
- VOLTAGE BATTERY:
  - SAMPLE V_{bat}: every 12 channels cycle the V_{bat} measurement is executed.
- OVERCURRENT CHECK: the following operations are related to an overcurrent check
  - I_{meas} CHECK: if $I_{meas}>I_{lim}$ the I_LIM_FLAG is raised and the next powered channel is prepared for the next monitor procedure.
  - START MONITOR: the T_{lim} counter is started if I_LIM_FLAG is found asserted.
  - COUNTER RESET: if I_LIM_FLAG is found de-asserted T_{lim} counter is reset taking into account that glitches of duration less than 10ms are filtered.
- POWER REMOVAL: the following operations are related to a power removal operation:
  - COUNTER CHECK: all the T_{lim} timers are checked and those expired are identified.
  - POWER REMOVAL: all the channels whose timer is expired are switched OFF.
  - ALARM SET: for all the channels whose timers are expired a corresponding alarm flag is raised in the FAULT_EVENT_CHn register and the related Ted timer is started.

3.3.3 Thermal monitoring

The procedures performed by the digital controller are impacted by the thermal monitoring data indicating the measured temperature.

Its behavior is based on a three-level control system*:*

1. When the chip's internal temperature reaches 110°C, only the channels already powered will be serviced. Possible new ones, will be rejected, redetected and eventually processed when the internal temperature cools down to 100°C. This behavior can be disabled setting the proper bit register.
2. A second temperature threshold is set at 130°C. When this value is reached, the channels that are in current limiting or inrush condition are immediately switched OFF, and their reactivation, subject to positive redetection, will only be possible when the chip's internal temperature has cooled down to 100 °C. This behavior can be disabled by setting the proper bit register.
3. The third temperature threshold is set at 150 °C. When this temperature is reached, all activated channels will be immediately switched OFF, and their reactivation, subject to positive redetection, will only be possible when the chip's internal temperature has decreased to 100°C. This behavior cannot be disabled.

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3.4 Internal 3.3V/10V generator

The STE12PS can be configured either as 3.3V and 10V generator or load by means of the S/U control input. In this manner, the need for extra, low-voltage batteries is avoided, greatly simplifying the system design. If S/U is left open, the device will operate as an SMPS controller. With the SMPS configured at 3.3V, the device can be used to power up a “1Amp” load with high efficiency voltage conversion.

Figure 6 on page 19 shows a typical DC-DC, buck converter configuration for the 3.3V supply. The 10V supply is generated by means of an internal, linear regulator. The 3.3V supply can source up to 1A.

In *Figure 7*, use of a small transformer for the 10V supply can save up to 0.3W for each powered device. Both the 3.3V and 10V supplies can power others devices.

Figure 8 depicts a typical application with an external supply.

3.5 Logic interface

The STE12PS can operate autonomously - notifying, externally, ports status via dedicated pins (Parallel Monitor Interface) - or it can be controlled as a slave device via the I^2C interface by a host processor. In the latter case, the host can perform system configurations, monitor status conditions and assert alarm flags making it possible to drive, manually, different operations for detection, classification and monitoring.

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Figure 6. Simple SMPS

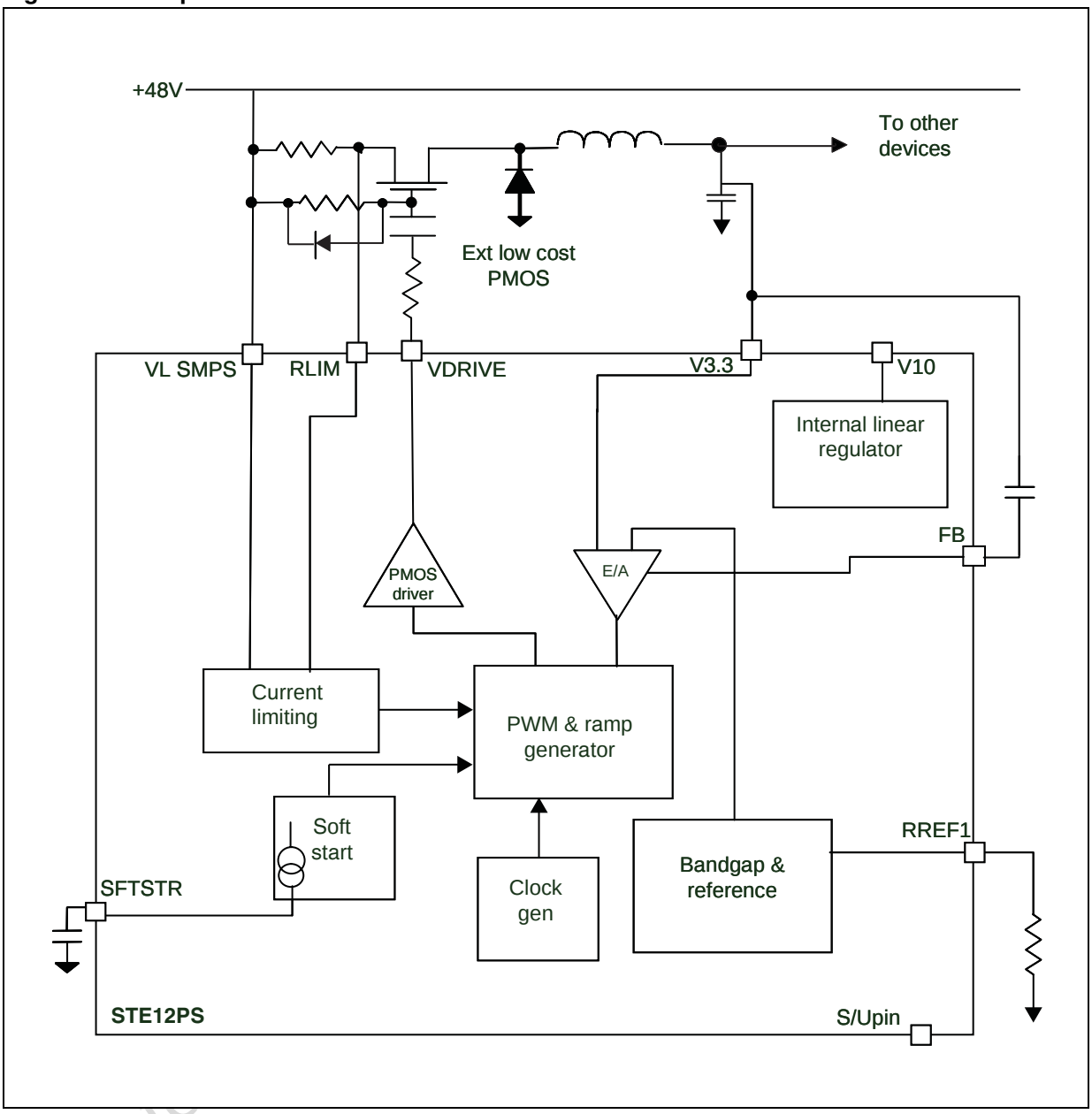

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Figure 7. Advanced SMPS

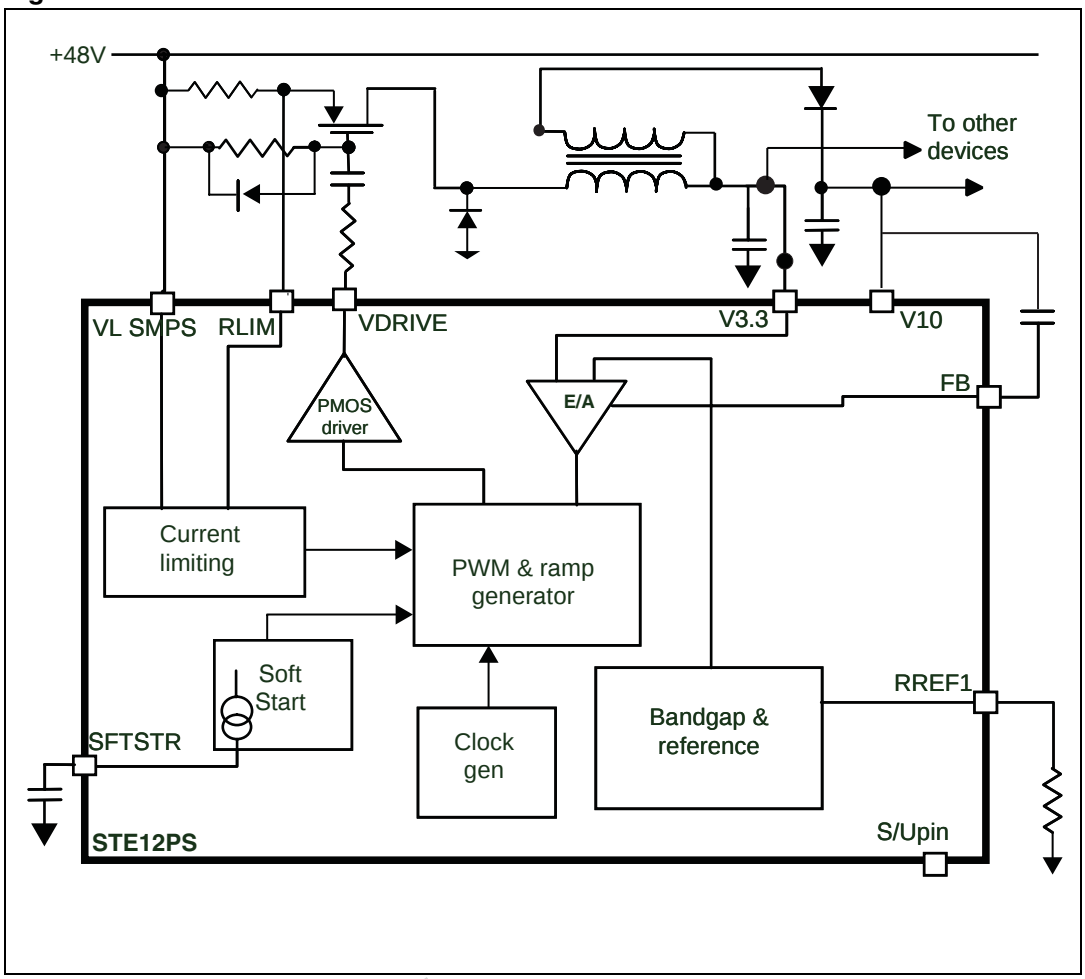

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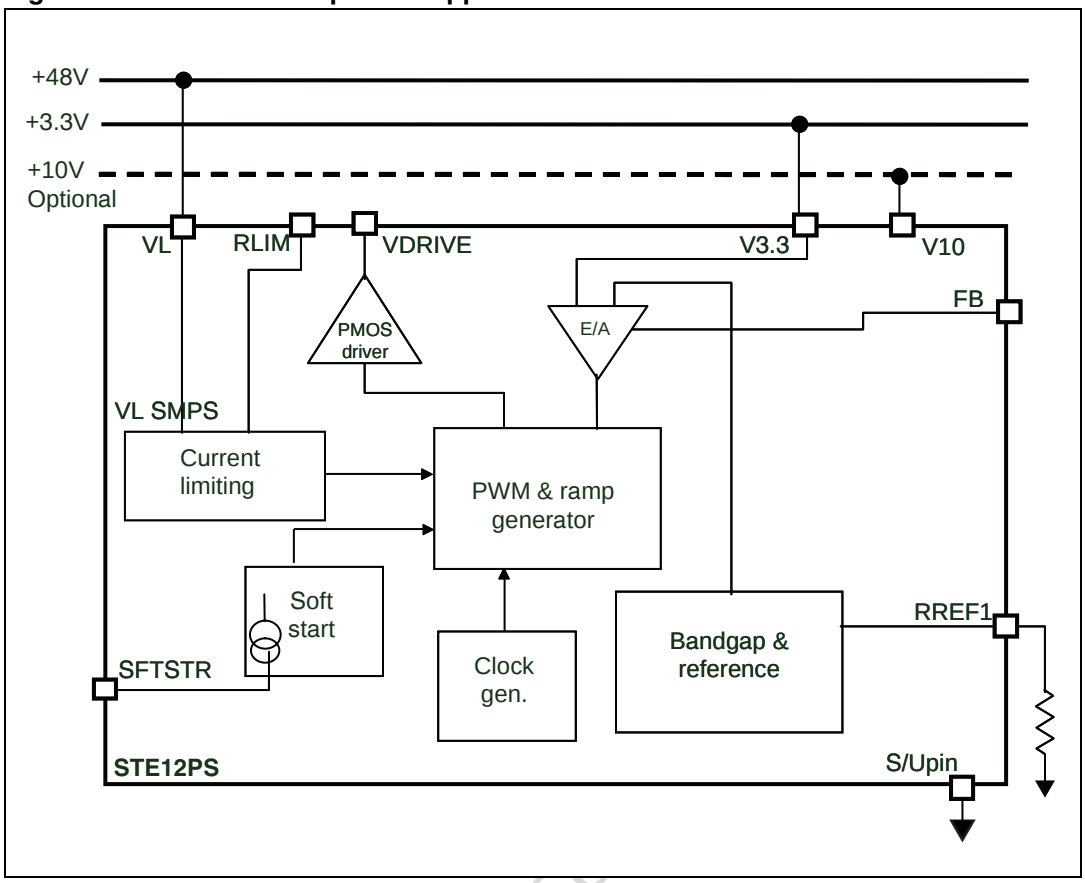
Figure 8. With external power supplies



3.6 6 MHz clock generator

Figure 10 on page 23, and *Figure 11* and *Figure 12 on page 24* show the three possible clock generation configurations:

a) with a 6 MHz crystal for a high precision clock,
b) with an external RC for low-cost applications,
c) with an external clock.

3.7 Smart-power mode

When this mode is enabled, the whole system is set to manage and deliver a limited amount of power to the channel. In Auto Mode, it is actually possible to set a maximum power budget for the device. When a PD is connected to a port, the STE12PS verifies the class and decides to power the line only if there's enough power available. It is also possible to set different priorities for the different channels. The device probes channels starting with those of highest priority. In case of shortage of available power, it is possible to disable the powering of newly detected ports of lower priority until the ones with a higher detected priority are serviced. If a channel exceeds its power class, that channel can be powered-down, and its power made available again. A 12-bit ADC is used to provide high-quality voltage and current measurements during the various phases of port detection,

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classification and powering. These measurements can be loaded into dedicated registers via the I^2C bus and are intended to be averaged over time in order to maximize PSSR and noise rejection as well as minimize 50 to 60 Hz interference.

3.8 Power boost mode - 30 W

3.8.1 Four channels in Auto mode

When this mode is activated, the device will run the classification extending the IEEE classes with an extra PD_Class boost as detailed in *Table 4*. If class boost is detected, an equivalent double port (parallel of two channels) is switched-on allowing up to 30W of power to be supplied. All the other IEEE classes behave as a standard port (powering on one channel only). *Table 5* below describes channel parallelism:

Table 5. Power boost mode: master/slave channel parallelism

Master Channel (MC)	Slave Channel (SC)
1	5
2	6
3	7
4	8

Channels in boost mode behave as master or slave according to the above table.

Detection and classification are performed only on the master ports. If a class 0 to 4 PD is detected, only MC is powered. Otherwise, if Boost Class is detected, both MC and the related SC are powered. Once powered, any fault condition (short circuit, over current, over power, PD disconnection) occurring either for MC or SC forces the reaction of both channels. All status and measurement information are stored in registers pertaining to the MC. Detection procedure is the same as the standard one while the classification phase is performed with 3 classification impulses (total classification time 70ms).

3.8.2 Six channels in Manual mode

To activate this mode the device should be set with CH_NUMx ="00" and the Manual mode must be selected. Under these conditions the output channels can be shorted together as illustrated in *Figure 9* and according to the following table.

Table 6. Power boost mode: master/slave channel parallelism

Master Channel (MC)	Slave Channel (SC)
1	5
2	6
3	7
4	8
9	12
10	11

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All the functions that manage the six "boost" channels must be implemented by an external microcontroller.

Figure 9. Power boost mode

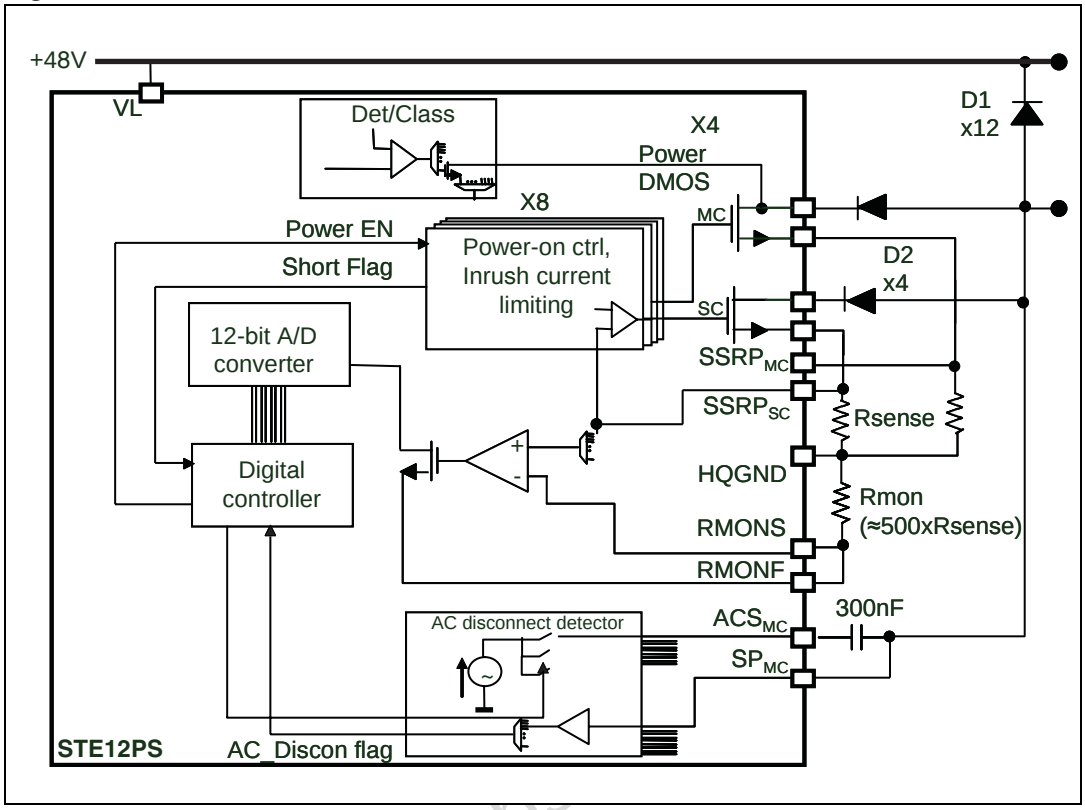


Figure 10. Crystal oscillator

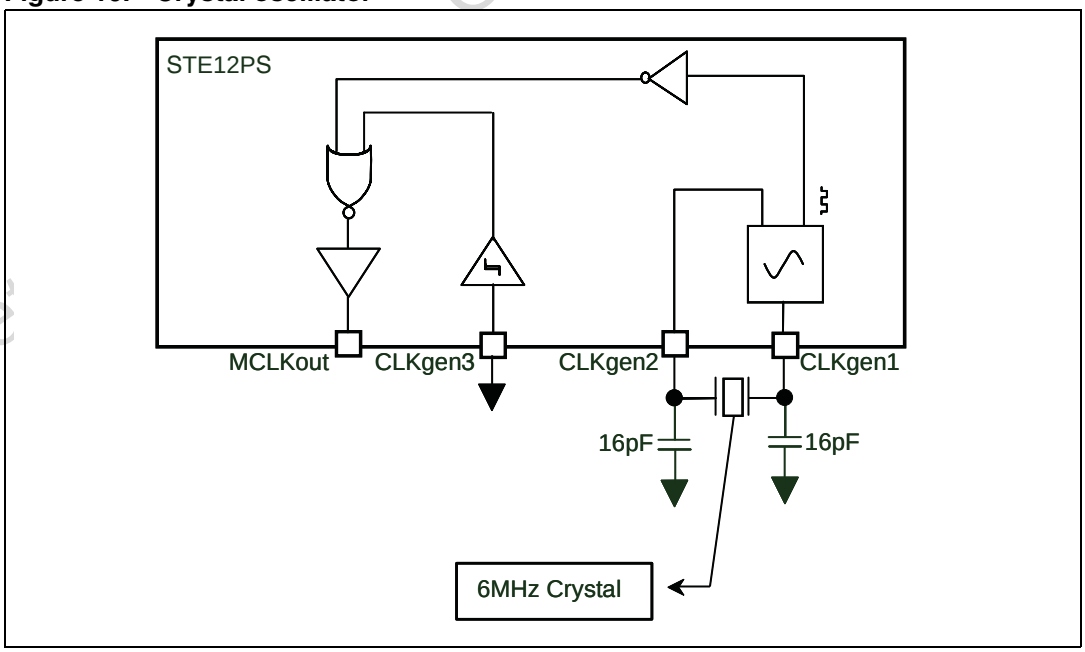


Figure 11. Low cost RC oscillator

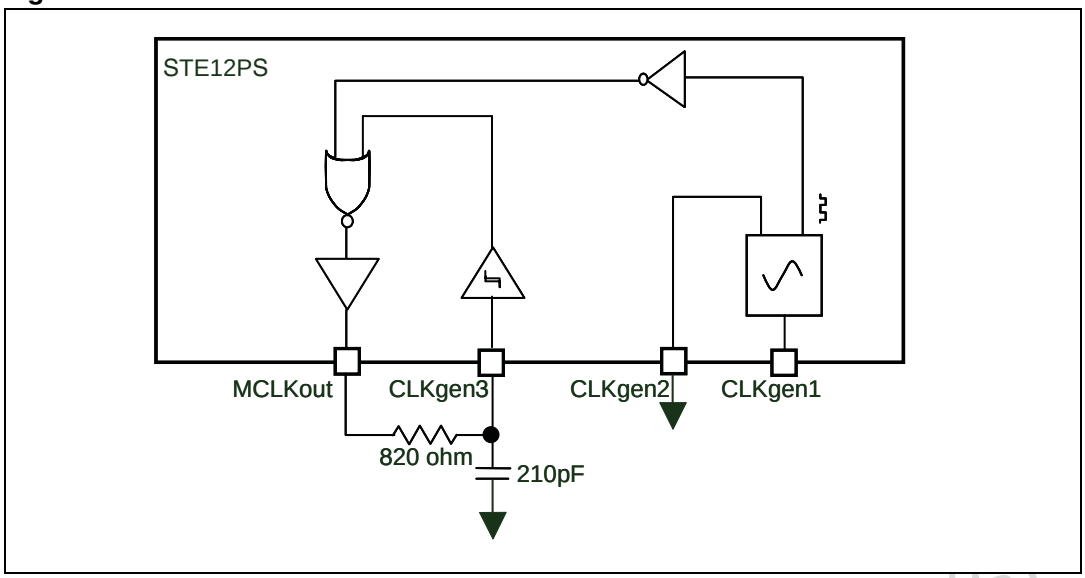
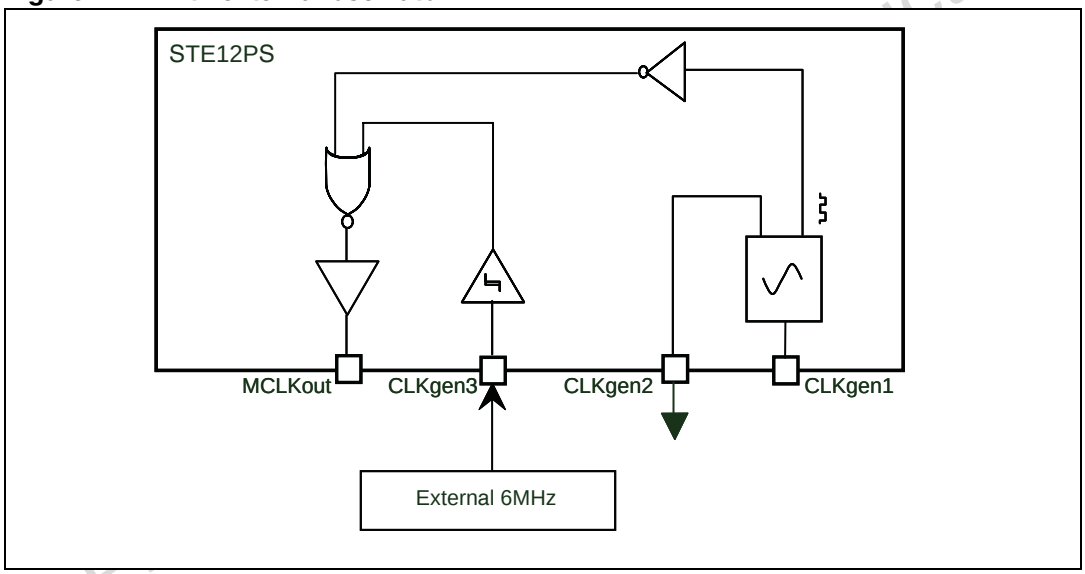


Figure 12. With external oscillator



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3.9 Measurement and parameter codings

Table 7 below lists codifications for the various parameters such as detection conductance or resistances, classification or monitoring currents, port voltages, port powers and power budgets.

Table 7. Measurement and parameter codings

Parameter	Description	Range	Step	Units	Number of steps
Idet	Detection current	0 to 1023	1	µA	1024
Gdet, Gdl, Gdh	Detection conductances	0 to 256	0.250	µS	1024
Rdet, Rdl, Rdh(1)	Detection residences	8 to 48.96	0.01	KΩ	4096
Iclass	Current classification	0 to 70	0.065064	mA	1024
Imon	Channel current during powering	0 to 1024	0.0312662	mA	32768
Vport	Battery voltage	0 to 70	0.27451	V	256
Pmeas	Channel power usage	0 to 35000	35.149	mW	1024

1. Rdet, Rdl and Rdh are the alternative to Gdet, Gdl and Gdh which are the default. If Rdet measures more than 500 kohms, the “open-circuit” flag is raised, that is set HIGH.

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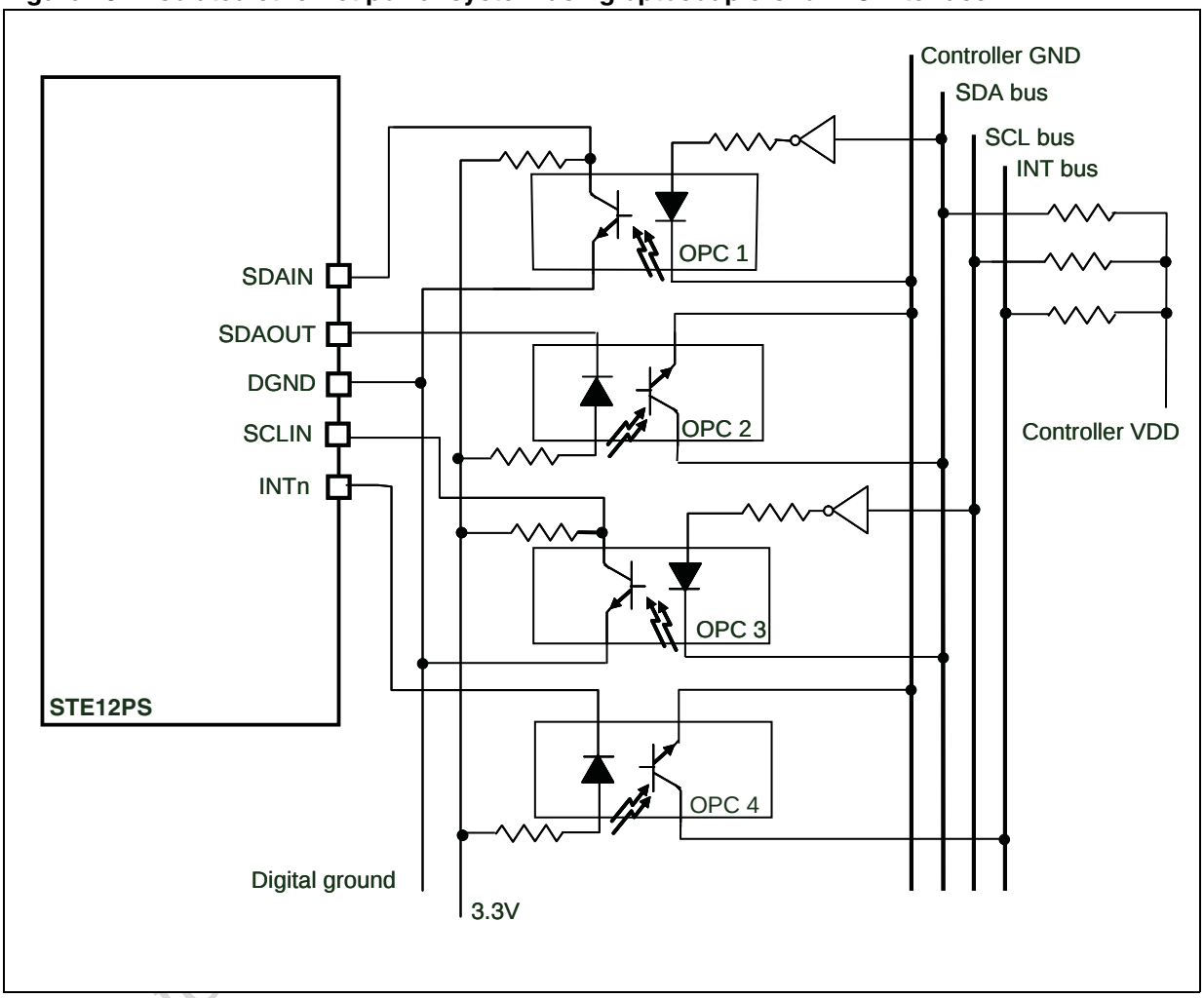
4 I2C interface

The STE12PS has an I2C interface to allow the access to the internal device registers. The external controller can be fully isolated from the Ethernet port thanks to an integrated 3.3V SMPS power source and using optocouplers on I2C bus.(*Figure 13*).

Figure 13. Isolated ethernet power system using optocouplers for I²C interface



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5 I²C slave protocol overview

The interface is capable of recognizing its own address (7 bit).

Data and addresses are transferred as 8-bit bytes, MSB first. The first byte following the start condition contains the device address.

A 9th clock pulse follows the 8 clock cycles of a byte transfer during which the receiver must pull LOW the SDA line to acknowledge the transfer.

The speed of the I²C interface is fixed at Fast I²C, that is, 100 to 400 kHz.

5.1 Functional description

As soon as a start condition is detected, the address is received from the SDA line and sent to a shift register; then it is compared with the internal address that is composed by the five pins for the five LSB and by a hardwired value equal to “01” for the other two bits.

In case of address mismatch the interface ignores it and waits for another Start condition.

If address is matched the interface generates an acknowledge pulse.

Following the address reception, POE digital controller receives bytes from the SDA line into the data register via an internal shift register or sends bytes from the data register to the SDA line through the internal shift register. After each byte reception an acknowledge pulse is generated by the controller.

A Stop condition generated by the host processor, after the last data byte is transferred, closes the communication.

5.2 Error cases

An error state is generated when Stop or Start conditions are detected during a byte transfer. If it is a Stop then the interface discards the data, releases the lines and waits for another Start condition. If it is a Start then the interface discards the data and waits for the next slave address on the bus.

5.3 Interrupts

Irq register bits indicate which signals can generate an interrupt. The register is read only and to clear the interrupt bits the corresponding source event has to be cleared. The logic OR condition of the interrupt bits causes the INTN pin assertion. The INTN assertion can be masked via the interrupt mask register *Irq_mask*.

5.4 I²C device address

The device is required to have an I²C address of: 01xxxxxb(A6 down to A0).

Pins I2C_ADDR[4:0] can be used to set the lower I²C address bits.

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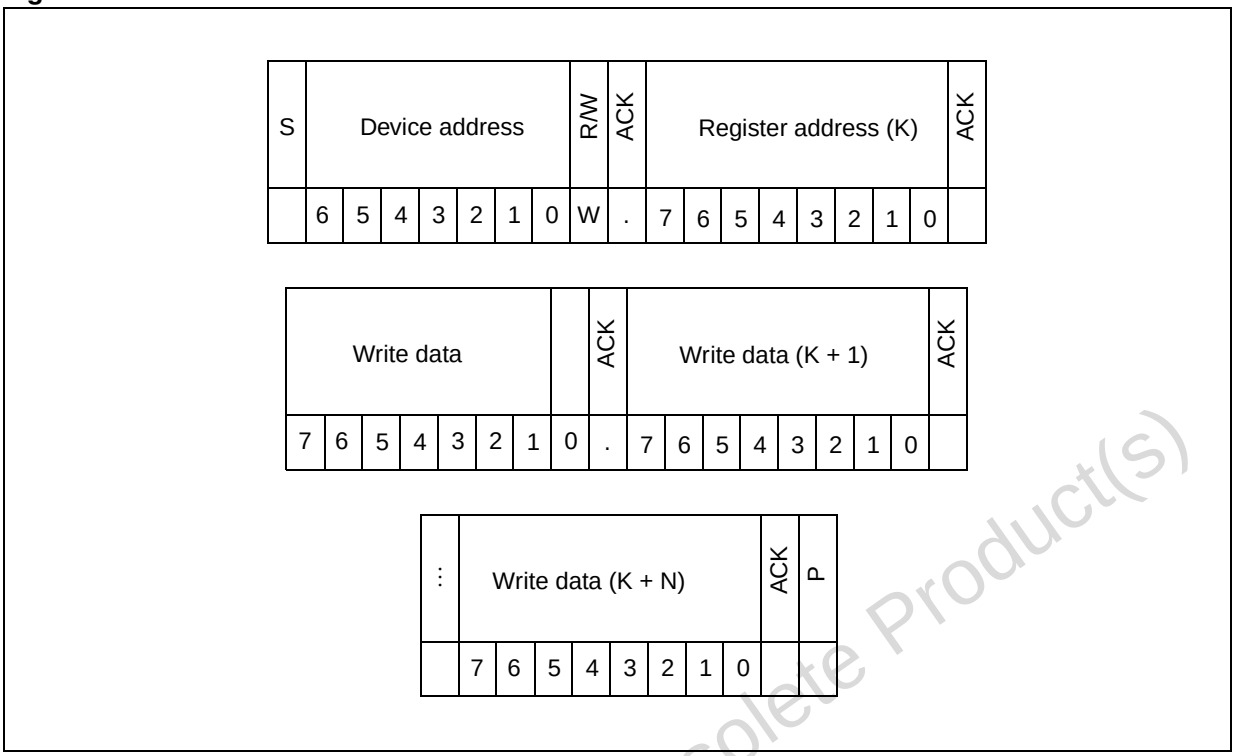
5.5 Register addressing: write command format

I²C write command format is shown in *Figure 14*.

Figure 14. Write command



The formatting bits shown in *Figure 14* are defined as follows:

- S - I²C start condition
- P - I²C stop condition
- ACK – acknowledge
- NACK - not acknowledge
- R/W - read/write

The device address is the value specified in I²C device address. The register address is an eight-bit value that is written into an internal Index Register. Each time a byte of data is written to, or read from the POE controller, the Index Register increments by one.

If the initial value written to the Index Register is K, then the byte immediately following the Register Address byte is written to the register with an address of K. The next byte is written to the register with the address of K+1, and so on.

An I²C write command can contain from 0 to 255 write data bytes. Write commands to an unknown register location are ignored by the interface.

As shown in *Figure 14*, bits are ordered with the most significant bit first.

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5.6 Register addressing: read command format

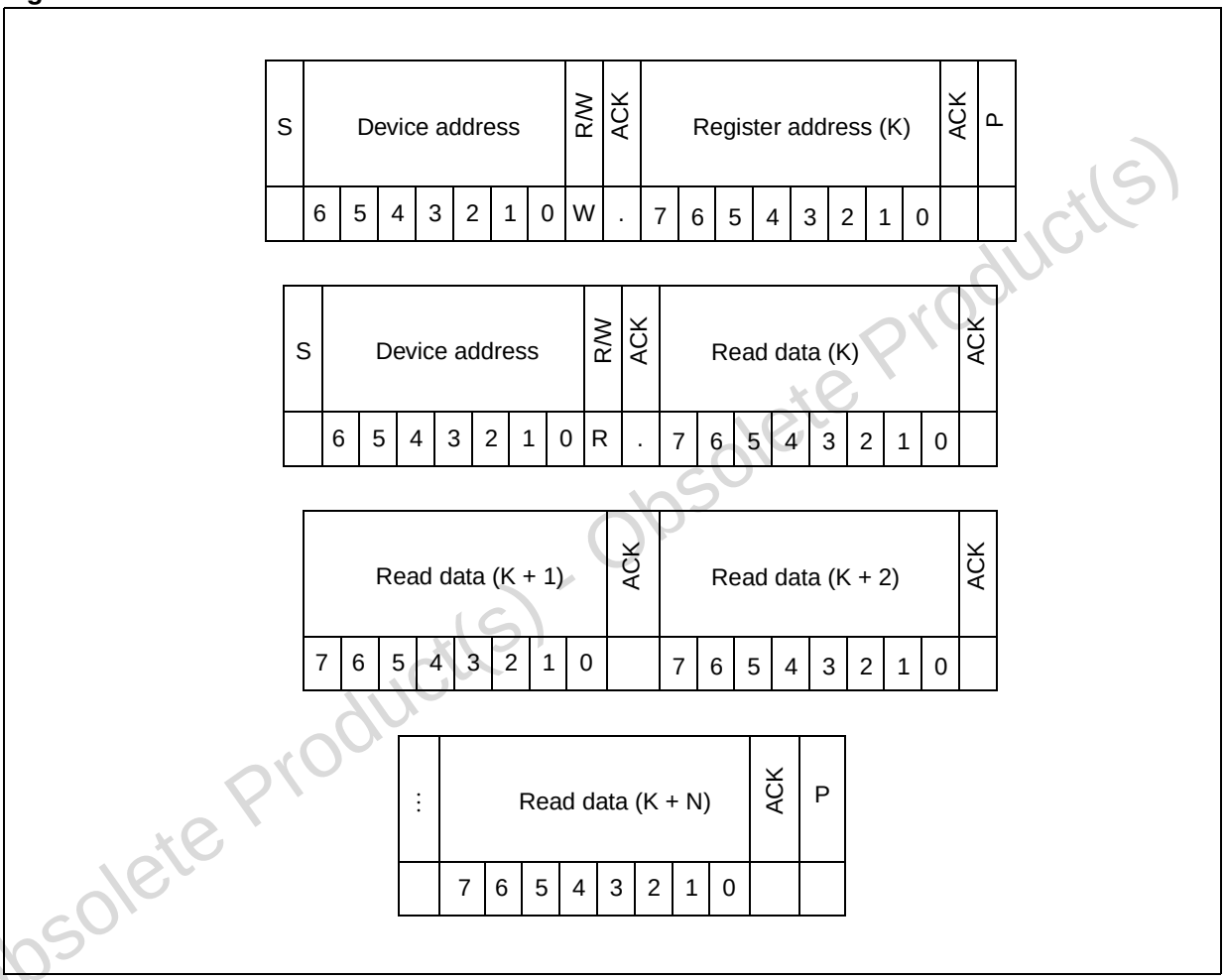
The general format of the read command is shown in *Figure 15*.

First part of the general read command consists of writing an address to the Index Register of the POE controller. If the Index Register already contains the address of the register to be read, as the result of a previous read or write command, then it is not necessary to write that address to the Index Register again.

After each byte is read from the POE controller, the Index Register is required to increment by one.

A read command can contain from 0 to 255 bytes.

Figure 15. Read command



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5.7 Parallel monitoring interface

In order to monitor the status of the different ports without the I^2C register addressing, a simple, output status interface has been implemented.

This digital interface is comprised of 9 output pins: CH_SEL[3:0], POK, OVLD, OVCUR, AC_DC_DISCON and DET_CLASS.

Bits *CH_SEL[3:0]* indicate the channel status flags (POK,..., DET_CLASS) that are currently notified, externally. CH_SEL is incremented every 60 MCLK clock cycles.

POK stands for Power OK. When HIGH, it indicates that the channel is currently powered-on in normal condition.

OVLD stands for OverLoad and indicates a faulty condition due to abnormal power dissipation (more than Pclass) of a powered channel.

OVCUR stands for OverCurrent, and it highlights a channel whose current has reached the power-on current limit of 425 mA (typ. value).

Bit *AC_DC_DISCON* goes HIGH when a powered channel fails in providing a correct MPS (maintain power signature). This typically happens when a PD is disconnected from the line.

DET_CLASS indicates a situation where a channel is not yet powered and whose “signature” is currently being probed.

Status flag notification is enabled by bit STATUS_FLAG_EN of the configuration register Global_cfg2. By default this bit is HIGH, that is, enabled.

This information is particularly useful in simple applications without a microprocessor or for testing purposes. Another use is to easily build-up an LED graphical interface showing runtime status of the various channels.

Obsolete Product(s) - Obsolete Product(s)

6 Electrical specifications and timings

Table 8. Absolute maximum ratings

Symbol	Parameter	Value	Units
V_L, $SMPSV_L$	Battery voltage	90	V
Vcc3,Vdd,Vdde	3.3V power supply	3.6	V
V10,Vdd10	10V power supply	12	V
Tj	Maximum junction temperature	150	°C

Table 9. Operating range

Symbol	Parameter	Value	Units
T_{opt}	Operating temperature range	-20 to +85	°C
V_L, $SMPSV_L$	Battery voltage	44 to 57	V
GNDs	Ground separation	-0.3	V
Vcc3, Vdd, Vdde	3.3V when externally supplied	3 to 3.6	V
V10, Vdd10	10V when externally supplied	9 to 11	V
I_{V10}, I_{Vdd10}	10V current sink (when externally supplied)	6.7 typ.	mA
I_{VI}	Battery current sink (when 10V is externally supplied)	0.4 typ.	mA
I_{VI}	Battery current sink (when 10V is self generated)	7.4 typ.	mA
$I_{v3.3}$	3.3V current sink (AUTO mode)	20 typ.	mA

Table 10. Thermal data

Symbol	Parameter	Value	Units
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient (natural convection)	25	°C/W

Table 11. ESD

Symbol	Parameter	Value	Units
HBM (Human Body Model)	All pins but pins Px_1-2 & Px_3	-2 to +2	kV
	All pins but pins FSRPx_1-2 & Px_3 (x = 1 to 12)		
	Pins Px_1-2 & Px_3	-250 to +250	V
	Pins FSRPx_1-2 & Px_3 (x = 1 to 12)		

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Table 11. ESD (continued)

Symbol	Parameter	Value	Units
CDM (Charge Device Model)	Corner pins	-750 to +750	V
	All pins but pins Px_1-2 & Px_3	-500 to +500	V
	All pins but pins FSRPx_1-2 & Px_3 (x = 1 to 12)		
	Pins Px_1-2 & Px_3	-250 to +250	V
	Pins FSRPx_1-2 & Px_3 (x = 1 to 12)		
MM (Machine Model)	All pins but pins Px_1-2 & Px_3	-200 to +200	V
	All pins but pins FSRPx_1-2 & Px_3 (x = 1 to 12)		
	Pins Px_1-2 & Px_3	-50 to +50	V
	Pins FSRPx_1-2 & Px_3 (x = 1 to 12)		

Table 12. Electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
Detection						
Vdl	Detection voltage LOW level	3.7	4	4.3	V	Between port terminals
Vdh	Detection voltage HIGH level	7.4	8	8.6	V	Between port terminals
Tds	Transient time between Vdl and Vdh	300			µs	Adjustable with external capacitor Cdetslow
Gdl	Conductance signature, lower limit (Software programmable)	25		50	µmhos	Software programmable)
Gdh	Conductance signature, upper limit (Software programmable)	41		82	µmhos	Software programmable
Rdl	Resistance signature, lower limit (Software programmable)	12		24	kΩ	Software programmable, to be used as an alternative to Gdh
Rdh	Resistance signature, upper limit (Software programmable)	20		40	kΩ	Software programmable, to be used as an alternative to Gdl
Idlim	Current limit during detection			1.1	mA	
Tdet	Detection time		50		ms	12-port configuration, one channel at a time
Tdetd	Detection delay time (from PD insertion to end of detection phase)			852	ms	Maximum delay for 12-port configuration
Tdbo	Back-off time (midspan mode)	2			sec.	Back off time in case of failed PD detection, avoided if Rdet > 500kΩ or Gdet < 2µmhos
Ted	Error delay time	750			ms	

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Table 12. Electrical characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
Classification						
Vcl	Classification probing voltage	15.9	17	18.1	V	Between port terminals
Icllim	Current limit during classification	55		70	mA	
Tcl	Classification time		15		ms	One channel at a time, classification measurement has to be considered as sampled and integrated over this time interval.
Ithcl0	Class0-1 current threshold	5.5	6.5	7.5	mA	
Ithcl1	Class1-2 current threshold	13.5	14.5	15.5	mA	
Ithcl2	Class2-3 current threshold	21.8	23	24.2	mA	
Ithcl3	Class3-4 current threshold	31.5	33	34.5	mA	
Ithcl4	Class4-0 current threshold	45.5	46.5	47.5	mA	
Powering						
Pall	Maximum power per channel			15.4	W	See also classification paragraph (doubled in case of Boost configuration)
Iinrush	Output current startup mode	400		450	mA	Inrush current soft start
Imin	Power off current	5		10	mA	Disconnect for t > TPMDO (DC disconnection method)
Acfre	AC disconnection sinusoidal generator		50		Hz	Frequency spread related to clock stability
Vacd	AC generator open line voltage		2.5		V_{pp}	
Zac	AC impedance needed to maintain power		100		kΩ	
Tmpdo	PD power maintenance request drop out time limit (Software programmable)	300		400	ms	The STE12PS will not remove power if the PD maintenance signal is absent for less than 300ms duration. If an absence of power maintenance signal has been detected, the STE12PS shall remove power within 400ms max(1)
Icut	Over load current	Pall/Vport		400	mA	After time duration of Tovld the STE12PS will disconnect the power from the port.

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Table 12. Electrical characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
Tovld	Over load time limit (Software programmable)	50	65	75	ms	In fault condition for Tovld, the STE12PS will disconnect the port. (1)
Tshort	Short-circuit/inrush time limit (Software programmable)	50	65	75	ms	In fault condition for Tshort, the STE12PS will disconnect the port.(1)
I_{lim}	Output load current under short - circuit condition	400		450	mA	Max. value of port current during short circuit condition. Power will be disconnected from the port within Tshort
Tinrush	Rise time of Vport time limit			75	ms	Expired Tinrush if the channel is still in limiting condition it is considered in fault
Toff	Turn off time			100	ms	From VPort to 2.8V DC
Ron	Internal MOSFET resistance in ON mode			1	ohms	
VsLR	3V range in generator mode	3	3.3	3.6	V	
V10 int	10V range internally generated		8.7		V	
Digital						
Fclk	Clock frequency		6		MHz	
V_{IH}	Input HIGH level voltage	2			V	@ V_{DD} = 3.3V
V_{IL}	Input LOW level voltage		0.8		V	@ V_{DD} = 3.3V
I_{IH}	Input High current			30	µA	
I_{IL}	Input LOW current			10	µA	

1. See also timer programmability

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7 Ball coordinates

Figure 16. Balls top view layout (as viewed through package)

VIEW THROUGH PACKAGE

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	CH_SEL0	CH_SEL1	OVLD	SCL	INTN	SDAIN	SDAOUT	CH_NUM1	CH_NUM0	AGND	IDET_HVLV	I_REF	Vbatref	AGND	RESETN	PORn	vdde	gnde	vdd	POWER_EN0	POWER_EN1	POWER_EN2
B	CH_SEL2	CH_SEL3	AC_DC_DISCON	DET_CLASS	I2C_ADDR0	I2C_ADDR1	I2C_ADDR2	TEST_MODE1	TEST_MODE0	AGND	AGND	IMON_HVLV	Vbatmon	AGND	vdde	vdde	gnde	vdd	gnd	POWER_EN3	POWER_EN4	POWER_EN5
C	vdd10	V10	V3_3	POK	OVCUR	I2C_ADDR3	I2C_ADDR4	A_BN_SEL	AUTO_START	SCAN_EN	AGND	AGND	AGND	AGND	vdde	gnde	vdd	gnd	gnd	POWER_EN6	POWER_EN7	POWER_EN8
D	SMPSGND	SFTstr	Acin	Acout	gnd	CLK_GEN1	CLK_GEN2	MCLKout	CLK_GEN3	VDDA	gnd	gnd	gnd	gnde	gnde	vdd	vdd	gnd	gnd	POWER_EN9	POWER_EN10	POWER_EN11
E	S/U	NC	RREF	gnd															gnd	CdetSlow	NC	NC
F	NC	NC	FB	gnd															RMONS	RMONF	NC	P8_1-2
G	SenseR	NC	SenseProg Pin0	DGND															HQgnd	FSRp8_1-2	NC	P8_3
H	Vdrive	NC	SenseProg Pin1	DGND															ACS8	FSRp8_3	NC	SP8
J	SMPSVL	NC	ACS5	GND					gnd	gnd	gnd	gnd	gnd	gnd					SSRp8	ACS4	NC	NC
K	VL	NC	SSRp5	GND					GND	GND	GND	GND	GND	GND					SSRp4	FSRp4_1-2	NC	P4_1-2
L	NC	NC	FSRp5_1-2	GND					GND	GND	GND	GND	GND	GND					GND	FSRp4_3	NC	P4_3
M	P5_1-2	NC	FSRp5_3	GND					GND	GND	GND	GND	GND	GND					GND	ACS12	NC	SP4
N	P5_3	NC	ACS1	GND					GND	GND	GND	GND	GND	GND					GND	SSRp12	NC	NC
P	SP5	NC	SSRp1	GND					GND	GND	GND	GND	GND	GND					GND	FSRp12_1-2	NC	P12_1-2
R	NC	NC	FSRp1_1-2	GND															GND	FSRp12_3	NC	P12_3
T	P1_1-2	NC	FSRp1_3	GND															GND	ACS7	NC	SP12
U	P1_3	NC	ACS9	GND															GND	SSRp7	NC	NC
V	SP1	NC	SSRp9	GND															GND	FSRp7_1-2	NC	P7_1-2
W	NC	NC	FSRp9_1-2	GND	SSRp6	GND	GND	SSRp2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	SSRp3	FSRp7_3	NC	P7_3
Y	P9_1-2	NC	FSRp9_3	ACS6	FSRp6_1-2	FSRp6_3	ACS2	FSRp2_1-2	FSRp2_3	ACS10	SSRp10	FSRp10_1-2	FSRp10_3	FSRp11_1-2	FSRp11_3	SSRp11	ACS11	FSRp3_3	FSRp3_1-2	ACS3	NC	SP7
AA	P9_3	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
AB	SP9	NC	P6_1-2	P6_3	SP6	NC	P2_1-2	P2_3	SP2	NC	P10_1-2	P10_3	SP10	NC	SP11	P11_3	P11_1-2	NC	SP3	P3_3	P3_1-2	NC

Table 13. Pad coordinates

Column	Row	Pin name
1	A	CH_SEL0
1	AA	P9_3
1	AB	SP9
1	B	CH_SEL2
1	C	vdd10
1	D	SMPSGND
1	E	S/U
1	F	NC
1	G	RSENSE
1	H	Vdrive
1	J	SMPSVL
1	K	VL
1	L	NC
1	M	P5_1-2
1	N	P5_3
1	P	SP5
1	R	NC
1	T	P1_1-2
1	U	P1_3
1	V	SP1
1	W	NC
1	Y	P9_1-2
2	A	CH_SEL1
2	B	CH_SEL3
2	C	V10
2	D	SFTstr
2	E	NC
2	F	NC
2	G	NC
2	H	NC
2	J	NC
2	K	NC
2	L	NC
2	M	NC
2	N	NC

Column	Row	Pin name
2	P	NC
3	M	FSRp5_3
3	N	ACS1
2	R	NC
2	T	NC
2	U	NC
2	V	NC
2	W	NC
2	Y	NC
2	AA	NC
2	AB	NC
3	A	OVLD
3	B	AC_DC_DISCON
3	C	V3_3
3	D	ACin
3	E	RREF
3	F	FB
3	G	SenseProgPin0
3	H	SenseProgPin1
3	J	ACS5
3	K	SSRp5
3	L	FSRp5_1-2
3	P	SSRp1
3	R	FSRp1_1-2
3	T	FSRp1_3
3	U	ACS9
3	V	SSRp9
3	W	FSRp9_1-2
3	Y	FSRp9_3
3	AA	NC
3	AB	P6_1-2
4	A	SCL
4	B	DET_CLASS
4	C	POK
4	D	ACout

Obsolete Product(s) - Obsolete Product(s)

Table 13. Pad coordinates (continued)

Column	Row	Pin name
4	AA	NC
4	AB	P6_3
4	E	gnd
4	F	gnd
4	G	DGND
4	H	DGND
4	J	GND
4	K	GND
4	L	GND
4	M	GND
4	N	GND
4	P	GND
4	R	GND
4	T	GND
4	U	GND
4	V	GND
4	W	GND
4	Y	ACS6
5	A	INTN
5	AA	NC
5	AB	SP6
5	B	I2C_ADDR0
5	C	OVCUR
5	D	gnd
5	W	SSRp6
5	Y	FSRp6_1-2
6	A	SDAIN
6	AA	NC
6	AB	NC
6	B	I2C_ADDR1
6	C	I2C_ADDR3
6	D	CLK_GEN1
6	W	GND
6	Y	FSRp6_3
7	A	SDAOUT

Column	Row	Pin name
9	B	TEST_MODE0
9	C	AUTO_START
7	B	I2C_ADDR2
7	C	I2C_ADDR4
7	D	CLK_GEN2
7	W	GND
7	Y	ACS2
7	AA	NC
7	AB	P2_1-2
8	A	CH_NUM1
8	B	TEST_MODE1
8	C	A_BN_SEL
8	D	MCLKout
8	W	SSRp2
8	Y	FSRp2_1-2
8	AA	NC
8	AB	P2_3
9	A	CH_NUM0
9	D	CLK_GEN3
9	P	GND
9	W	GND
9	J	gnd
9	K	GND
9	L	GND
9	M	GND
9	N	GND
9	Y	FSRp2_3
10	D	VDDA
10	J	gnd
9	AA	NC
9	AB	SP2
10	A	AGND
10	B	AGND
10	C	SCAN_EN
10	K	GND

Obsolete Product(s) - Obsolete Product(s)

Table 13. Pad coordinates (continued)

Column	Row	Pin name
10	AA	NC
10	AB	NC
10	L	GND
10	M	GND
10	N	GND
10	P	GND
10	W	GND
10	Y	ACS10
11	A	IDET_HVLV
11	AA	NC
11	AB	P10_1-2
11	B	AGND
11	C	AGND
11	D	gnd
11	J	gnd
11	K	GND
11	L	GND
11	M	GND
11	N	GND
11	P	GND
11	W	GND
11	Y	SSRp10
12	A	I_REF
12	AA	NC
12	B	IMON_HVLV
12	C	AGND
12	D	gnd
12	J	gnd
12	K	GND
12	L	GND
12	M	GND
12	N	GND
12	P	GND
12	W	GND
12	Y	FSRp10_1-2
13	K	GND
13	L	GND
12	AB	P10_3
13	A	Vbatref
13	B	Vbatmon
13	C	AGND
13	D	GND
13	J	GND
13	M	GND
14	K	GND
14	L	GND
13	N	GND
13	P	GND
13	W	GND
13	Y	FSRp10_3
13	AA	NC
13	AB	SP10
14	A	AGND
14	B	AGND
14	C	AGND
14	D	gnde
14	J	gnd
14	M	GND
15	Y	FSRp11_3
14	N	GND
14	P	GND
14	W	GND
14	Y	FSRp11_1-2
14	AA	NC
14	AB	NC
15	A	RESETN
15	B	vdde
15	C	vdde
15	D	gnde
15	W	GND

Obsolete Product(s) - Obsolete Product(s)

Table 13. Pad coordinates (continued)

Column	Row	Pin name
15	AA	NC
15	AB	SP11
16	A	PORn
16	AA	NC
16	AB	P11_3
16	B	vdde
16	C	gnde
16	D	vdd
16	W	GND
16	Y	SSRp11
17	A	vdde
17	AA	NC
17	AB	P11_1-2
17	B	gnde
17	C	vdd
17	D	vdd
17	W	GND
17	Y	ACS11
18	A	gnde
18	AA	NC
18	AB	NC
18	B	vdd
18	C	gnd
18	D	gnd
18	W	GND
18	Y	FSRp3_3
19	A	vdd
19	B	gnd
19	C	gnd
19	D	gnd
19	E	gnd
19	F	RMONS
19	G	HQgnd
19	H	ACS8
19	J	SSRp8
19	K	SSRp4
19	L	GND
19	M	GND
19	V	GND
19	W	SSRp3
19	N	GND
19	P	GND
19	R	GND
19	T	GND
19	U	GND
19	Y	FSRp3_1-2
20	D	POWER_EN9
20	E	CdetSlow
19	AA	NC
19	AB	SP3
20	A	POWER_EN0
20	B	POWER_EN3
20	C	POWER_EN6
20	F	RMONF
20	M	ACS12
20	N	SSRp12
20	G	FSRp8_1-2
20	H	FSRp8_3
20	J	ACS4
20	K	FSRp4_1-2
20	L	FSRp4_3
20	P	FSRp12_1-2
20	R	FSRp12_3
20	T	ACS7
20	U	SSRp7
20	V	FSRp7_1-2
20	W	FSRp7_3
20	Y	ACS3
20	AA	NC
20	AB	P3_3

Obsolete Product(s) - Obsolete Product(s)

Table 13. Pad coordinates (continued)

Column	Row	Pin name
21	A	POWER_EN1
21	AB	P3_1-2
21	B	POWER_EN4
21	C	POWER_EN7
21	D	POWER_EN10
21	E	NC
21	F	NC
21	G	NC
21	H	NC
21	J	NC
21	K	NC
21	L	NC
21	M	NC
21	N	NC
21	P	NC
21	R	NC
21	T	NC
21	U	NC
21	V	NC
21	W	NC
21	Y	NC
22	A	POWER_EN2
22	B	POWER_EN5
22	C	POWER_EN8
22	D	POWER_EN11
22	E	NC
22	F	P8_1-2
22	G	P8_3
22	H	SP8
22	J	NC
22	K	P4_1-2
22	L	P4_3
22	M	SP4
22	N	NC
22	P	P12_1-2
22	R	P12_3
22	T	SP12
22	U	NC
22	V	P7_1-2
22	W	P7_3
22	Y	SP7
22	AA	NC
22	AB	NC

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8 Package information - mechanical data

In order to meet environmental requirements, ST Microelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST Microelectronics trademark. ECOPACK specifications are available at: www.st.com.

Package code: TN

JEDEC/EIAJ reference number: JEDEC standard No. 95-1, section 14 (ball grid array package design guide)

Table 14. Package dimensions

Ref.	Databook (mm)			Drawing (mm)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		1.720		1.620	1.720	1.820
A1	0.270			0.350	0.400	0.450
A2		1.320			1.320	
b	0.450	0.500	0.550	0.450	0.500	0.550
D	22.800	23.000	23.200	22.900	23.000	23.100
D1		21.000				21.000
E	22.800	23.000	23.200	22.900	23.000	23.100
E1		21.000				21.000
e	0.950	1.000	1.050	0.950	1.000	1.050
f	0.875	1.000	1.125	0.875	1.000	1.125
ddd			0.200			0.200

Note: 1 Maximum mounted height, dimension A, is 1.77mm based on a 0.35mm ball pad diameter. Solder paste is 0.15mm thick and 0.35mm in diameter.

2 PBGA stands for Plastic Ball Grid Array.

3 The terminal A1 corner must be on the top surface by using a corner chamfer, ink, metallized markings or some other feature of the package body or internal heatslug.

4 A distinguishing feature is allowed on the bottom surface of the package to identify terminal the A1 corner.

5 Exact shape of each corner is optional.

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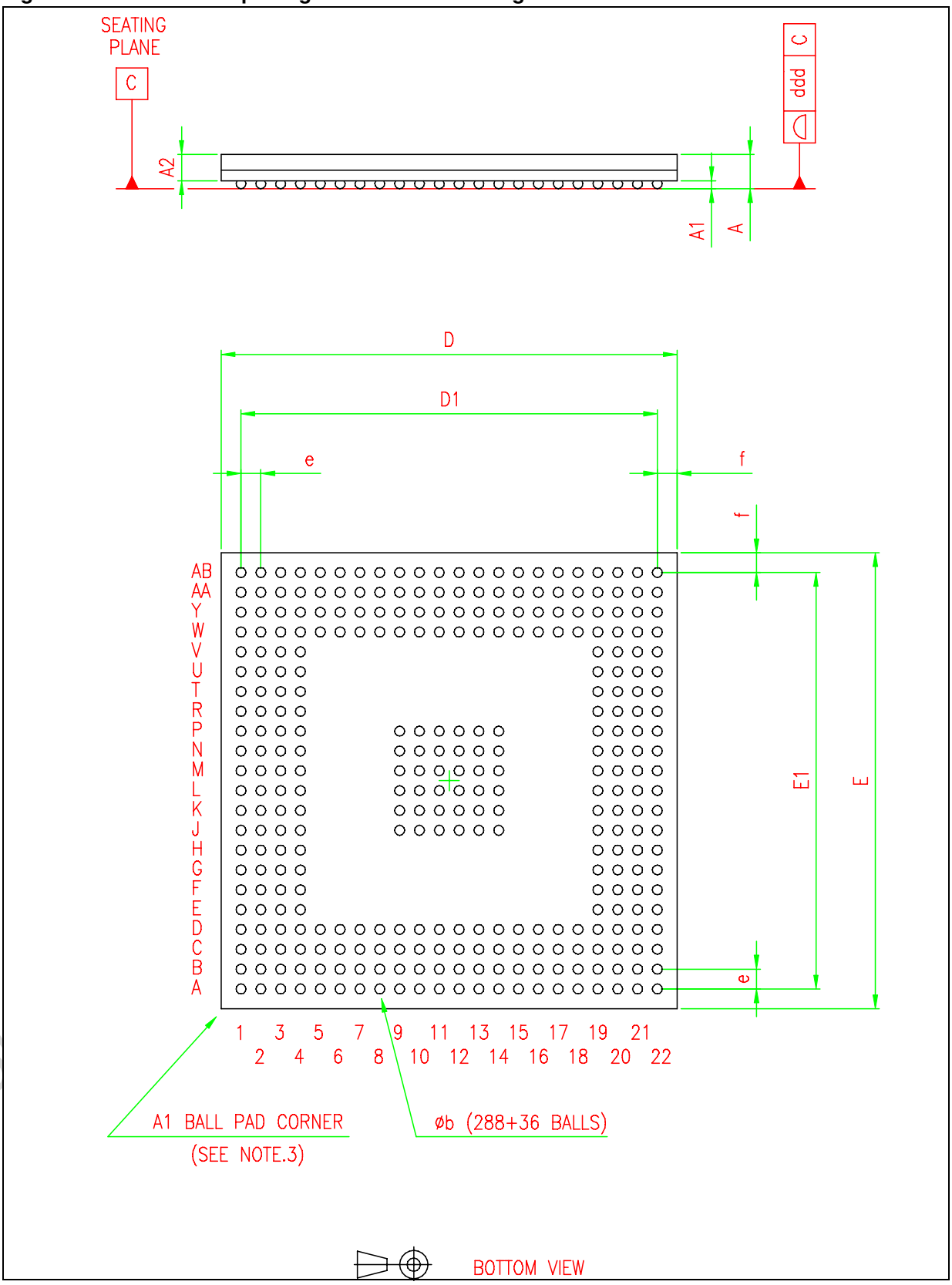
Figure 17. PBGA23x23 package mechanical drawing



9 Ordering information

Table 15. Order codes

Part number	Temperature range	Package
E-STE12PS(1)	-40°C to +85 °C	PBGA (23mm x 23mm x 1.82mm)

1. E-: ECOPACK®

10 Revision history

Table 16. Document revision history

Date	Revision	Changes
10-Nov-2006	1	Initial release
13-Dec-2006	2	Updated the number of 30W boosted ports to be four or six instead of four previously (cover page and *Section 3.8*).
17-Aug-2007	3	Added *Table 11: ESD* in *Chapter 6*.

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