
Evaluation board using PD55008L-E for UHF mobile radio

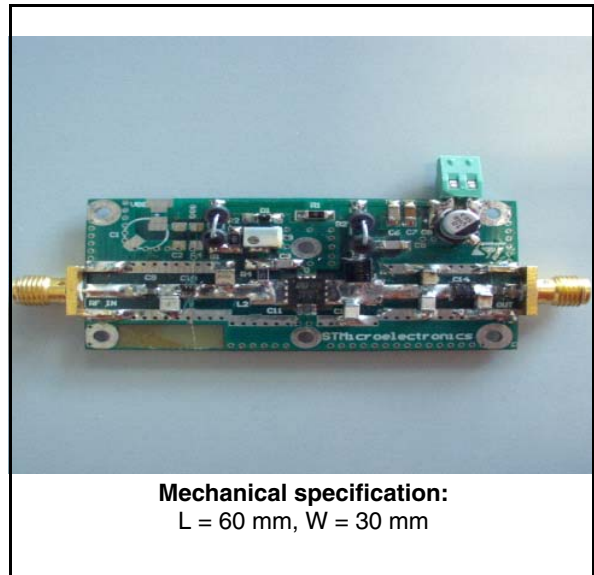
Features

- Excellent thermal stability
- Frequency: 400 - 470 MHz
- Supply voltage: 12.5 V
- Output power: 8 W
- Power gain: 16.7 ± 2.0 dB
- Efficiency: 49 % - 61 %
- Load mismatch: 20:1
- Beo free amplifier

Description

The DB-55008L-470 is an evaluation board using PD55008L-E LDMOS transistor and designed for UHF analog and digital mobile radios.

For additional informations on PD55008L-E, please refer to its datasheet

**Table 1. Device summary**

Part number
DB-55008L-470

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1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	16	V
I_D	Drain current	1.6	A
T_{CASE}	Operating case temperature	-20 to +85	°C
T_A	Max. ambient temperature	+55	°C

2 Electrical characteristics

$T_A = +25\text{ °C}$, $V_{DD} = 12.5\text{ V}$, $I_{dq} = 100\text{ mA}$

Table 3. Electrical specification

Symbol	Test conditions	Min	Typ	Max	Unit
Freq	Frequency range	400		470	MHz
P_{OUT}		7	8		W
Gain	@ $P_{OUT} = 8\text{ W}$		16.7 ± 2.0		dB
ND	@ $P_{OUT} = 8\text{ W}$		49 - 61		%
H2	2 ND Harmonic @ $P_{OUT} = 8\text{ W}$		-43 / -70		dBc
H3	3 RD Harmonic @ $P_{OUT} = 8\text{ W}$		-49 / -72		dBc
VSWR	Load mismatch all phases @ $P_{OUT} = 8\text{ W}$		20:1		

3 Impedance

Table 4. Impedance data

F(MHz)	Z_{GS}	Z_{DL}
380	2.6 + J1.4	2.9 + J2.1
400	2.5 + J2.1	3.3 + J2.5
420	2.5 + J2.8	3.8 + J2.9
440	2.6 + J3.5	4.3 + J3.0
460	2.8 + J4.1	4.8 + J3.1
480	3.1 + J4.6	5.3 + J3.0

4 Typical performances

Figure 1. Pout vs pin and frequency

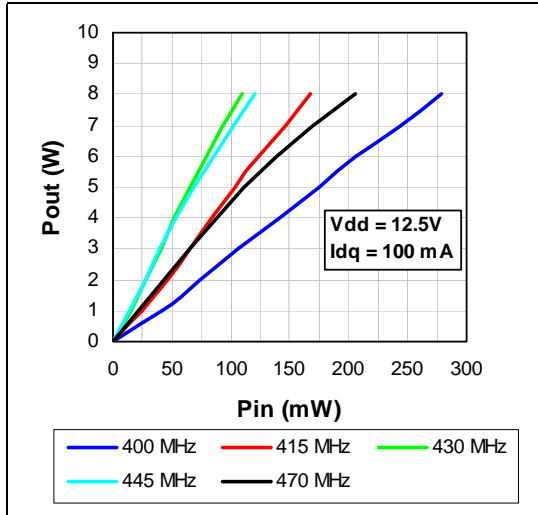


Figure 2. Efficiency vs pout and frequency

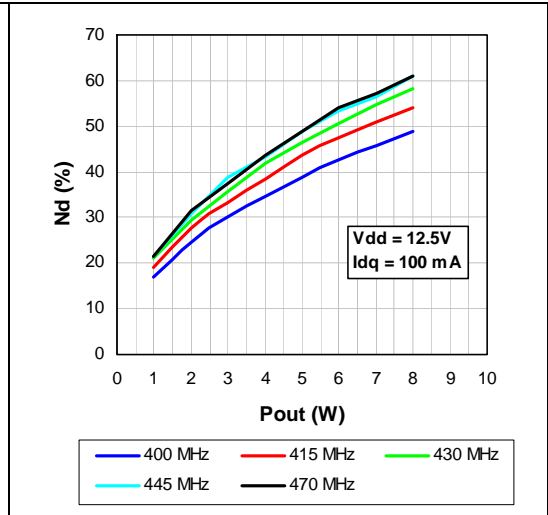


Figure 3. Gain and efficiency vs frequency

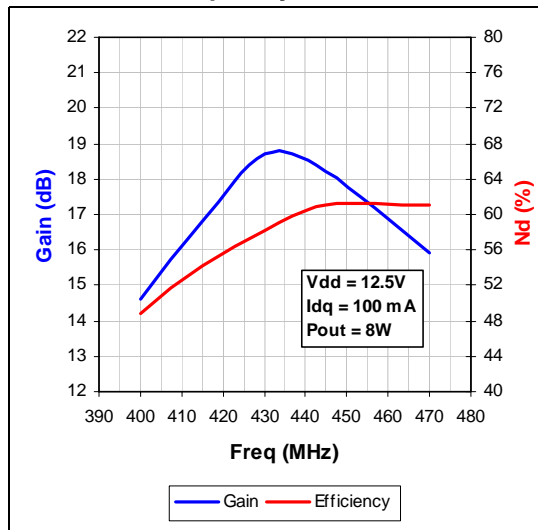


Figure 4. Input return loss vs frequency

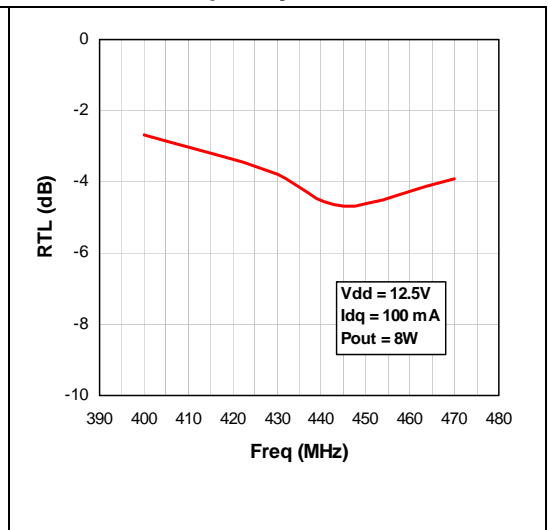


Figure 5. Harmonics vs frequency

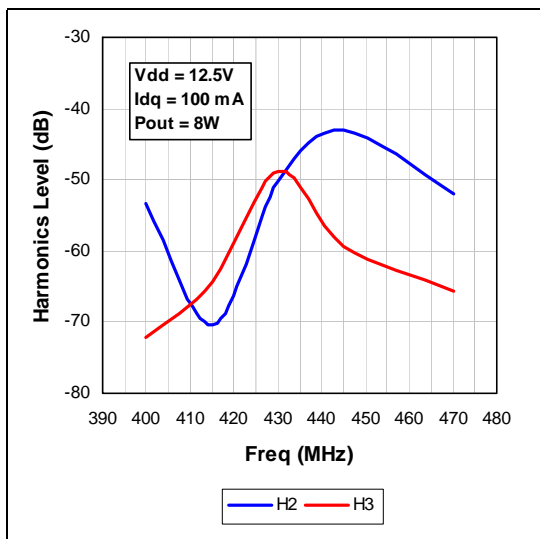
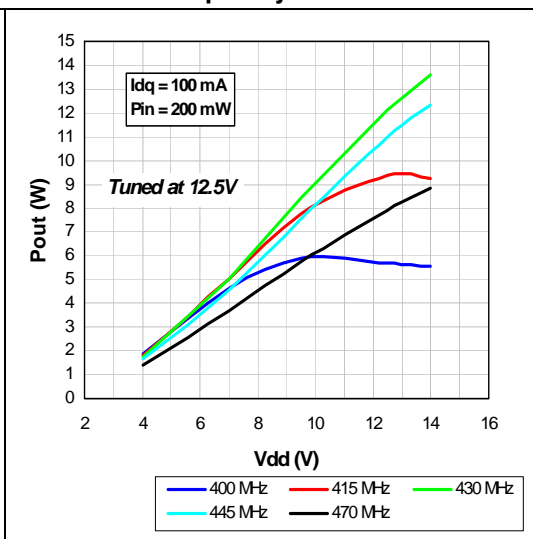


Figure 6. Pout vs drain voltage and frequency



5 Circuit layout and parts list

Figure 7. Circuit layout

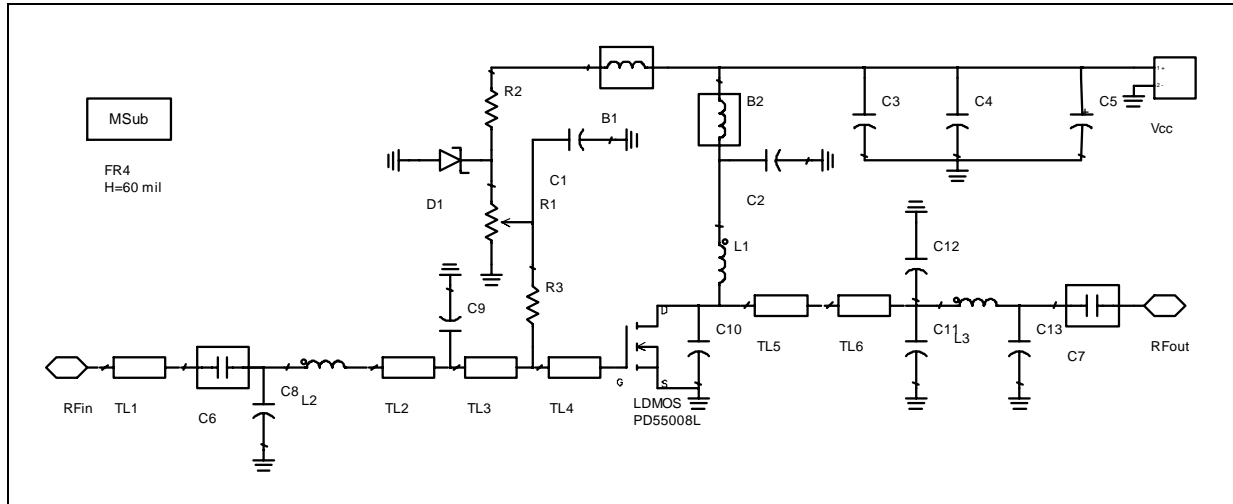


Table 5. Circuit parts list

Component ID	Description	Value	Case size	Manufacturer	Part code
B1	Ferrite Bead			Panasonic	EXCELDRC35C
B2	Ferrite Bead			Panasonic	EXCELDRC35C
C1, C2	Capacitor	120 pF	1206	ATC	GRM42-6C0G121J50
C3	Capacitor	1 nF	1206	Murata	GRM42-6C0G102J50
C4	Capacitor	10 nF	1206	Murata	GRM42-6X7R104K50
C5	Capacitor	10 uF	SMT	Panasonic	EEVHB1V100P
C6, C7	Capacitor	300 pF	100B	Murata	GRM42-6C0G301J50
C8	Capacitor	18 pF	100B	ATC	180
C9	Capacitor	33 pF	100B	ATC	330
C10	Capacitor	39 pF	100B	ATC	390
C11	Capacitor	15 pF	100B	ATC	150
C12	Capacitor	33 pF	100B	ATC	330
C13	Capacitor	11 pF	100B	ATC	110
D1	Zener diode	NC			
L1	Inductor	35.5 nH		Coilcraft	B09T
L2	Inductor	8 nH		Coilcraft	A03T
R1	Potentiometer	10 KΩ		Bourns electronics	103
R2	Resistor	1 KΩ	1206	Tyco electronics	01623440-1
R3	Resistor	15 Ω	1206	Tyco electronics	150
TL1	Transmission line	W=2.87mm	L=8.6 mm		

Table 5. Circuit parts list (continued)

Component ID	Description	Value	Case size	Manufacturer	Part code
TL2	Transmission line	W=2.87mm	L=3.1 mm		
TL3	Transmission line	W=2.87mm	L=2.8 mm		
TL4	Transmission line	W=4.9mm	L=5.4 mm		
TL5	Transmission line	W=4.9mm	L=5.4 mm		
TL6	Transmission line	W=2.87mm	L=8.6 mm		
PD55008L-E	LDMOS			STMicroelectronics	PD55008L-E
Board	FR4 THk = 0.060" 2OZ Cu both sides				

Figure 8. Test circuit photomaster

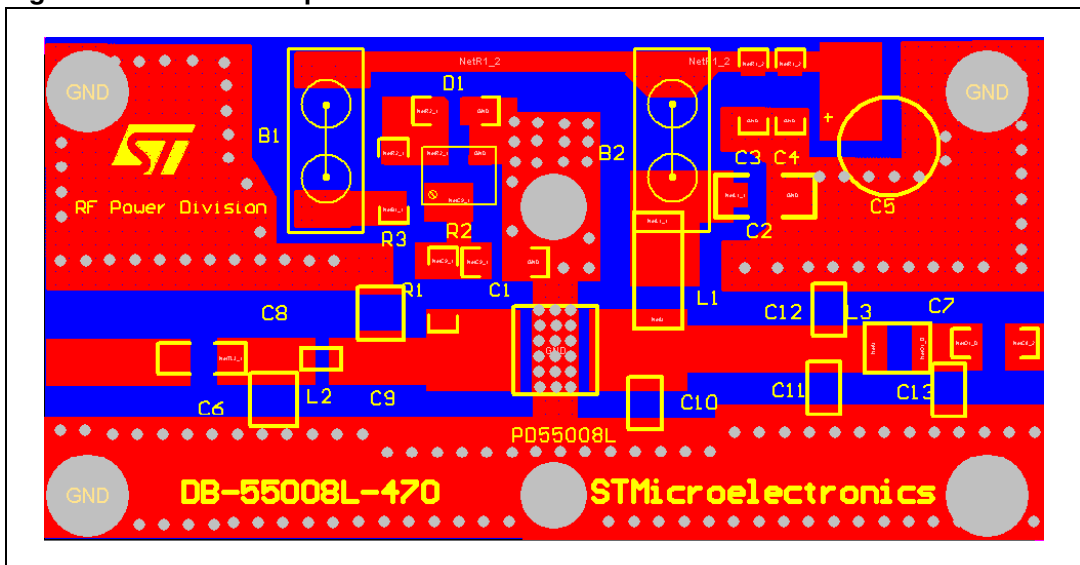
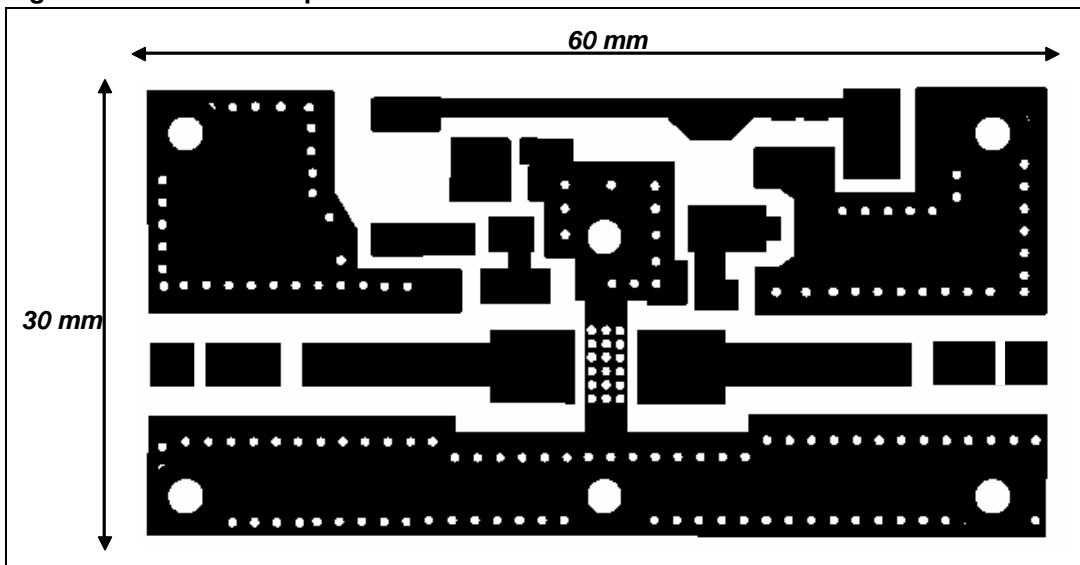
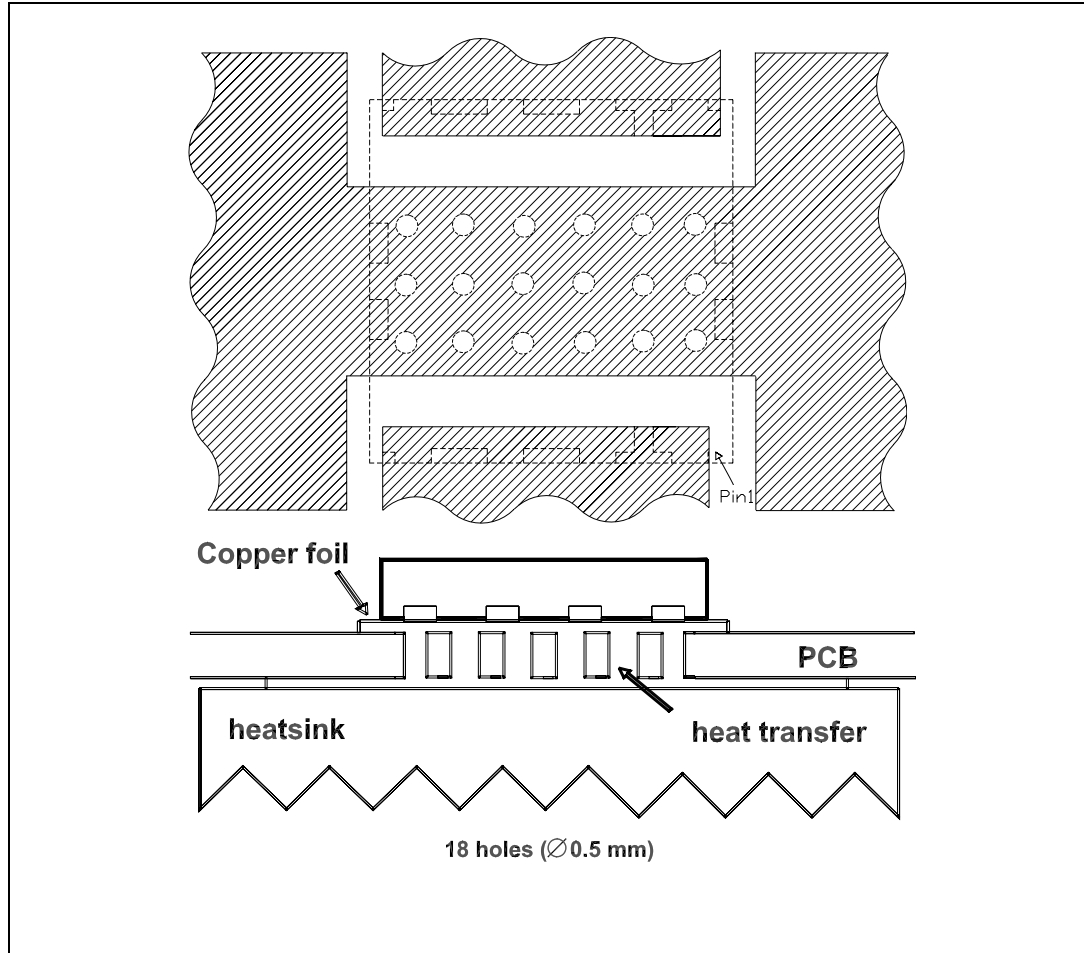


Figure 9. Test circuit photomaster



6 Mounting indications - PD55008L-E

Figure 10. Standard SMD mounting



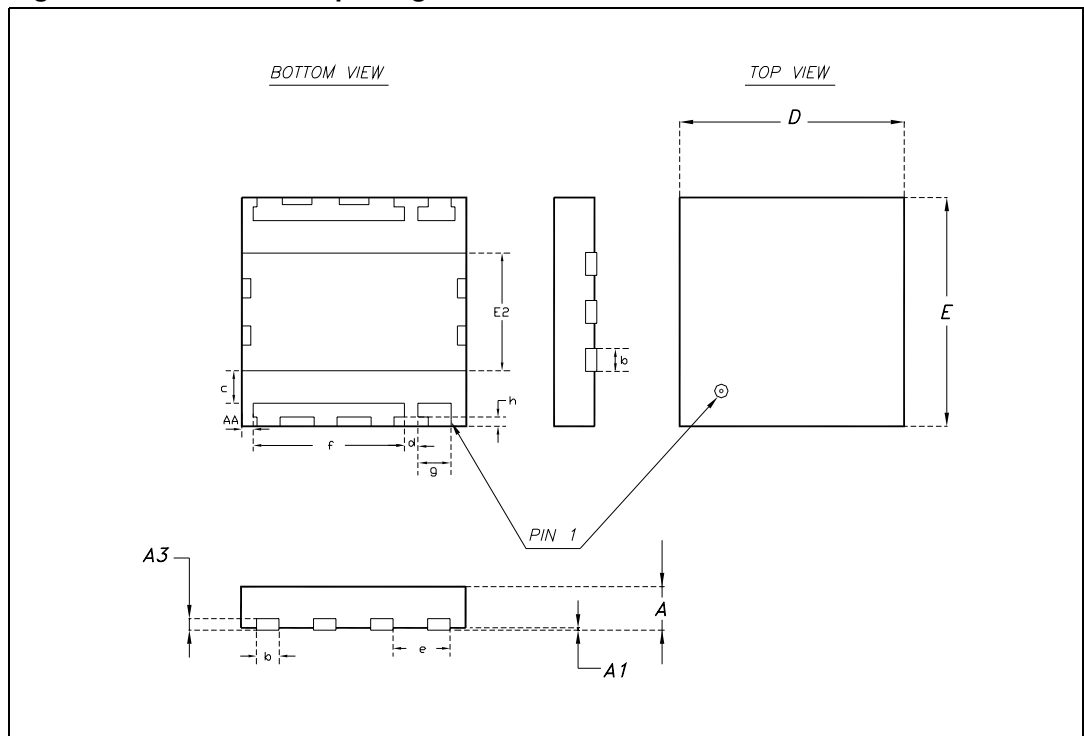
7 Package mechanical data - PD55008L-E

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 6. PD55008L-E PowerFLAT™ mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.24			0.009	
AA	0.15	0.25	0.35	0.006	0.01	0.014
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.64	0.71	0.79	0.025	0.028	0.031
D		5.00			0.197	
d		0.30			0.011	
E		5.00			0.197	
E2	2.49	2.57	2.64	0.098	0.101	0.104
e		1.27			0.050	
f		3.37			0.132	
g		0.74			0.03	
h		0.21			0.008	

Figure 11. PowerFLAT™ package dimensions



8 Revision history

Table 8. Document revision history

Date	Revision	Changes
07-Dec-2006	1	Initial release
18-Dec-2007	2	Updated: Table 5 on page 7

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