



# STD70N2LH5 STU70N2LH5

N-channel 25 V, 0.006  $\Omega$ , 48 A - DPAK - IPAK  
STripFET™ V Power MOSFET

Preliminary Data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STD70N2LH5	25 V	0.0071 $\Omega$	48 A
STU70N2LH5	25 V	0.0075 $\Omega$	48 A

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

## Application

- Switching applications

## Description

This product utilizes the 5<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology. The lowest available R<sub>DS(on)</sub>\*Q<sub>g</sub>, in the standard packages, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

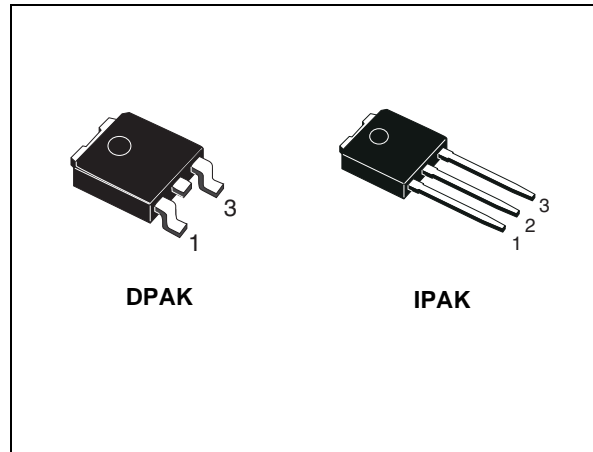


Figure 1. Internal schematic diagram

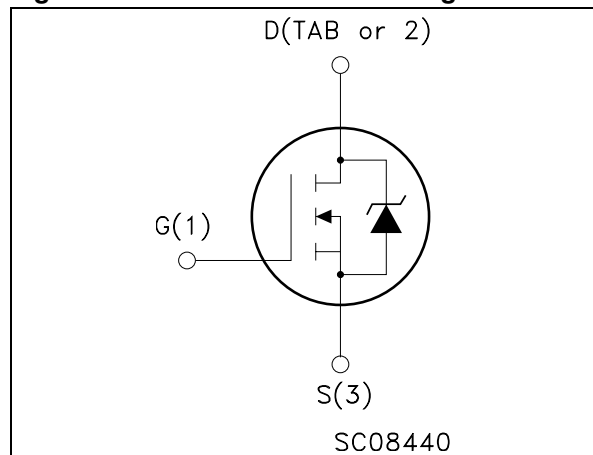


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD70N2LH5	70N2LH5	DPAK	Tape & reel
STU70N2LH5	70N2LH5	IPAK	Tube

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS}=0$ )	25	V
$V_{GS}$	Gate-Source voltage	$\pm 22$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	48	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	43	A
$I_{DM}^{(2)}$	Drain current (pulsed)	192	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	60	W
	Derating factor	0.4	W/ $^{\circ}\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	TBD	mJ
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	$^{\circ}\text{C}$

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting  $T_j = 25\text{ }^{\circ}\text{C}$ ,  $I_D = 24\text{ A}$ ,  $V_{DD} = 12\text{ V}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.5	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-case max	100	$^{\circ}\text{C/W}$
$T_j$	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

## 2 Electrical characteristics

( $T_{CASE} = 25^{\circ}\text{C}$  unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	25			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 25\ \text{V}$ $V_{DS} = 25\ \text{V}$ , $T_C = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 22\ \text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 24\ \text{A}$ SMD version		0.006	0.0071	$\Omega$
		$V_{GS} = 10\ \text{V}$ , $I_D = 24\ \text{A}$		0.0064	0.0075	$\Omega$
		$V_{GS} = 5\ \text{V}$ , $I_D = 24\ \text{A}$ SMD version		0.008	0.01	$\Omega$
		$V_{GS} = 5\ \text{V}$ , $I_D = 24\ \text{A}$		0.0084	0.0104	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\ \text{V}$ , $f = 1\ \text{MHz}$ , $V_{GS} = 0$		1300		pF
$C_{oss}$	Output capacitance			300		pF
$C_{rss}$	Reverse transfer capacitance			50		pF
$Q_g$	Total gate charge	$V_{DD} = 15\ \text{V}$ , $I_D = 48\ \text{A}$		8		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 5\ \text{V}$		TBD		nC
$Q_{gd}$	Gate-drain charge	(Figure 3)		TBD		nC
$Q_{gs1}$	Pre $V_{th}$ gate-to-source charge	$V_{DD} = 15\ \text{V}$ , $I_D = 48\ \text{A}$		TBD		nC
$Q_{gs2}$	Post $V_{th}$ gate-to-source charge	$V_{GS} = 5\ \text{V}$ (Figure 8)		TBD		nC
$R_G$	Gate input resistance	$f = 1\ \text{MHz}$ gate bias Bias = 0 test signal level = 20 mV open drain		1.1		$\Omega$

**Table 6. Switching on/off (resistive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=10\text{ V}$ , $I_D=24\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (Figure 2 and Figure 7)		TBD TBD		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=10\text{ V}$ , $I_D=24\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (Figure 2 and Figure 7)		TBD TBD		ns ns

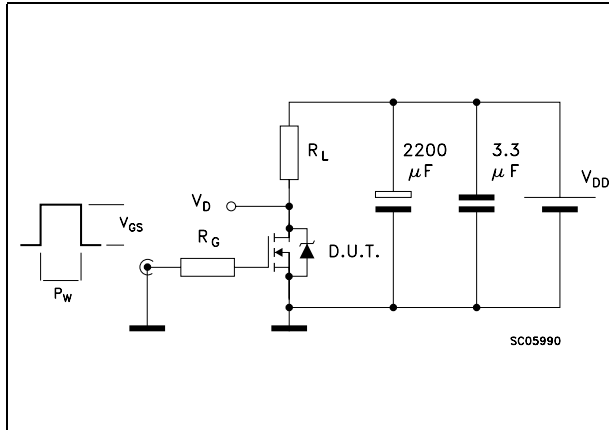
**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				48	A
$I_{SDM}$	Source-drain current (pulsed) <sup>(1)</sup>				192	A
$V_{SD}$	Forward on voltage	$I_{SD}=24\text{ A}$ , $V_{GS}=0$			1.1	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=48\text{ A}$ , $di/dt=100\text{ A}/\mu\text{s}$ , $V_{DD}=20\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ (Figure 4)		TBD TBD TBD		ns nC A

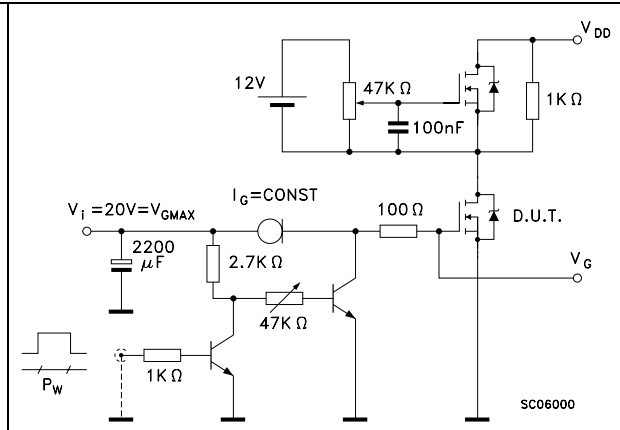
1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

### 3 Test circuit

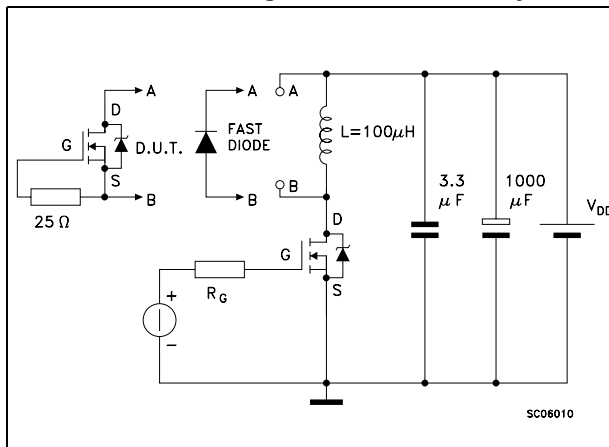
**Figure 2. Switching times test circuit for resistive load**



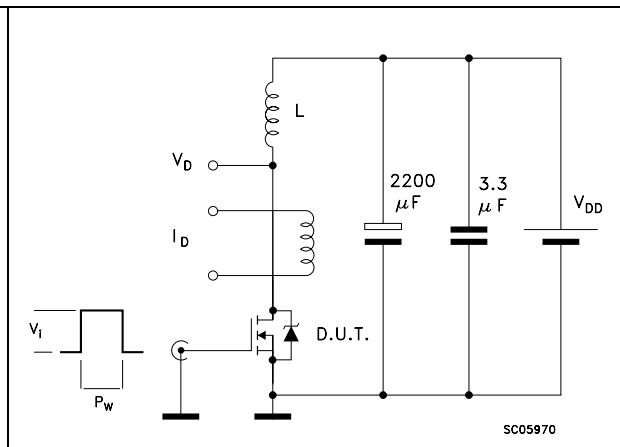
**Figure 3. Gate charge test circuit**



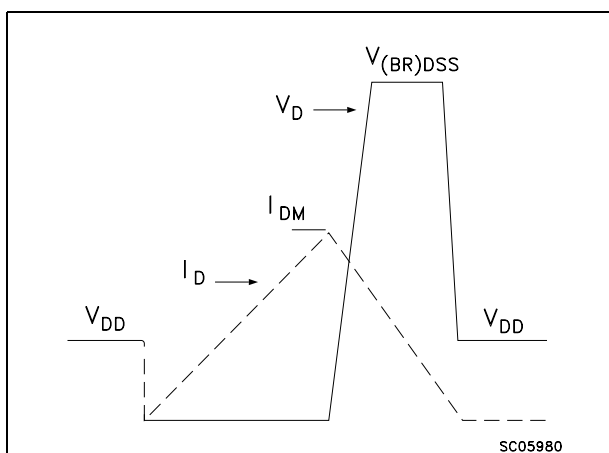
**Figure 4. Test circuit for inductive load switching and diode recovery times**



**Figure 5. Unclamped Inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**

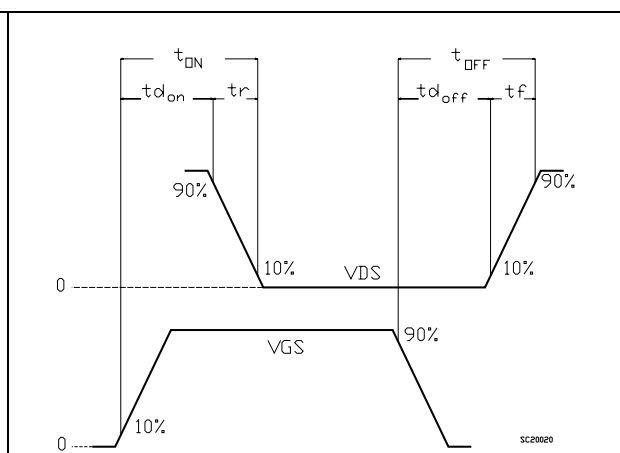
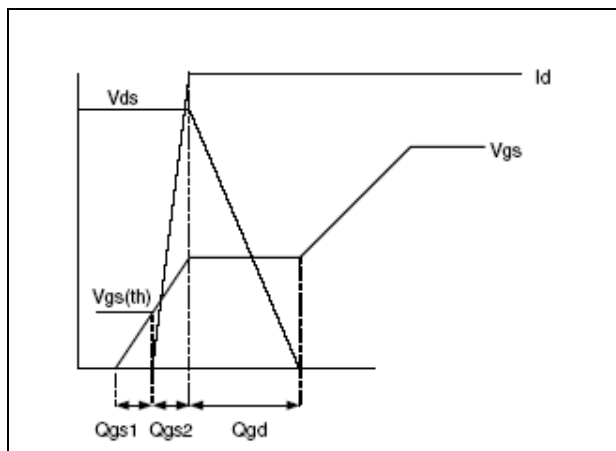


Figure 8. Gate charge waveform

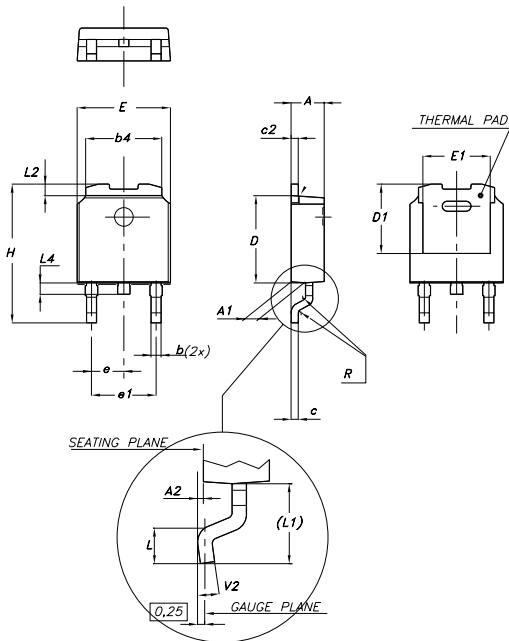


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**DPAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



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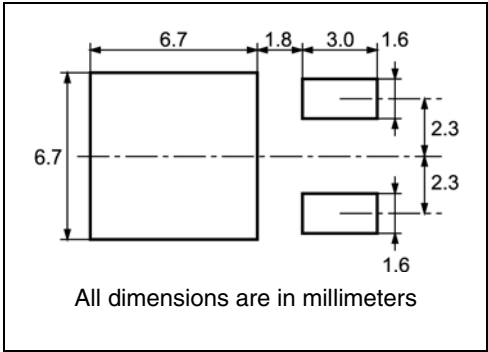
TO-251 (IPAK) MECHANICAL DATA						
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

The diagram illustrates the mechanical specifications of the TO-251 (IPAK) package. The top view shows the package body with dimensions A (height), A1 (lead height), A3 (lead length), B (lead width), B2 (body width), B3 (lead width at base), B5 (lead width at tip), B6 (lead width at base), C (lead thickness), C2 (body thickness), D (body length), E (body width), G (lead length), L (lead length), L1 (lead length at base), and L2 (lead length at tip). The side view shows the package body with dimensions H (height), A (height), A1 (lead height), A3 (lead length), B (lead width), B2 (body width), B3 (lead width at base), B5 (lead width at tip), B6 (lead width at base), C (lead thickness), C2 (body thickness), D (body length), E (body width), G (lead length), L (lead length), L1 (lead length at base), and L2 (lead length at tip).

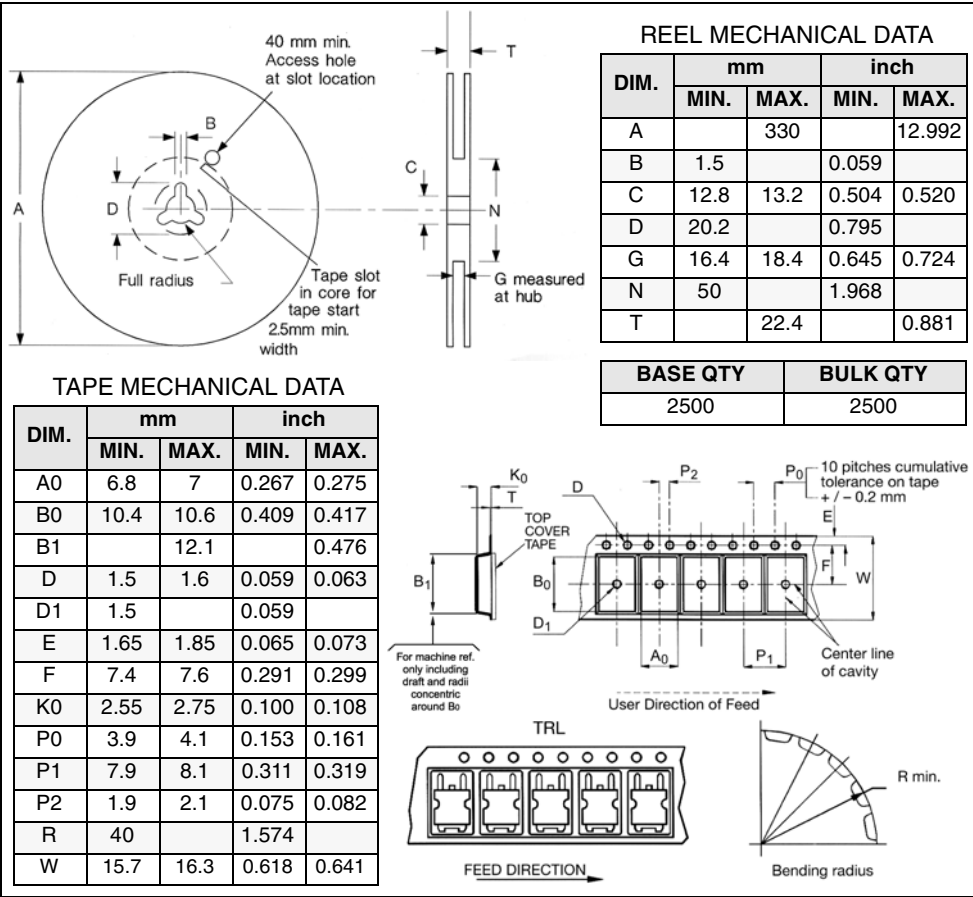
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# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT



## 6 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
16-Jan-2008	1	First release
23-Sep-2008	2	V <sub>GS</sub> value has been changed on <a href="#">Table 2</a> and <a href="#">Table 5</a>

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