M41ST84W

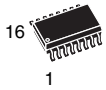
3.0/3.3 V I^2C serial RTC with 44 bytes of NVRAM and supervisory functions

Features

- Automatic battery switchover and deselect
  - Power-fail deselect, V_{PFD} = 2.60 V (nom)
  - Switchover, V_{SO} = 2.50 V (nom)
- 400 kHz I^2C serial interface
- 3.0/3.3 V operating voltage
  - V_{CC} = 2.7 to 3.6 V
- Ultra-low battery supply current of 500 nA (max)
- RoHS compliance
  Lead-free components are compliant with the RoHS directive

Serial RTC features

- 400 kHz I^2C
- 44 bytes of general purpose NVRAM
- Counters for:
  - Seconds, minutes, hours, day, date, month, and year
  - Century
  - 10ths/100ths of seconds
  - Clock calibration register allows compensation for crystal variations over temperature
- Programmable alarm with interrupt
  - Functions during battery backup mode
- Power-down timestamp (HT bit)
- 2.5 to 5.5 V oscillator operating voltage
- 32 KHz oscillator with integrated load capacitance (12.5 pF)
- Battery low flag



SO16 (MQ)

Microprocessor supervisory features

- Programmable watchdog timer
  - 62.5 ms to 128 s time-out period
- Power-on reset/low voltage detect output
- PFI/PFO with 1.25 V reference

Other features

- Programmable squarewave generator (1 Hz to 32 KHz)
- –40°C to +85°C operation
- Packaged in a 16-lead SOIC

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1 Description

The M41ST84W serial real-time clock is built in a low power CMOS SRAM process. It has a 64-byte memory space with 44 bytes of NVRAM and 20 memory-mapped RTC registers (see *Table 3 on page 18*). The RTC registers are configured in binary coded decimal (BCD) format.

A built-in, low power 32.768 kHz oscillator (external crystal controlled) provides the time base for the timekeeping and calendar functions.

The basic clock/calendar functions are handled by the first eight RTC registers, while the other twelve bytes provide status/control for the alarm, watchdog, and square wave functions.

Addresses and data are transferred serially via the two line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

The M41ST84W has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the SRAM and clock operations can be supplied by a small lithium button-cell supply when a power failure occurs. Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupts, watchdog timer and programmable square wave output. Other features include a power-on reset as well as an additional input ($\overline{RSTIN}$) which can also generate an output reset ($\overline{RST}$). The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24 hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically.

The M41ST84W is supplied in a 16-lead SOIC package.

Figure 1. Logic diagram

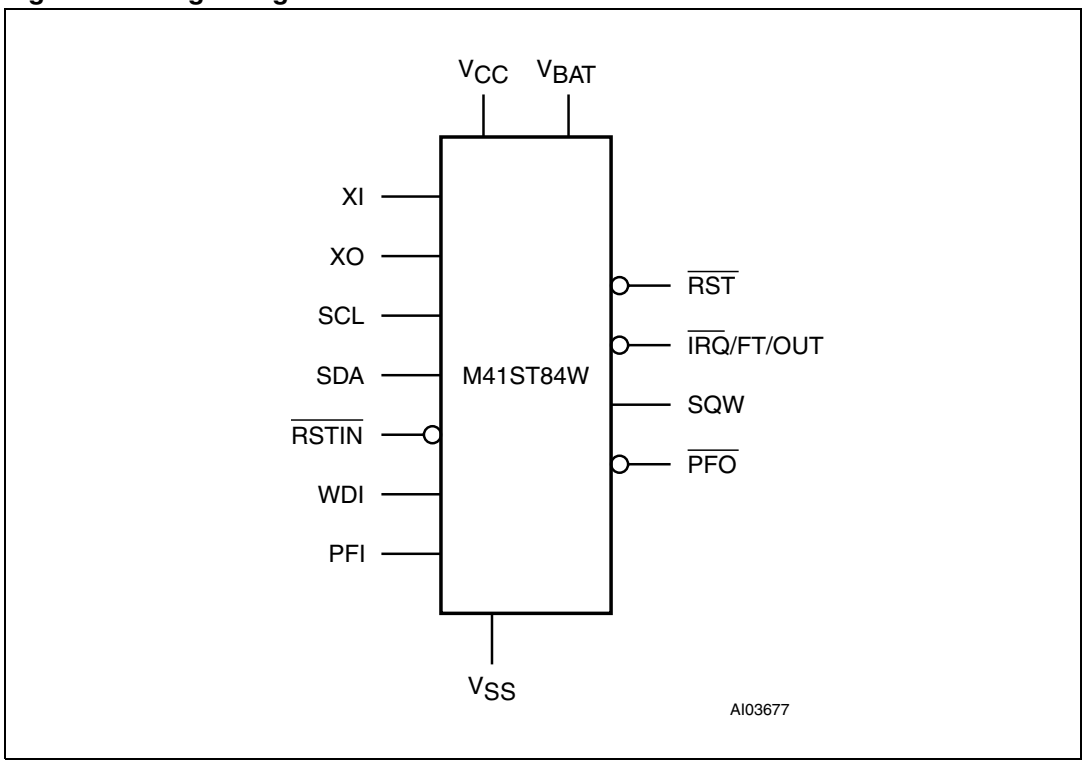


Table 1. Signal names

XI	Oscillator input
XO	Oscillator output
$\overline{IRQ}$/FT/OUT	Interrupt/frequency test/out output (open drain)
PFI	Power fail input
$\overline{PFO}$	Power fail output
$\overline{RST}$	Reset output (open drain)
$\overline{RSTIN}$	Reset input
SCL	Serial clock input
SDA	Serial data input/output
SQW	Square wave output
WDI	Watchdog input
V_{CC}	Supply voltage
V_{BAT}	Battery supply voltage
V_{SS}	Ground
NC	No connect

Figure 2. 16-pin SOIC connections

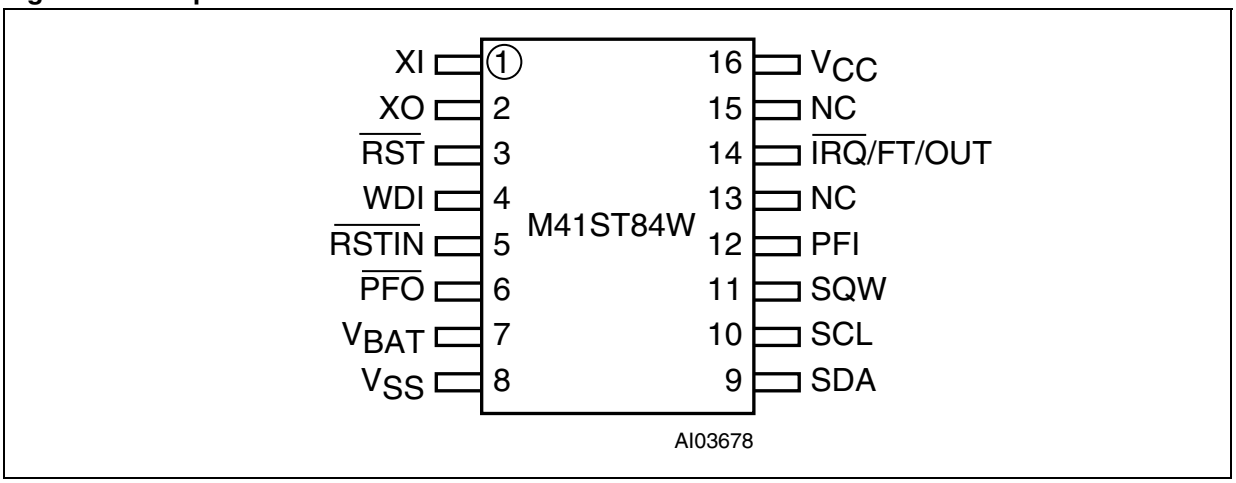
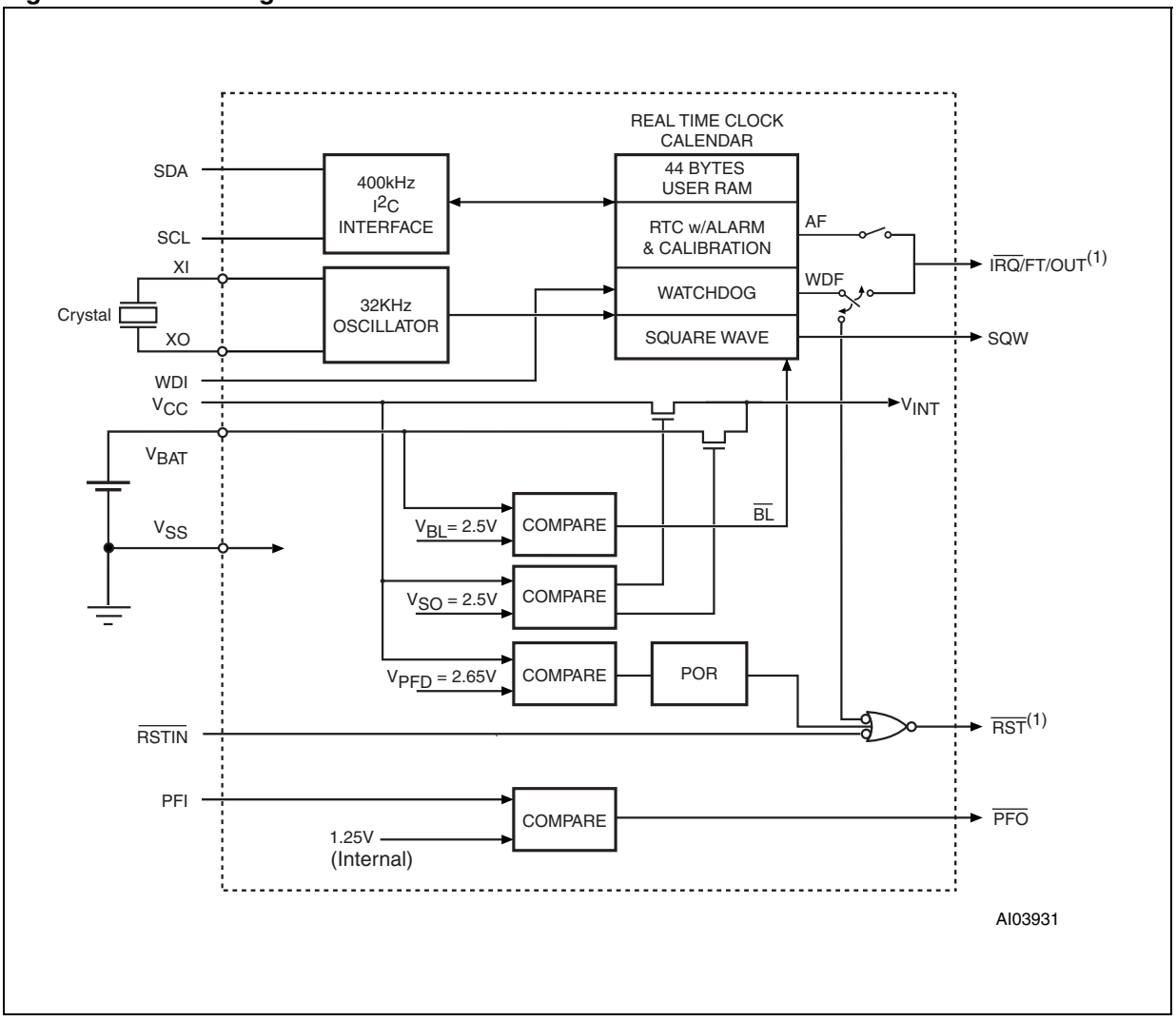
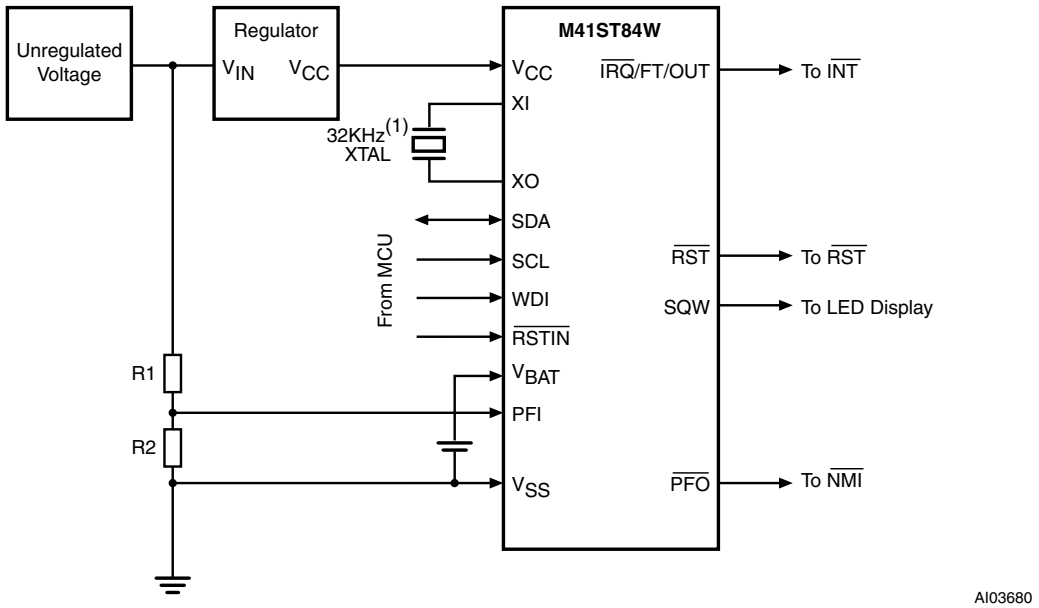


Figure 3. Block diagram



1. Open drain output

Figure 4. Hardware hookup



1. User-supplied crystal

2 Operating modes

The M41ST84W clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Tenths/hundredths of a second register
2. Seconds register
3. Minutes register
4. Century/hours register
5. Day register
6. Date register
7. Month register
8. Year register
9. Control register
10. Watchdog register

11. - 16. Alarm registers

17. - 19. Reserved

20. Square wave register

21. - 64. User RAM

The M41ST84W clock continually monitors V_{CC} for an out-of tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system. When V_{CC} falls below V_{SO}, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min) plus t_{rec} (min).

For more information on battery storage life refer to application note AN1012.

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. the data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter”, the receiving device that gets the message is called “receiver”. The device that controls the message is called “master”. The devices that are controlled by the master are called “slaves”.

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 5. Serial bus data transfer sequence

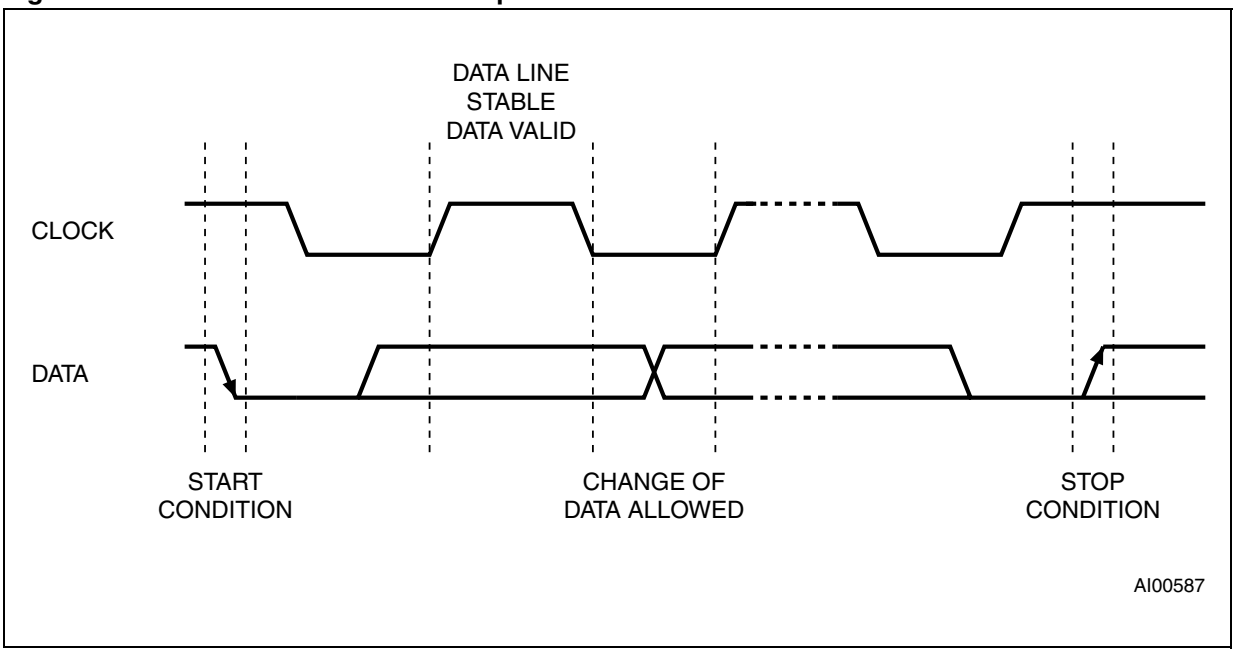


Figure 6. Acknowledgement sequence

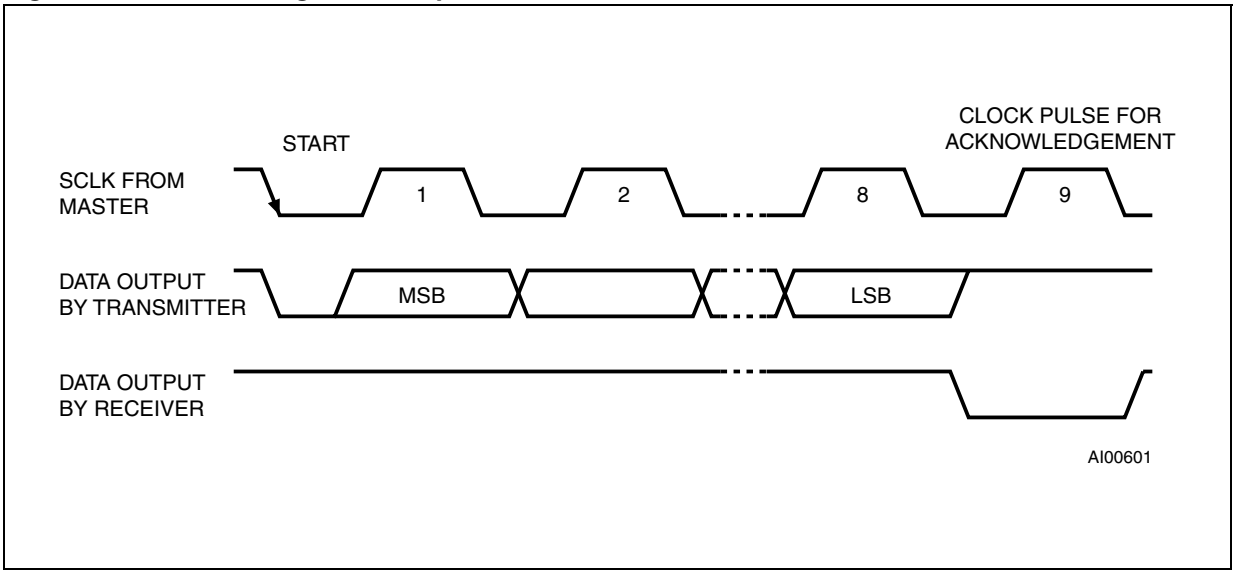


Figure 7. Bus timing requirements sequence

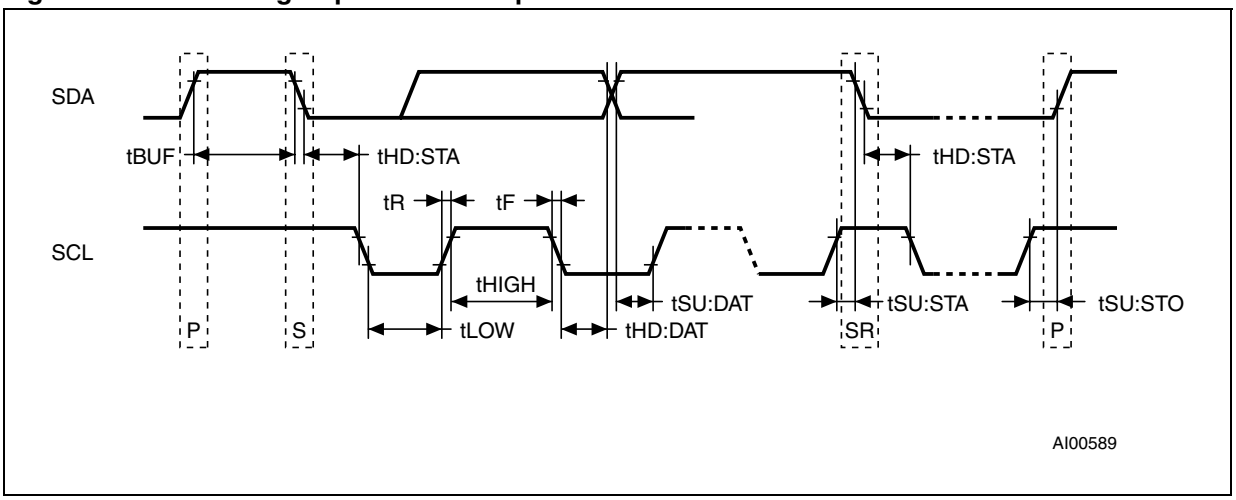


Table 2. AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		µs
t_F	SDA and SCL fall time		300	ns
$t_{HD:DAT}$[2]	Data hold time	0		µs
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600		ns
t_{HIGH}	Clock high period	600		ns
t_{LOW}	Clock low period	1.3		µs
t_R	SDA and SCL rise time		300	ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600		ns
$t_{SU:STO}$	STOP condition setup time	600		ns

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 3.6 V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

2.2 READ mode

In this mode the master reads the M41ST84W slave after setting the slave address (see *Figure 8*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41ST84W slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to "An+2."

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter (see *Figure 9 on page 15*).

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a stop condition or when the pointer increments to a non-clock or RAM address.

Note: This is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41ST84W slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 10 on page 15*).

Figure 8. Slave address location

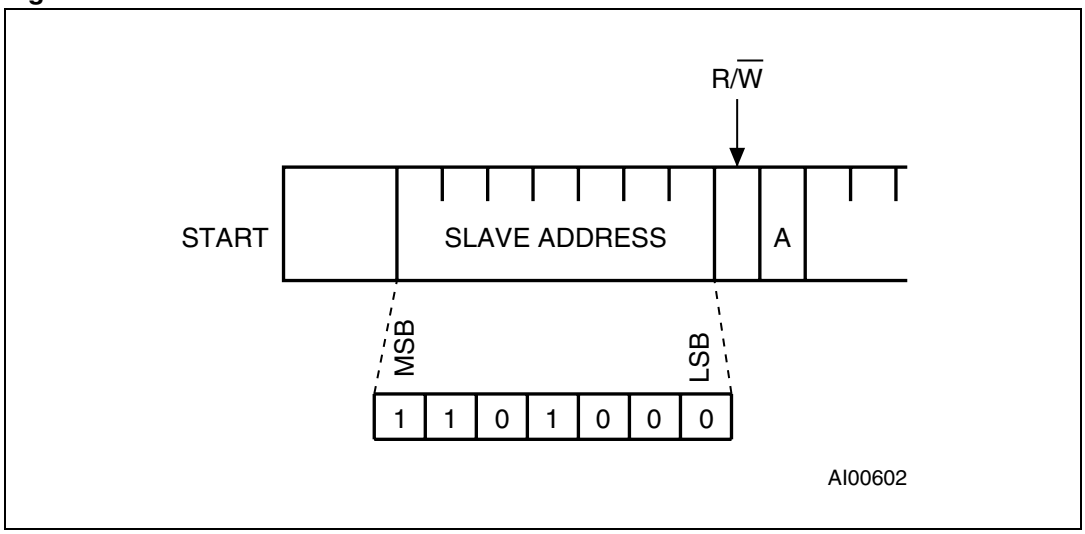


Figure 9. READ mode sequence

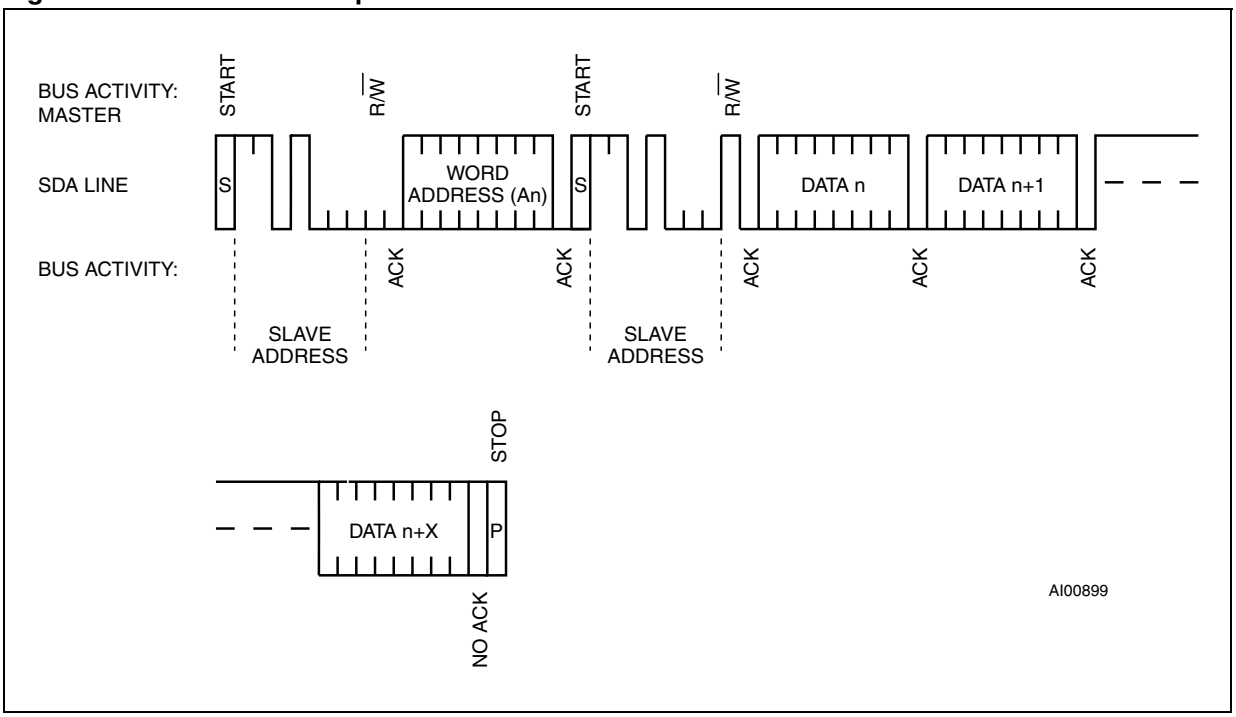
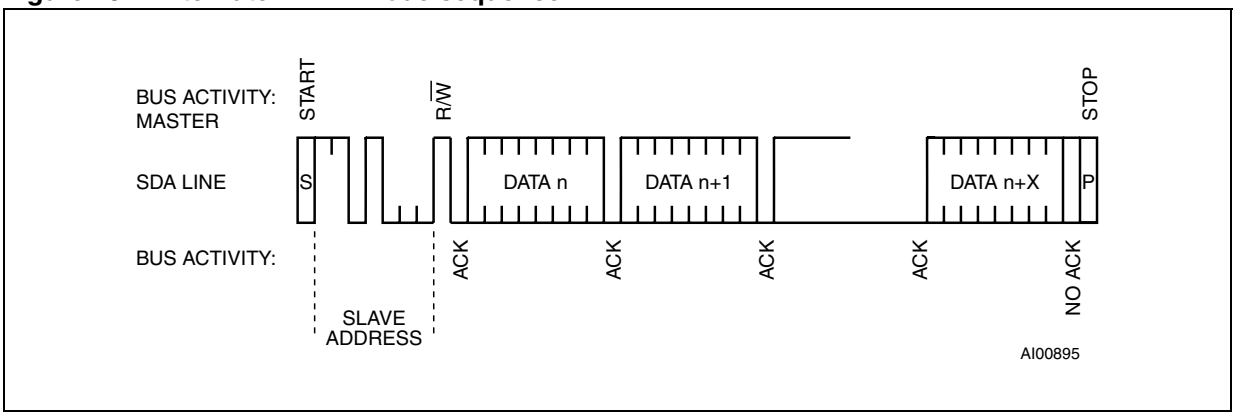


Figure 10. Alternate READ mode sequence



2.3 WRITE mode

In this mode the master transmitter transmits to the M41ST84W slave receiver. Bus protocol is shown in *Figure 11*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41ST84W slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address (see *Figure 8 on page 14*) and again after it has received the word address and each data byte.

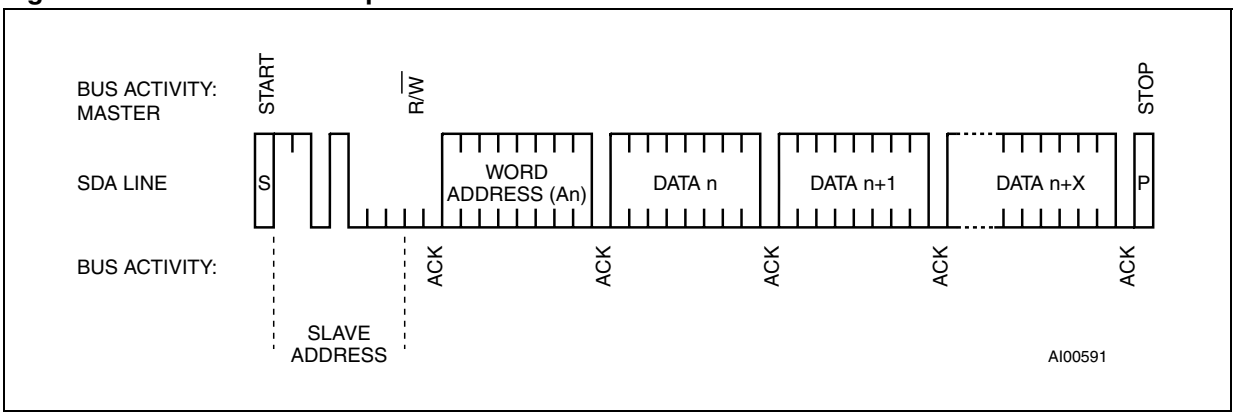
2.4 Data retention mode

With valid V_{CC} applied, the M41ST84W can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M41ST84W will automatically deselect, write protecting itself when V_{CC} falls between V_{PFD}(max) and V_{PFD}(min). This is accomplished by internally inhibiting access to the clock registers. At this time, the Reset pin ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the battery backup switchover voltage (V_{SO}), power input is switched from the V_{CC} pin to the external battery, and the clock registers and SRAM are maintained from the attached battery supply.

All outputs become high impedance. On power up, when V_{CC} returns to a nominal value, write protection continues for t_{rec}. The $\overline{RST}$ signal also remains active during this time (see *Figure 18 on page 30*).

For a further more detailed review of lifetime calculations, please see application note AN1012.

Figure 11. WRITE mode sequence



3 Clock operation

The eight byte clock register (see *Table 3 on page 18*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

Note: A WRITE to any clock register will result in the tenths/hundredths of seconds being reset to "00," and tenths/hundredths of seconds cannot be written to any value other than "00."

Bits D6 and D7 of clock register 03h (century/hours register) contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle. Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month and years. The ninth clock register is the control register (this is described in the clock calibration section). Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The eight clock registers may be read one byte at a time, or in a sequential block. The control register (address location 08h) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

3.1 Power-down time-stamp

When a power failure occurs, the Halt update bit (HT) will automatically be set to a '1.' This will prevent the clock from updating the TIMEKEEPER® registers, and will allow the user to read the exact time of the power-down event. Resetting the HT bit to a '0' will allow the clock to update the timekeeper registers with the current time. for more information, see application note AN1572.

3.2 TIMEKEEPER® registers

The M41ST84W offers 12 additional internal registers which contain the Alarm, watchdog, flag, square wave and control data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a stop condition or when the pointer increments to a non-clock or RAM address.

TIMEKEEPER and alarm registers store data in BCD. Control, watchdog and square wave registers store data in binary format.

Table 3. TIMEKEEPER® register map

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0.1 seconds				0.01 seconds				Seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	CEB	CB	10 hours		Hours (24 hour format)				Century/hours	0-1/00-23
04h	TR	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Control	
09h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	ABE	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	HT	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	BL	0	0	0	0	Flags	
10h	0	0	0	0	0	0	0	0	Reserved	
11h	0	0	0	0	0	0	0	0	Reserved	
12h	0	0	0	0	0	0	0	0	Reserved	
13h	RS3	RS2	RS1	RS0	0	0	0	0	SQW	

Keys:
- S = Sign bit
- FT = Frequency test bit
- ST = Stop bit
- 0 = Must be set to zero
- BL = Battery low flag (read only)
- BMB0-BMB4 = Watchdog multiplier bits
- CEB = Century enable bit
- CB = Century bit
- OUT = Output level
- AFE = Alarm flag enable flag
- RB0-RB1 = Watchdog resolution bits
- WDS = Watchdog steering bit
- ABE = Alarm in battery backup mode enable bit
- RPT1-RPT5 = Alarm repeat mode bits
- WDF = Watchdog flag (read only)
- AF = Alarm flag (read only)
- SQWE = Square wave enable
- RS0-RS3 = SQW frequency
- HT = Halt update bit
- TR = t_{rec} bit

3.3 Calibrating the clock

The M41ST84W is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not exceed +/–35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about +/–1.53 minutes per month. When the Calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25°C.

The oscillation rate of crystals changes with temperature (see *Figure 12 on page 20*). Therefore, the M41ST84W design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 13 on page 20*. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the control register (08h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41ST84W may require.

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934: TIMEKEEPER calibration. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{\text{IRQ}}$/FT/OUT pin. The pin will toggle at 512Hz, when the stop bit (ST, D7 of 01h) is '0,' the frequency test bit (FT, D6 of 08h) is '1,' the alarm flag enable bit (AFE, D7 of 0Ah) is '0,' and the watchdog steering bit (WDS, D7 of 09h) is '1' or the watchdog register (09h = 0) is reset.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

The $\overline{\text{IRQ}}$/FT/OUT pin is an open drain output which requires a pull-up resistor to V_{CC} for proper operation. A 500 to 10 k resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

Figure 12. Crystal accuracy across temperature

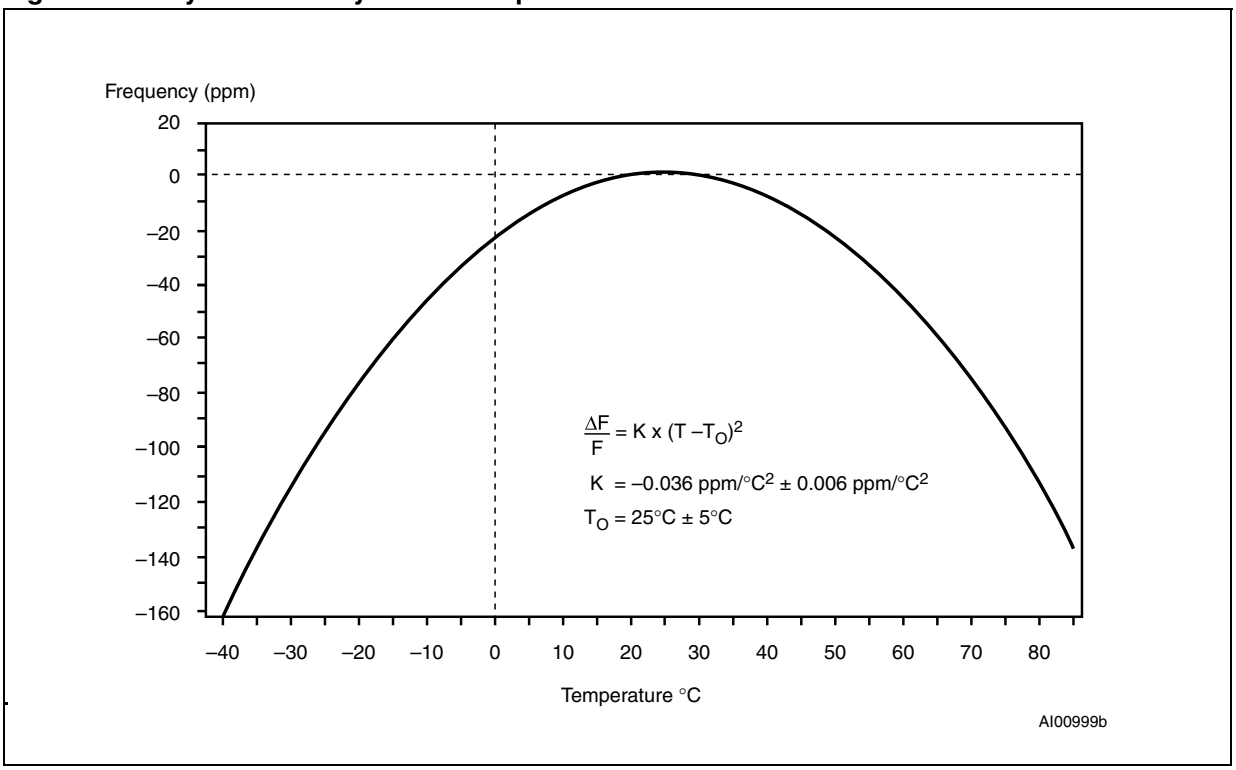
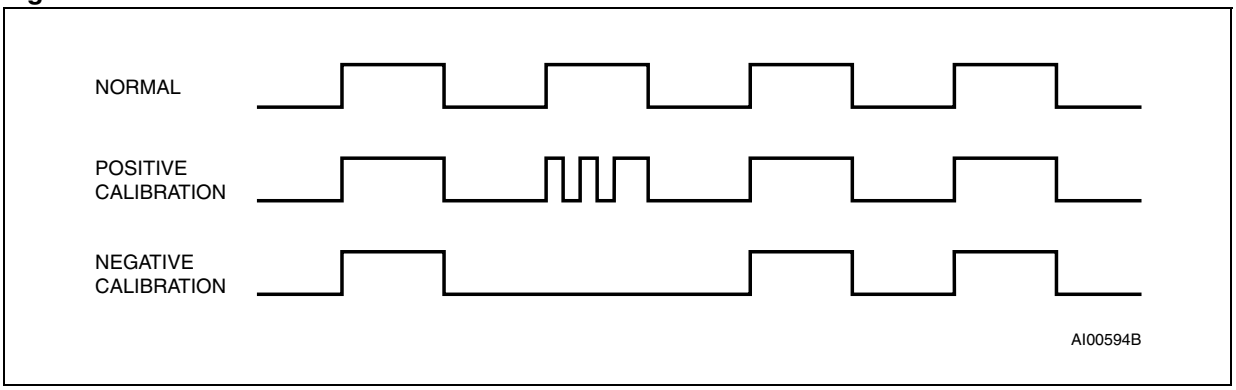


Figure 13. Clock calibration



3.4 Setting alarm clock registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the M41ST84W is in the battery backup to serve as a system wakeup call.

Bits RPT5-RPT1 put the alarm in the repeat mode of operation. *Table 4* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5-RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT/OUT pin.

Note: If the address pointer is allowed to increment to the flag register address, an alarm condition will not cause the interrupt/flag to occur until the address pointer is moved to a different address. it should also be noted that if the last address written is the "alarm seconds," the address pointer will increment to the flag address, causing this situation to occur.

The $\overline{IRQ}$/FT/OUT output is cleared by a READ to the flags register as shown in *Figure 14*. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

The $\overline{IRQ}$/FT/OUT pin can also be activated in the battery backup mode. The $\overline{IRQ}$/FT/OUT will go low if an alarm occurs and both ABE (alarm in battery backup mode enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the flag register at system boot-up to determine if an alarm was generated while the M41ST84W was in the deselect mode during power-up. *Figure 15 on page 22* illustrates the backup mode alarm timing.

Figure 14. Alarm interrupt reset waveform

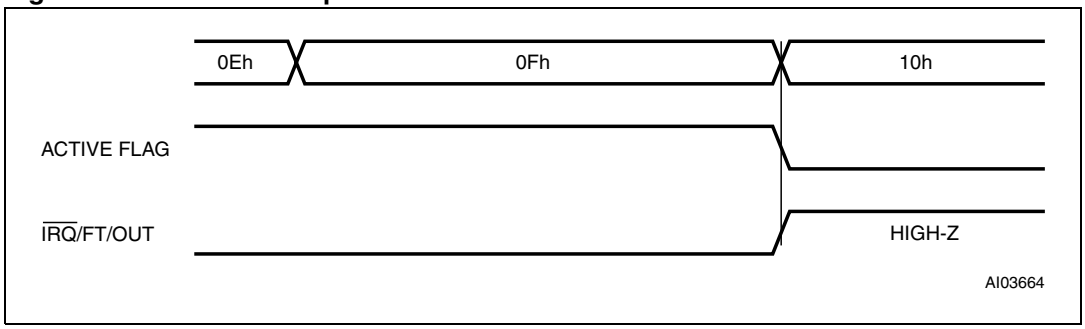
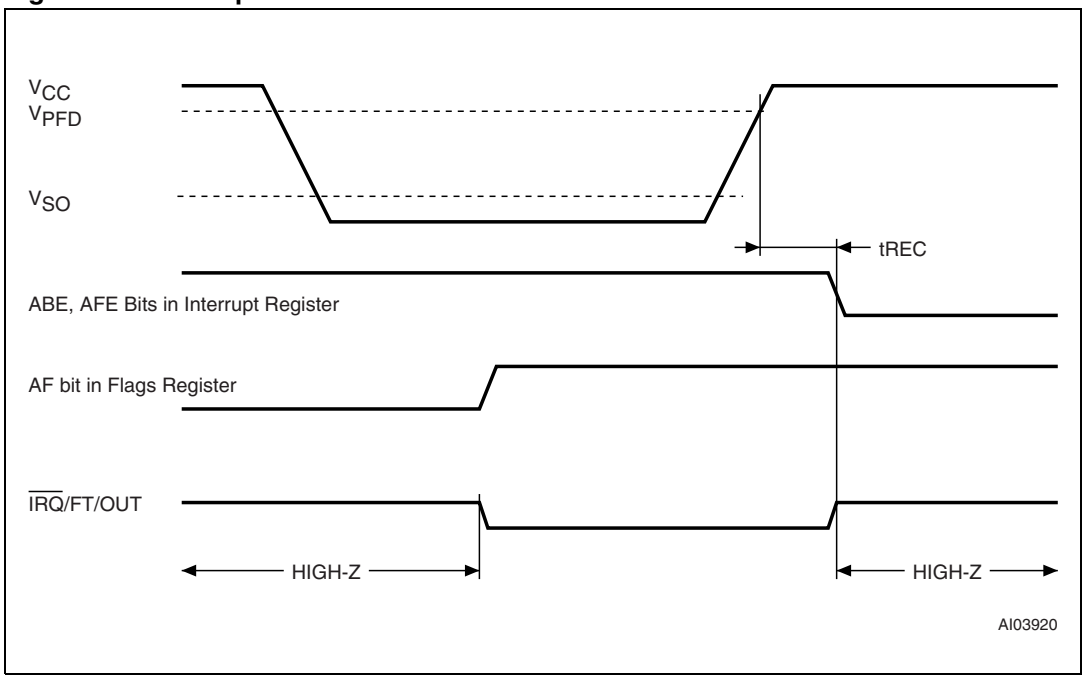


Table 4. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

Figure 15. Backup mode alarm waveform



3.5 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog Register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1, or 3 seconds).

Note: Accuracy of timer is within ± the selected resolution.

If the processor does not reset the timer within the specified period, the M41ST84W sets the WDF (watchdog flag) and generates a watchdog interrupt or a microprocessor reset.

The most significant bit of the watchdog register is the watchdog steering bit (WDS). When set to a '0,' the watchdog will activate the $\overline{IRQ}$/FT/OUT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the $\overline{RST}$ pin for t_{rec}. The watchdog register, FT, AFE, ABE and SQWE bits will reset to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1.'

The watchdog timer can be reset by two methods: 1) a transition (high-to-low or low-to-high) can be applied to the watchdog input pin (WDI) or 2) the microprocessor can perform a WRITE of the watchdog register. The time-out period then starts over.

Note: The WDI pin should be tied to V_{SS} if not used.

In order to perform a software reset of the watchdog timer, the original time-out period can be written into the watchdog register, effectively restarting the count-down cycle.

Should the watchdog timer time-out, and the WDS bit is programmed to output an interrupt, a value of 00h needs to be written to the watchdog register in order to clear the $\overline{IRQ}$/FT/OUT

pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the flags register will reset the watchdog flag (Bit D7; Register 0Fh).

The watchdog function is automatically disabled upon power-up and the watchdog register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT/OUT pin and the frequency test (FT) function is activated, the watchdog function prevails and the frequency test function is denied.

3.6 Square wave output

The M41ST84W offers the user a programmable square wave function which is output on the SQW pin. The RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in *Table 5*. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 0Ah.

Table 5. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

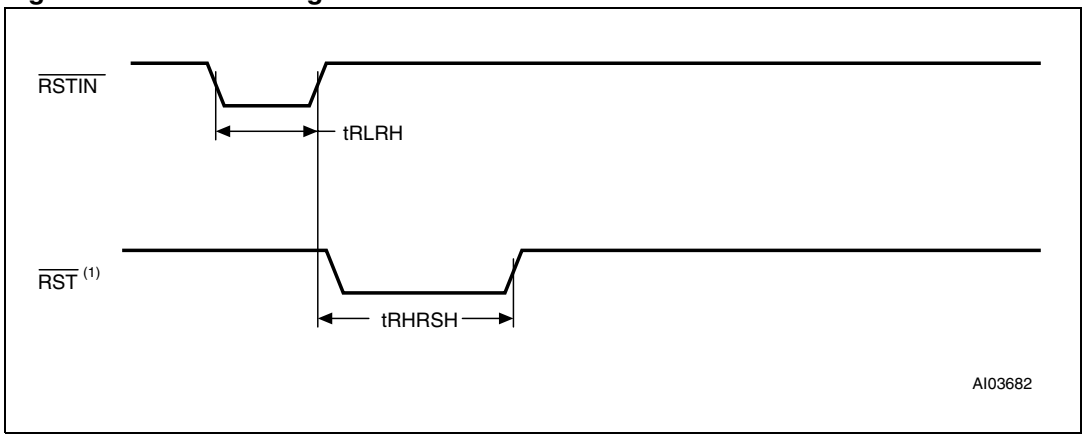
3.7 Power-on reset

The M41ST84W continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for t_{rec} after V_{CC} passes V_{PFD}(max). The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor should be chosen to control rise time.

3.8 Reset input ($\overline{RSTIN}$)

The M41ST84W provides an independent input which can generate an output reset. The duration and function of this reset is identical to a reset generated by a power cycle. *Table 6* and *Figure 16* illustrate the AC reset characteristics of this function. Pulses shorter than t_{RLRH} will not generate a reset condition. $\overline{RSTIN}$ is internally pulled up to V_{CC} through a 100 kΩ resistor.

Figure 16. $\overline{RSTIN}$ timing waveform



Note: With pull-up resistor

Table 6. Reset AC characteristics

Symbol	Parameter(1)	Min	Max	Unit
t_{RLRH}(2)	$\overline{RSTIN}$ low to $\overline{RSTIN}$ high	200		ns
t_{RHRSH}(3)	$\overline{RSTIN}$ high to $\overline{RST}$ high	40	200	ms

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 3.6 V (except where noted).
2. Pulse width less than 50 ns will result in no RESET (for noise immunity).
3. Programmable (see *Table 8 on page 26*)

3.9 Power-fail INPUT/OUTPUT

The power-fail input (PFI) is compared to an internal reference voltage (1.25 V). If PFI is less than the power-fail threshold (V_{PFI}), the power-fail output ($\overline{PFO}$) will go low. This function is intended for use as an under-voltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see *Figure 4 on page 9*) to either the unregulated DC input (if it is available) or the regulated output of the V_{CC} regulator. The voltage divider can be set up such that the voltage at PFI falls below V_{PFI} several milliseconds before the regulated V_{CC} input to the M41ST84W or the microprocessor drops below the minimum operating voltage.

During battery backup, the power-fail comparator turns off and $\overline{PFO}$ goes (or remains) low. This occurs after V_{CC} drops below V_{PFD}(min). When power returns, $\overline{PFO}$ is forced high, irrespective of V_{PFI} for the write protect time (t_{rec}), which is the time from V_{PFD}(max) until the inputs are recognized. At the end of this time, the power-fail comparator is enabled and $\overline{PFO}$ follows PFI. If the comparator is unused, PFI should be connected to V_{SS} and $\overline{PFO}$ left unconnected.

3.10 Century bit

Bits D7 and D6 of clock register 03h contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a “1” will cause CB to toggle, either from a “0” to “1” or from “1” to “0” at the turn of the century (depending upon its initial state). If CEB is set to a “0”, CB will not toggle.

3.11 Output driver pin

When the FT bit, AFE bit and watchdog register are not set, the $\overline{IRQ}$/FT/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words, when D7 (OUT bit) and D6 (FT bit) of address location 08h are a '0,' then the $\overline{IRQ}$/FT/OUT pin will be driven low.

Note: The $\overline{IRQ}$/FT/OUT pin is an open drain which requires an external pull-up resistor.

3.12 Battery low warning

The M41ST84W automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The battery low (BL) bit, bit D4 of flags register 0Fh, will be asserted if the battery voltage is found to be less than approximately 2.5 V. The BL bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery backup mode, the battery should be replaced. The battery may be replaced while V_{CC} is applied to the device.

The M41ST84W only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery backup mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

3.13 t_{rec} bit

Bit D7 of clock register 04h contains the t_{rec} bit (TR). t_{rec} refers to the automatic continuation of the deselect time after V_{CC} reaches V_{PFD}. This allows for a voltage setting time before WRITEs may again be performed to the device after a power-down condition. The t_{rec} bit will allow the user to set the length of this deselect time as defined by *Table 7 on page 26*.

3.14 Initial power-on defaults

Upon initial application of power to the device, the following register bits are set to a '0' state: watchdog register, TR, FT, AFE, ABE, and SQWE. The following bits are set to a '1' state: ST, OUT, and HT (see *Table 8 on page 26*).

Table 7. t_{rec} definitions

t_{REC} bit (TR)	STOP bit (ST)	t_{rec} time		Units
		Min	Max	
0	0	96	98	ms
0	1	40	200(1)	ms
1	X	50	2000	µs

1. Default setting

Table 8. Default values

Condition	TR	ST	HT	Out	FT	AFE	ABE	SQWE	WATCHDOG register(1)
Initial power-up (battery attach)(2)	0	1	1	1	0	0	0	0	0
Subsequent power-up (with battery backup)(3)	UC	UC	1	UC	0	0	0	0	0

1. WDS, BMB0-BMB4, RB0, RB1.
2. State of other control bits undefined.
3. UC = Unchanged

4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 9. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	–55 to 150	°C
T_{SLD}(1)(2)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltages	–0.3 to V_{CC} + 0.3	V
V_{CC}	Supply voltage	–0.3 to 4.6	V
I_O	Output current	20	mA
P_D	Power dissipation	1	W

1. For SO package, standard (SnPb) lead finish: Reflow at peak temperature of 225°C (total thermal budget not to exceed 180°C for between 90 to 150 seconds).
2. For SO package, lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

5 DC and AC parameters

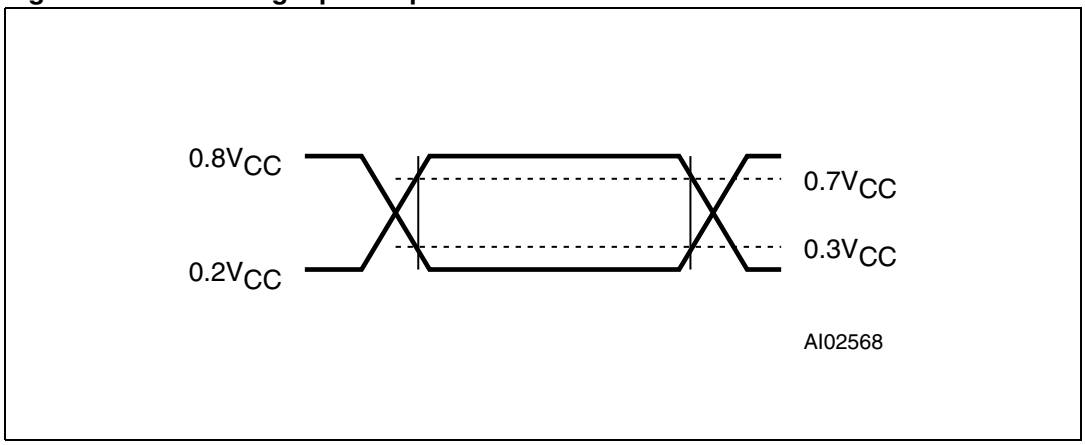
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 10. DC and AC measurement conditions

Parameter	M41ST84W
V_{CC} supply voltage	2.7 to 3.6 V
Ambient operating temperature	–40 to 85°C
Load capacitance (C_L)	50 pF
Input rise and fall times	≤ 50 ns
Input pulse voltages	0.2 to 0.8V_{CC}
Input and output timing ref. voltages	0.3 to 0.7V_{CC}

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 17. AC testing input/output waveforms



Note: 50 pF for M41ST84W.

Table 11. Capacitance

Symbol	Parameter(1)(2)	Min	Max	Unit
C_{IN}	Input capacitance		7	pF
C_{IO}(3)	Input / output capacitance		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

1. Effective capacitance measured with power supply at 3 V. Sampled only, not 100% tested.
2. At 25°C, f = 1 MHz.
3. Outputs deselected.

Table 12. DC characteristics

Sym	Parameter	Test condition(1)	M41ST84W			Unit
			Min	Typ	Max	
I_{BAT}	Battery current OSC ON	T_A = 25°C, V_{CC} = 0 V, V_{BAT} = 3 V		400	500	nA
	Battery current OSC OFF			50		nA
I_{CC1}	Supply current	f = 400 kHz			0.75	mA
I_{CC2}	Supply current (standby)	SCL, SDA = V_{CC} – 0.3 V or V_{SS} + 0.3 V			0.50	mA
I_{LI}(2)	Input leakage current	0V ≤ V_{IN} ≤ V_{CC}			±1	µA
	Input leakage current (PFI)		–25	2	25	nA
I_{LO}(3)	Output leakage current	0V ≤ V_{OUT} ≤ V_{CC}			±1	µA
V_{IH}	Input high voltage		0.7V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input low voltage		–0.3		0.3V_{CC}	V
V_{BAT}	Battery voltage		2.5	3.0	3.5(4)	V
V_{OH}	Output high voltage(5)	I_{OH} = –1.0mA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 3.0mA			0.4	V
	Output low voltage (open drain)(6)	I_{OL} = 10mA			0.4	V
	Pull-up supply voltage (open drain)	$\overline{RST}$, $\overline{IRQ}$/FT/OUT			3.6	V
V_{PFD}	Power fail deselect		2.55	2.60	2.70	V
V_{PFI}	PFI input threshold	V_{CC} = 3V(W)	1.225	1.250	1.275	V
	PFI hysteresis	PFI Rising		20	70	mV
V_{SO}	Battery backup switchover			2.5		V

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 3.6 V (except where noted).
2. $\overline{RSTIN}$ internally pulled-up to V_{CC} through 100 KΩ resistor. WDI internally pulled-down to V_{SS} through 100 KΩ resistor.
3. Outputs deselected.
4. For rechargeable backup, V_{BAT} (max) may be considered V_{CC}.
5. For $\overline{PFO}$ and SQW pins (CMOS).
6. For $\overline{IRQ}$/FT/OUT, $\overline{RST}$ pins (open drain): if pulled-up to supply other than V_{CC}, this supply must be equal to, or less than 3.0 V when V_{CC} = 0 V (during battery backup mode).

Table 13. Crystal electrical characteristics (externally supplied)

Symbol	Parameter(1)(2)	Typ	Min	Max	Unit
f_0	Resonant frequency	32.768			kHz
R_S	Series resistance			50	kΩ
C_L	Load capacitance	12.5			pF

1. Load capacitors are integrated within the M41ST84W. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
2. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, tuning fork type (thru-hole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. KDS can be contacted at http://www.kds.info/index_en.htm for further information on this crystal type.

Figure 18. Power down/up mode AC waveforms

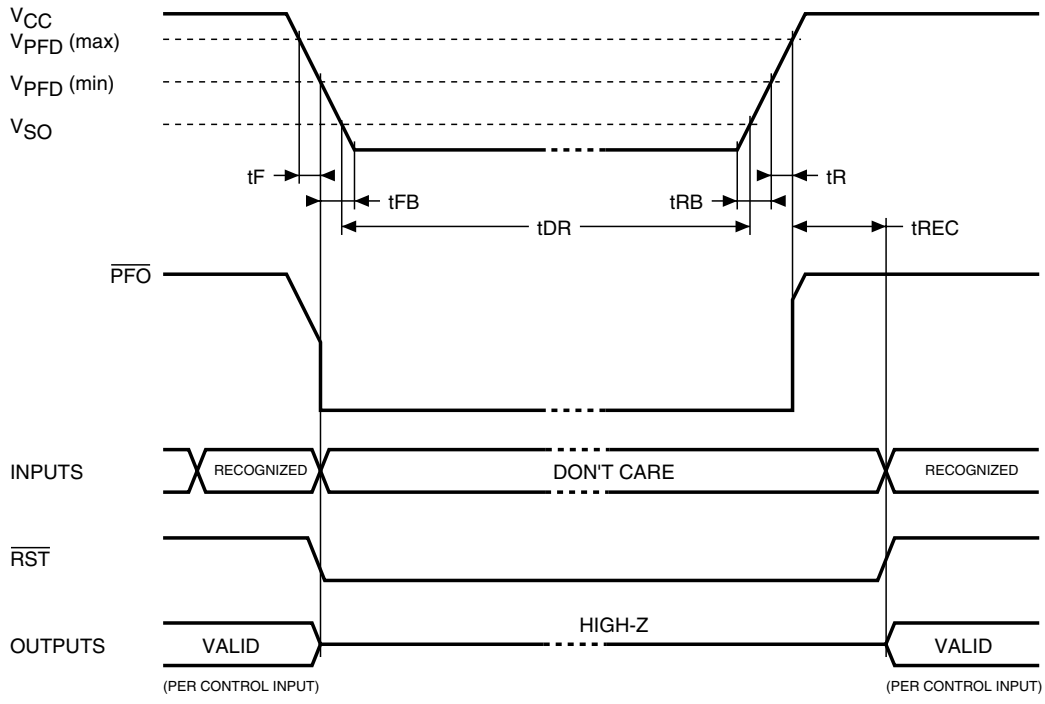


Table 14. Power down/up AC characteristics

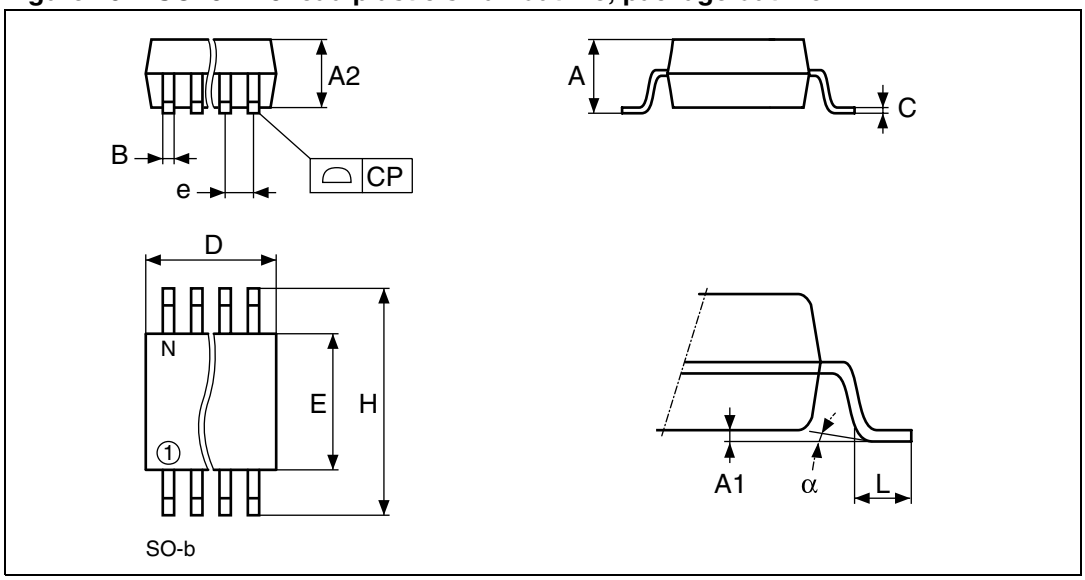
Symbol	Parameter[1]	Min	Typ	Max	Unit
t_F[2]	V_{PFD}(max) to V_{PFD}(min) V_{CC} fall time	300			µs
t_{FB}[3]	V_{PFD}(min) to V_{SS} V_{CC} fall time	10			µs
t_{PFD}	PFI to $\overline{PFO}$ propagation delay		15	25	µs
t_R	V_{PFD}(min) to V_{PFD}(max) V_{CC} rise time	10			µs
t_{RB}	V_{SS} to V_{PFD}(min) V_{CC} rise time	1			µs
t_{rec}[4]	Power up deselect time	40		200	ms

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 3.6 V (except where noted).
2. V_{PFD}(max) to V_{PFD}(min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD}(min).
3. V_{PFD}(min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.
4. Programmable (see *Table 7 on page 26*)

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 19. SO16 – 16-lead plastic small outline, package outline



Note: Drawing is not to scale.

Table 15. SO16 – 16-lead plastic small outline, package mechanical data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2			1.60			0.063
B		0.35	0.46		0.014	0.018
C		0.19	0.25		0.007	0.010
D		9.80	10.00		0.386	0.394
E		3.80	4.00		0.150	0.158
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
L		0.40	1.27		0.016	0.050
a		0°	8°		0°	8°
N		16			16	
CP			0.10			0.004

7 Part numbering

Table 16. Ordering information scheme

Example: M41ST 84W MQ 6 E

Device type

M41ST

Supply voltage and write protect voltage

84W = V_{CC} = 2.7 to 3.6 V; 2.55 V ≤ V_{PFD} ≤ 2.70 V

Package

MQ = SO16

Temperature range

6 = –40 to 85°C

Shipping method

For SO16:

E = ECOPACK® package, tubes

F = ECOPACK® package, tape & reel

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

8 Revision history

Table 17. Document revision history

Date	Revision	Changes
Aug-2000	1	First issue
24-Aug-2000	1.2	Block diagram added (*Figure 3*)
08-Sep-2000	1.3	SO16 package measures change
18-Dec-2000	2	Reformatted, TOC added, and PFI input leakage current added (*Table 12*)
18-Jun-2001	2.1	Addition of t_{rec} information, table changed, one added (*Table 3*, *7*); changes to PFI/$\overline{PFO}$ graphic (see *Figure 3*); change to DC and AC Characteristics, Order Information (*Table 12*, *2*, *16*); note added to “Setting Alarm Clock Registers” section; added temp./voltage info. to tables (*Table 11*, *12*, *13*, *2*, *14*); addition of Default Values (*Table 8*); textual improvements
25-Jun-2001	2.2	Special note added in *Section 3: Clock operation on page 17*
26-Jul20-01	3	Change in product maturity
07-Aug-2001	3.1	Improve text for “Setting the alarm clock” section
20-Aug-2001	3.2	Change V_{PFD} values in document
06-Sep-2001	3.3	DC characteristics V_{BAT} changed; PFI hysteresis (PFI rising) spec. added; and crystal electrical characteristics series resistance spec. changed (*Table 12*, *13*)
03-Dec-2001	3.4	Change READ/WRITE mode sequence drawings (*Figure 9*, *11*); change in V_{PFD} lower limit for 5V (M41ST84Y) part only (*Table 12*, *16*)
14-Jan-2002	3.5	Change series resistance (*Table 13*)
01-May-2002	3.6	Change t_{rec} definition (*Table 7*); modify reflow time and temperature footnote (*Table 9*)
03-Jul-2002	3.7	Modify DC and crystal electrical characteristics footnotes, default values (*Table 12*, *13*, *8*)
01-Aug-2002	3.8	Add marketing status (*Figure 1*; *Table 16*)
16-Jun-2003	4	New Si changes (*Table 14*, *6*, *7*, *8*)
15-Jun-2004	5	Reformatted; added Lead-free information; update characteristics (*Figure 12*; *Table 9*, *12*, *16*)
18-Oct-2004	6	Add marketing status (*Figure 1*; *Table 16*)
10-Jan-2006	7	Updated template, lead-free text, characteristics (*Figure 1*, *2*, *5*, *6*; *Table 1*, *2*, *6*, *8*, *9*, *10*, *11*, *12*, *13*, *14*, *16*)
28-Aug-2008	8	Reformatted document and modified title; updated cover page, *Figure 3*, *Table 13*, *16*, and *Section 6: Package mechanical data*.

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