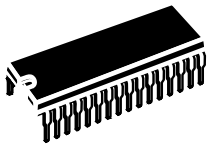
TDA9112A

High-end I2C controlled deflection processor for multisync monitor

Features

- General
  - Advanced I^2C bus controlled deflection processor dedicated for high-end CRT monitors
  - Single supply voltage 12 V
  - Very low jitter
  - DC/DC converter controller
  - Advanced EW drive
  - Advanced asymmetry corrections
  - Automatic multistandard synchronization
  - I^2C bus status register
- Horizontal section
  - 150 kHz maximum frequency
  - Corrections of geometric asymmetry: pin cushion asymmetry, parallelogram, separate top/bottom corner asymmetry
  - Tracking of asymmetry corrections with vertical size and position
- Vertical section
  - 200 Hz maximum frequency
  - Vertical ramp for DC-coupled output stage with adjustments of: C-correction, S-correction for super-flat CRT, vertical size, vertical position
- EW section
  - Symmetrical geometry corrections: pin cushion, keystone, top/bottom corners separately, S- and W-corrections
  - Horizontal size adjustment
  - Tracking of EW waveform with vertical size and position, horizontal size and frequency
- Dynamic correction section
  - Generates waveforms for dynamic corrections like focus, brightness uniformity
  - 1 output with vertical dynamic correction waveform, both polarities, tracking with vertical size and position



SDIP 32 (Shrink DIP package)

- DC/DC controller section
  - Step-up and step-down conversion modes
  - External sawtooth configuration
  - I^2C bus controlled output voltage
  - Synchronized on horizontal frequency with phase selection
  - Selectable polarity of drive signal
  - Protection at H unlock condition

Description

The TDA9112A is a monolithic integrated circuit assembled in a 32-pin shrink dual-in-line plastic package. This IC controls all the functions related to horizontal and vertical deflection in multimode or multi-frequency computer display monitors.

Combined with other ST components dedicated for CRT monitors (microcontroller, video preamplifier, video amplifier, OSD controller), the TDA9112A allows fully I^2C bus controlled computer display monitors to be built with a reduced number of external components.

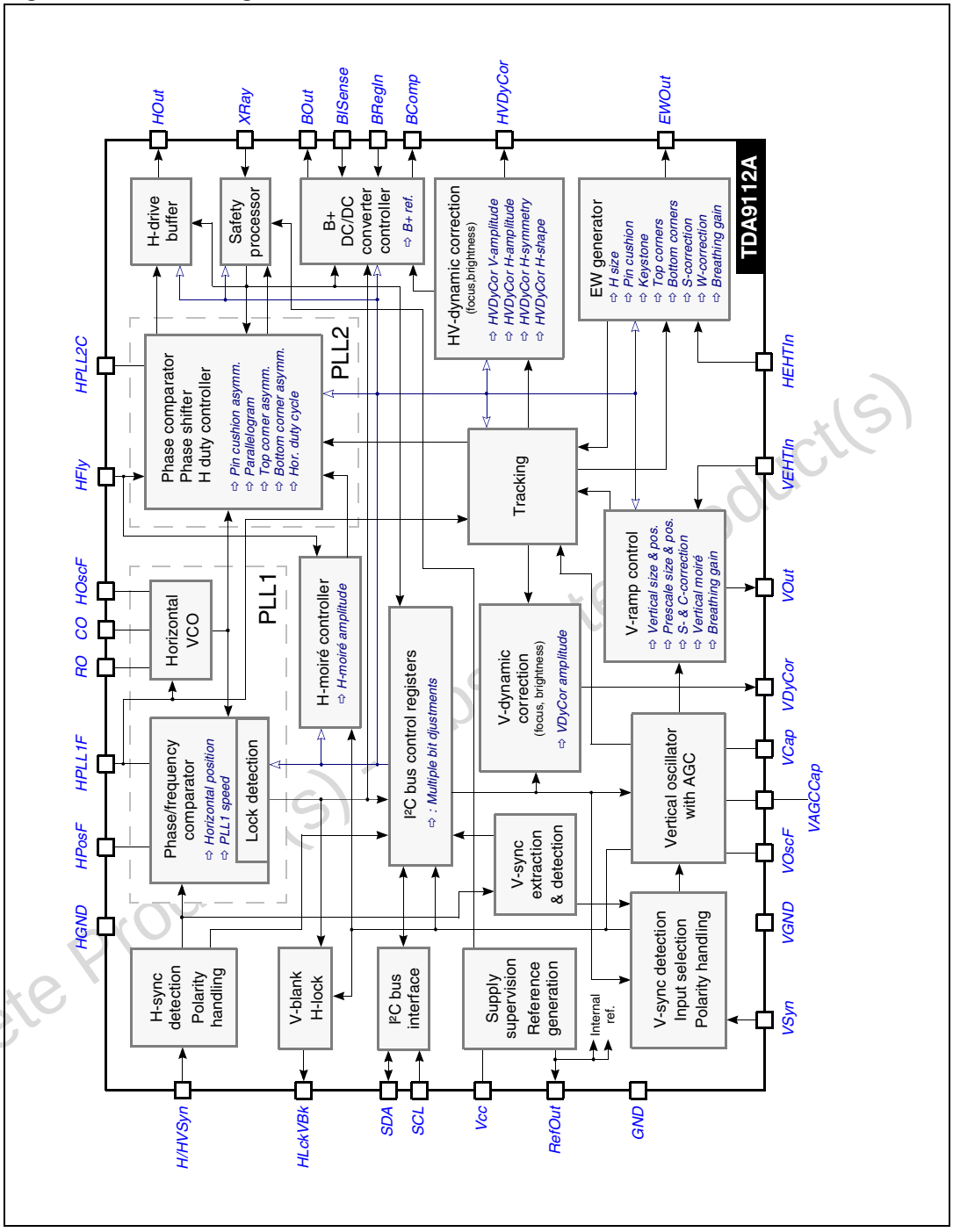
Table 1. Device summary

Order code	Package
TDA9112A	Tray

Contents

1 Block diagram

Figure 1. Block diagram



2 Package mechanical data

Figure 2. Pin configuration

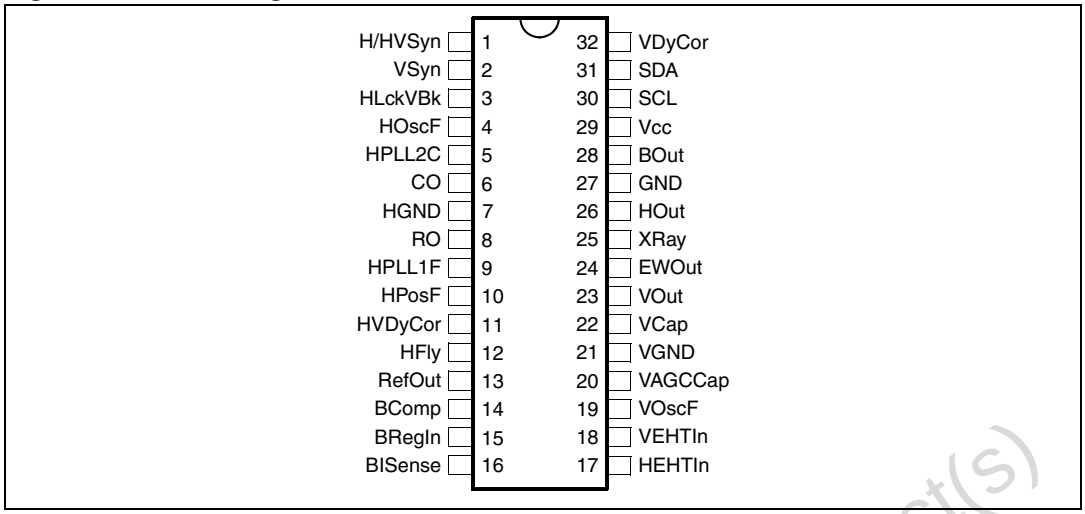


Table 2. Pin function reference

Pin	Name	Function
1	H/HVSyn	TTL compatible **H**orizontal **/ H**orizontal and **V**ertical **Sync**. input
2	VSyn	TTL compatible **V**ertical **Sync**. input
3	HLckVBk	**H**orizontal PLL1 **Lock** detection and **V**ertical early **B**lan**k**ing composite output
4	HOscF	High **H**orizontal **Osc**illator sawtooth threshold level **F**ilter input
5	HPLL2C	**H**orizontal **PLL2** loop **C**apacitive filter input
6	CO	Horizontal **O**scillator **C**apacitor input
7	HGND	**H**orizontal section **GrouND**
8	RO	Horizontal **O**scillator **R**esistor input
9	HPLL1F	**H**orizontal **PLL1** loop **F**ilter input
10	HPosF	**H**orizontal **Pos**ition **F**ilter and soft-start time constant capacitor input
11	HVDyCor	**H**orizontal and **V**ertical **Dy**namic **Cor**rection output
12	HFly	**H**orizontal **Fly**back input
13	RefOut	**Ref**erence voltage **Out**put
14	BComp	**B**+ DC/DC error amplifier (**Comp**ensation) output
15	BRegIn	**Reg**ulation feedback **In**put of the **B**+ DC/DC converter controller
16	BISense	**B**+ DC/DC converter current (**I**) **Sense** input
17	HEHTIn	**In**put for compensation of **H**orizontal amplitude versus **EHT** variation
18	VEHTIn	**In**put for compensation of **V**ertical amplitude versus **EHT** variation

Table 2. Pin function reference (continued)

Pin	Name	Function
19	VOscF	**V**ertical **Osc**illator sawtooth low threshold **F**ilter (capacitor to be connected to VGND)
20	VAGCCap	Input for storage **Cap**acitor for **A**utomatic **G**ain **C**ontrol loop in **V**ertical oscillator
21	VGND	**V**ertical section **G**rou**ND**
22	VCap	**V**ertical sawtooth generator **Cap**acitor
23	VOut	**V**ertical deflection drive **Out**put for a DC-coupled output stage
24	EWOut	**E/W Out**put
25	XRay	**X-Ray** protection input
26	HOut	**H**orizontal drive **Out**put
27	GND	Main **G**rou**ND**
28	BOut	**B**+ DC/DC converter controller **Out**put
29	Vcc	Supply voltage
30	SCL	I²C bus **S**erial **CL**ock Input
31	SDA	I²C bus **S**erial **DA**ta input/output
32	VDyCor	**V**ertical **Dy**namic **Cor**rection output

Table 3. Quick reference data

Characteristic	Value	Unit
General		
Package	SDIP 32	
Supply voltage	12	V
Supply current	65	mA
Application category	High-end	
Means of control • Maximum clock frequency	I²C bus • 400	kHz
EW drive	Yes	
DC/DC converter controller	Yes	
Horizontal section		
Frequency range	15 to 150	kHz
Autosync frequency ratio (can be enlarged in application)	4.28	
Positive • Negative polarity of horizontal sync signal • Automatic adaptation	Yes • Yes • Yes	
Duty cycle range of the drive signal	30 to 65	%
Position adjustment range with respect to H period	±10	%
Soft start • Soft stop feature	Yes • Yes	
Hardware • Software PLL lock indication	Yes • Yes	

Table 3. Quick reference data (continued)

Characteristic	Value	Unit
Parallelogram	Yes	
Pin cushion asymmetry correction (also called Side pin balance)	Yes	
Top • Bottom • Common corner asymmetry correction	Yes • Yes • No	
Tracking of asymmetry corrections with vertical size & position	Yes	
Horizontal moiré cancellation (int.) for Combined • Separated architecture	Yes • Yes	
Vertical section		
Frequency range	35 to 200	Hz
Autosync frequency range (150nF at VCap and 470nF at VAGCCap)	50 to 180	Hz
Positive • Negative polarity of vertical sync signal • Automatic adaptation	Yes • Yes • Yes	
S-correction • C-correction • Super-flat tube characteristic	Yes • Yes • Yes	
Vertical size • Vertical position • Prescale adjustments	Yes • Yes • Yes	
Vertical moiré cancellation (internal)	Yes	
EHT breathing compensation • With I²C bus gain control	Yes • Yes	
EW section		
Pin cushion correction	Yes	
Keystone correction	Yes	
Top • Bottom • Common corner correction	Yes • Yes • No	
S-correction • W-correction	Yes • Yes	
Horizontal size adjustment	Yes	
Tracking of EW waveform with Frequency • Vertical size & position	Yes • Yes	
EHT breathing compensation • With I²C bus gain control	Yes • Yes	
Dynamic correction section (dyn. focus, dyn. brightness,...)		
Vertical dynamic correction output VDyCor • Positive or negative polarity	Yes • Yes	
Horizontal dynamic correction output HDyCor	No	
Composite HV dynamic correction output HVDyCor • Positive or negative polarity	Yes • Yes	
Shape control on H waveform component of HVDyCor output	Yes	
Tracking of horizontal waveform component with Horizontal size • EHT	Yes • No	
Tracking of vertical waveforms (component) with V. size & position	Yes	
DC • DC controller section		
Step-up • Step-down conversion mode	Yes • Yes	
Internal • External sawtooth configuration	No • Yes	

Table 3. Quick reference data (continued)

Characteristic	Value	Unit
Bus-controlled output voltage • Inhibition at H unlock	Yes • Yes	
Mute • Soft start • Soft stop feature	Yes • Yes • Yes	
Positive (N-MOS) • Negative(P-MOS) polarity of BOut signal	Yes • Yes	
Phase selection • Max current selection • Frequency selection	Yes • Yes • Yes	

2.1 Environmentally-friendly packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance.

ECOPACK specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK is an ST trademark.

3 Absolute maximum ratings

All voltages are given with respect to ground.

Currents flowing from the device (sourced) are signed negative. Currents flowing to the device are signed positive.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
V_{CC}	Supply voltage (pin Vcc)	-0.4	13.5	V
$V_{(pin)}$	Pins HEHTIn, VEHTIn, XRay, HOut, BOut Pins H/HVSyn, VSyn, SCL, SDA Pins HLckVBk, CO, RO, HPLL1F, HPosF, HVDyCor, BRegIn, BISense, VAGCCap, VCap, VDyCor, HOscF, VOscF Pin HPLL2C Pin HFly	-0.4 -0.4 -0.4 -0.4 -0.4	*VCC* 5.5 *VRefO* *VRefO*/2 *VRefO*	V V V V V
V_{ESD}	ESD susceptibility (human body model: discharge of 100pF through 1.5kΩ)	-2000	2000	V
T_{stg}	Storage temperature	-40	150	°C
T_j	Junction temperature		150	°C

4 Electrical parameters and operating conditions

Medium (middle) value of an I²C bus control or adjustment register composed of bits D0, D1,...,Dn is the one having Dn at "1" and all other bits at "0". Minimum value is the one with all bits at 0, maximum value is the one with all at "1".

Currents flowing from the device (sourced) are signed negative. Currents flowing to the device are signed positive.

T_H is period of horizontal deflection.

4.1 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
T_{amb}	Operating ambient temperature	0		70	°C
$R_{th(j-a)}$	Junction-ambience thermal resistance		65		°C/W

4.2 Supply and reference voltages

T_{amb} = 25 °C

Table 6. Supply and reference voltages

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
V_{CC}	Supply voltage at Vcc pin		10.8	12	13.2	V
I_{CC}	Supply current to Vcc pin	*VCC* = 12 V		65		mA
V_{RefO}	Reference output voltage at RefOut pin	*VCC* = 12 V, *IRefO*= -2 mA	7.65	7.9	8.2	V
I_{RefO}	Current capability of RefOut output		-5		0	mA

4.3 Synchronization inputs

Vcc = 12 V, T_{amb} = 25 °C

Table 7. Synchronization inputs

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
$V_{LoH/HVSyn}$	LOW level voltage on *H/HVSyn*		0		0.8	V
$V_{HiH/HVSyn}$	HIGH level voltage on *H/HVSyn*		2.2		5	V
V_{LoVSyn}	LOW level voltage on *VSyn*		0		0.8	V
V_{HiVSyn}	HIGH level voltage on *VSyn*		2.2		5	V
R_{PdSyn}	Internal pull-down on *H/HVSyn*, *VSyn*		100	175	250	kΩ
$t_{PulseHSyn}$	H sync. pulse duration on *H/HVSyn* pin		0.5			µs
$t_{PulseHSyn}/T_H$	Proportion of H sync pulse to H period	Pin *H/HVSyn*			0.2	
$t_{PulseVSyn}$	V sync. pulse duration	Pins *H/HVSyn*, *VSyn*	0.5		750	µs
$t_{PulseVSyn}/T_V$	Proportion of V sync pulse to V period	Pins *H/HVSyn*, *VSyn*			0.15	
t_{extrV}/T_H	Proportion of H sync pulse length to H period for extraction as V sync pulse	Pin *H/HVSyn*, cap. on pin *CO* = 820pF	0.21	0.35		
$t_{HPolDet}$	Polarity detection time (after change)	Pin *H/HVSyn*	0.75			ms

4.4 Horizontal section

Table 8. Horizontal section (Vcc = 12 V, T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
PLL1						
I_{RO}	Current load on *RO* pin				1.5	mA
C_{CO}	Capacitance on *CO* pin		390			pF
f_{HO}	Frequency of hor. oscillator				150	kHz
$f_{HO(0)}$	Free-running frequency of hor. oscill.(1)	R_{RO}=5.23 kΩ, C_{CO}=820 pF	27	28.5	29.9	kHz
f_{HOCapt}	Hor. PLL1 capture frequency (2)	*fHO(0)* = 28.5 kHz	29		122	kHz
$\frac{\Delta f_{HO(0)}}{f_{HO(0)} \cdot \Delta T}$	Temperature drift of free-running freq.(3)			-150		ppm/°C
$\Delta f_{HO}/\Delta V_{HO}$	Average horizontal oscillator sensitivity	*fHO(0)* = 28.5 kHz		20.2		kHz/V
V_{HO}	H. oscill. control voltage on pin *HPLL1F*	*VRefO*=8 V	1.4		6.0	V
$V_{HOThrfr}$	Threshold on H. oscill. control voltage on *HPLL1F* pin for tracking of EW with freq.	*VRefO*=8 V		5.0		V
V_{HPosF}	Control voltage on *HPosF* pin	*HPOS* (Sadh): 11111111b 10000000b 00000000b		 2.8 3.4 4.0		 V V V
$V_{HOThrLo}$	Bottom of hor. oscillator sawtooth			1.6		V
$V_{HOThrHi}$	Top of hor. oscillator sawtooth			6.4		V
PLL2						
$R_{In(HFly)}$	Input impedance on *HFly* input	$V_{(HFly)}$ > *VThrHFly*(4)	300	500	700	Ω
I_{InHFly}	Current into *HFly* input	At top of H flyback pulse			5	mA
$V_{ThrHFly}$	Voltage threshold on *HFly* input		0.5	0.6		V
$V_{S(0)}$	H flyback lock middle point(5)	No PLL2 phase modulation		4.0		V
$V_{BotHPLL2C}$	Low clamping voltage on *HPLL2C* pin(6)			1.6		V
$V_{TopHPLL2C}$	High clamping voltage on *HPLL2C* pin			4.0		V
$t_{ph}(min)/T_H$	Min. advance of H-drive OFF before middle of H flyback(7)	Null asym. correction		0		%
$t_{ph}(max)/T_H$	Max. advance of H-drive OFF before middle of H flyback(8)	Null asym. correction		44		%
H-drive output on pin *HOut*						
I_{HOut}	Current into *HOut* output	Output driven LOW			30	mA
t_{Hoff}/T_H	Duty cycle of H-drive signal	f_H = 31 kHz; *HDUTY* (Sadh): x1111111b x0000000b Soft-start/Soft-stop value		 27 65 85		 % % %

Table 8. Horizontal section (Vcc = 12 V, T_{amb} = 25 °C) (continued)

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
Picture geometry corrections through PLL1 & PLL2						
t_{Hph}/T_H	Hor. VCO phase vs. sync signal (via PLL1)	*HPOS* (Sadh): 11111111b 10000000b 00000000b		 +11 0 -11		 % % %
t_{PCAC}/T_H	Contribution of pin cushion asymmetry correction to phase of H-drive vs. static phase (via PLL2), measured in corners	*PCAC* (Sadh) full span(9) *VPOS* at medium *VSIZE* at minimum *VSIZE* at medium *VSIZE* at maximum		 ±0.9 ±1.6 ±2.6		 % % %
t_{ParalC}/T_H	Contribution of parallelogram correction to phase of H-drive vs. static phase (via PLL2), measured in corners	*PARAL* (Sadh) full span *VPOS* at medium *VSIZE* at minimum *VSIZE* at medium *VSIZE* at maximum		 ±1.4 ±1.9 ±2.4		 % % %
t_{TCAC}/T_H	Contribution of top corner asymmetry correction to phase of H-drive vs. static phase (via PLL2), measured in corners	*TCAC* (Sadh) full span *VPOS* at medium *VSIZE* at minimum *VSIZE* at medium *VSIZE* at maximum		 ±0.4 ±1.4 ±3.5		 % % %
t_{BCAC}/T_H	Contribution of bottom corner asymmetry correction to phase of H-drive vs. static phase (via PLL2), measured in corners	*BCAC* (Sadh) full span *VPOS* at medium *VSIZE* at minimum *VSIZE* at medium *VSIZE* at maximum		 ±0.4 ±1.4 ±3.5		 % % %

1. Frequency at no sync signal condition. For correct operation, the frequency of the sync signal applied must always be higher than the free-running frequency. The application must consider the spread of values of real electrical components in R_{RO} and C_{CO} positions so as to always meet this condition. The formula to calculate the free-running frequency is *fHO(0)*=0.122/(R_{RO} C_{CO})
2. This capture range can be enlarged by external circuitry.
3. Evaluated and figured out during the device qualification phase. Informative. Not tested on every single unit.
4. Base of NPN transistor with emitter to ground is internally connected on pin *HFly* through a series resistance of about 500 Ω and a resistance to ground of about 20 kΩ
5. Internal threshold.
6. The voltage on *HPLL2C* pin corresponds to immediate phase of leading edge of H-drive signal on *HOut* pin with respect to internal horizontal oscillator sawtooth. It must be between the two clamping levels given. Voltage equal to one of the clamping values indicates a marginal operation of PLL2 or non-locked state.
7. The *tph(min)* parameter is fixed by the application. For correct operation of asymmetry corrections through dynamic phase modulation, this minimum must be increased by maximum of the total dynamic phase required in the direction leading to bending of corners to the left. Marginal situation is indicated by reach of *VTopHPLL2C* high clamping level by waveform on pin *HPLL2C*.
8. The *tph(max)* parameter is fixed by the application. For correct operation of asymmetry corrections through dynamic phase modulation, this maximum must be reduced by maximum of the total dynamic phase required in the direction leading to bending of corners to the right. Marginal situation is indicated by reach of *VBotHPLL2C* low clamping level by waveform on pin *HPLL2C*.
9. All other dynamic phase corrections of picture asymmetry set to their neutral (medium) positions.

4.5 Vertical section

Table 9. Vertical section (Vcc = 12 V, Tamb = 25 °C)

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
AGC-controlled vertical oscillator sawtooth; *VRefO* = 8V						
$R_{L(VAGCCap)}$	Ext. load resistance on *VAGCCap* pin(1)	$\Delta V_{amp}/V_{amp}(R=\infty) \leq 1\%$	65			MΩ
V_{VOB}	Sawtooth bottom voltage on *VCap* pin(2)	No load on *VOscF* pin		2		V
V_{VOTref}	Sawtooth top voltage internal reference			5		V
V_{VOT}	Sawtooth top voltage on *VCap* pin	AGC loop stabilized		5		V
t_{VODis}	Sawtooth Discharge time	C_{VCap}=150nF		80		µs
$f_{VO(0)}$	Free-running frequency	C_{VCap}=150nF		100		Hz
f_{VOCapt}	AGC loop capture frequency	C_{VCap}=150nF	50		185	Hz
$\frac{\Delta V_{VOdev}}{V_{VOamp}}$	Sawtooth non-linearity(3)	AGC loop stabilized(4)		0.5		%
$\frac{\Delta V_{VOamp}}{V_{VOamp} \cdot \Delta f_{VO}}$	Frequency drift of sawtooth amplitude(5) (6)	AGC loop stabilized $fVOCapt_{(min)} \leq f_{VO} \leq fVOCapt_{(max)}$		200		ppm/Hz
Vertical output drive signal (on pin *VOut*); *VRefO* = 8V						
V_{midref}	Internal reference for vertical sawtooth middle point			3.5		V
$V_{mid(VOut)}$	Middle point on *VOut* sawtooth	*VPOS* (Sadh):(7) x0000000b x1000000b x1111111b *VPOF* (Sadh):(8) x0000000b x1000000b x1111111b	3.65	 3.1 3.45 3.8 3.3 3.45 3.6	3.3	 V V V V V V
V_{amp}	Amplitude of *VOut* sawtooth (peak-to-peak voltage)	*VSIZE* (Sadh):(9) x0000000b x1000000b x1111111b *VSAG* (Sadh):(10) x0000000b x1000000b x1111111b	3.5	 2.25 3.0 3.75 2 2.5 3.0	2.5	 V V V V V V
$V_{offVOut}$	Level on *VOut* pin at V-drive "off"	I²C bus bit *VOutEn* at 0		4.0		V
I_{VOut}	Current delivered by *VOut* output		-5		0.25	mA
V_{SCor}/V_{amp}	S-correction range	AGC loop stabilized(11) t_{VR}=1/4 T_{VR} t_{VR}=3/4 T_{VR}		 -4.5 +4.5		 % %

Table 9. Vertical section (Vcc = 12 V, Tamb = 25 °C) (continued)

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
V_{CCor}/V_{amp}	C-correction range	(12)AGC loop stabilized t_{VR}=1/2 T_{VR}(13) *CCOR*(Sadh): x0000000b x1000000b x1111111b		 -2.5 0 +2.5		 % % %
V_{VEHT}	Control input voltage range on *VEHTIn* pin		1	4	6	V
$V_{VEHTnull}$	Neutral point on breathing characteristics(14)			4.0		V
$\frac{\Delta V_{amp}}{V_{amp} \cdot \Delta V_{VEHT}}$	Breathing compensation	*VRefO* < *VVEHT* < *VCC* $VVEHT_{(min)} \leq VVEHT \leq VVEHT_{(max)}$: *VEHTG* (Sadh): x0000000b x1000000b x1111111b		0 5 0 -5		%/V %/V %/V %/V

1. Value of acceptable cumulated parasitic load resistance due to humidity, AGC storage capacitor leakage, etc., for less than 1% of *Vamp* change.
2. The threshold for *VVOB* is generated internally and routed to *VOscF* pin. Any DC current on this pin will influence the value of *VVOB*.
3. If *VVEHT*=*VVEHTnull* or *VHEHT*=*VHEHTnull*, respectively, the influence of *VVEHT* on vertical drive amplitude or the influence of *VHEHT* on EW drive signal, respectively, is null.
4. Maximum of deviation from an ideally linear sawtooth ramp at null S-correction (*SCOR* at 0000000b) and null C-correction (*CCOR* at 1000000b). The same rate applies to V-drive signal on *VOut* pin, no effect on *EWOut*.
5. V_{VOamp} = *VVOT* - *VVOB*
6. Only the top of the saw tooth drifts. The same rate applies to V-drive signal on *VOut* pin.
7. *VPOS* at medium value 1000000b.
8. *VPOF* at medium value 1000000b.
9. *VSIZE* at medium value 1000000b.
10. *VSAG* at maximum value 1111111b.
11. Informative, not tested on each unit.
12. Maximum S-correction (*SCOR* at x1111111b), null C-correction (*CCOR* at 1000000b)
13. Null S-correction (*SCOR* at 0000000b).
14. "t_{VR}" is time from the beginning of vertical ramp of V-drive signal on *VOut* pin. "T_{VR}" is the duration of this ramp.

4.6 EW drive section

Table 10. EW drive section (V_{CC} = 12 V, T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
V_{EW}	Output voltage on *EWOut* pin		1.8		6.5	V
I_{EWOut}	Current delivered by *EWOut* output		-1.5		0.1	mA
V_{HEHT}	Control voltage range on *HEHTIn* pin		1		6	V
$V_{HEHTnull}$	Neutral point on breathing characteristics.			4.0		V
V_{EW-DC}	DC component of the EW-drive signal on *EWOut* pin	(1) (2) (3) (4) (5) (6) *EWTrHFr*=0 or *VHO*>*VHOThrfr* *HSIZE* (Sadh): 00000000b 10000000b 11111111b		 2 3.25 4.5		 V V V
$V_{EW-base}$	DC reference for the EW-drive signal on *EWOut* pin			2		V
$\frac{\Delta V_{EW-DC}}{\Delta V_{HEHT}}$	Breathing compensation on DC component of the EW-drive signal(7)	*VRefO* < *VHEHT* < *VCC* $VHEHT_{(min)} \leq VHEHT \leq VHEHT_{(max)}$: *HEHTG* (Sadh): x0000000b x1000000b x1111111b		0 0 -0.25 0 +0.25		V/V V/V V/V V/V V/V
$\frac{\Delta V_{EW-DC}}{V_{EW-DC} \cdot \Delta T}$	Temperature drift of DC component of the EW-drive signal	(8)		100		ppm/°C
V_{EW-PCC}	Pin cushion correction component of the EW-drive signal	*VSIZE* at maximum *PCC* (Sadh): x0000000b x1000000b x1111111b Tracking with *VSIZE*: *PCC* at x1000000b *VSIZE* (Sadh): x0000000b x1000000b		 0 0.75 1.5 0.25 0.5		 V V V V V
$\frac{V_{EW-PCC}[t_{vr}=0]}{V_{EW-PCC}[t_{vr}=T_{VR}]}$	Tracking of PCC component of the EW-drive signal with vertical position adjustment	(9) *PCC* at x1111111b *VPOS* (Sadh): x0000000b x1111111b		 0.5 2.0		
V_{EW-Key}	Keystone correction component of the EW-drive signal	(10) *KEYST* (Sadh): x0000000b x1111111b		 0.4 -0.4		 V V
$V_{EW-TCor}$	Top corner correction component of the EW-drive signal	(11) *TCC* (Sadh): x0000000b x1000000b x1111111b		 -1.4 0 +1.4		 V V V

Table 10. EW drive section (V_{CC} = 12 V, T_{amb} = 25 °C) (continued)

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
$V_{EW-BCor}$	Bottom corner correction component of the EW-drive signal	(12) (13) (14) *BCC* (Sadh): x0000000b x1000000b x1111111b		 -1.4 0 +1.4		 V V V
V_{EW-S}	Pin Cushion S correction component of EW-drive signal	(15) *EWSC* (Sadh): x0000000b x1000000b x1111111b		 -0.3 0 0.3		 V V V
V_{EW-W}	Pin Cushion W correction component of EW-drive signal	(16) (17) *EWWC* (Sadh): x0000000b x1000000b x1111111b		 -0.1 0 0.1		 V V V
$\frac{\Delta V_{EW-AC}}{V_{EW-AC}[f_{max}] \cdot \Delta V_{HO}}$	Tracking of AC component of EW-drive signal with horizontal frequency(18) (19)	I²C bit *EWTrHFr*=1 *VHO*>*VHOThrfr* *VHO*(min)≤*VHO*≤*VHOThrfr*		 0 20		 %/V %/V
$\frac{\Delta V_{EW-DC}}{V_{EW-DC}[span] \cdot \Delta V_{HO}}$	Tracking of DC component of EW-drive signal with horizontal frequency(20)	I²C bit *EWTrHFr*=1 *VHO*>*VHOThrfr* *VHO*(min)≤*VHO*≤*VHOThrfr*		 0 20		 %/V %/V
$\frac{V_{EW-AC}}{V_{EW-AC}[HSIZE_{max}]}$	Tracking of AC component of EW-drive signal with horizontal size	I²C bit *EWTrHSize*=0 *HSIZE* (Sadh): 00000000b 10000000b 11111111b		 138 119 100		 % % %
$\frac{\Delta V_{EW-AC}}{V_{EW-AC} \cdot \Delta V_{HEHT}}$	Breathing compensation on AC component of the EW-drive signal(21)	*VRefO* < *VHEHT* < *VCC* *VHEHT*(min)≤*VHEHT*≤*VHEHT*(max) : *HEHTG* (Sadh): 0000000b 1000000b 1111111b		0 3.5 0 -3.5		%/V %/V %/V %/V

1. *KEYST* at medium (neutral) value.
2. *TCC* at medium (neutral) value.
3. *BCC* at medium (neutral) value.
4. *PCC* at minimum value.
5. *VPOS* at medium (neutral) value.
6. *HSIZE* I²C field at maximum value.
7. Defined as difference of (voltage at t_{VR}=1/4 T_{VR}) minus (voltage at t_{VR}=3/4 T_{VR}).
8. Informative, not tested on each unit.
9. Ratio "A/B"of parabola component voltage at t_{VR}=0 versus parabola component voltage at t_{VR}=T_{VR}. See *Figure 4*.
10. Difference (voltage at t_{VR}=0) minus (voltage at t_{VR}=T_{VR}).
11. Defined as difference of (voltage at t_{VR}=0) minus (voltage at t_{VR}=1/2 T_{VR}).
12. Defined as difference of (voltage at t_{VR}=T_{VR}) minus (voltage at t_{VR}=1/2 T_{VR}).
13. *VSIZE* at maximum value.
14. *EWWC* at medium (neutral) value.
15. *VHEHT*>*VRefO*, *VVEHT*>*VRefO*

16. Defined as difference of (voltage at t_{VR}=1/2 T_{VR}) minus (voltage at t_{VR}=1/4 T_{VR}).
17. *EWSC* at medium (neutral) value.
18. More precisely tracking with voltage on *HPLL1F* pin which itself depends on frequency at a rate given by external components on PLL1 pins
19. *VEW-DC*[span] = *VEW-DC*[*VHO*>*VHOThrfr*] - *VEW-DC*[*HSIZE*=0000000b].
    $V_{EW-AC}[f_{max}] = V_{EW-AC}$[*VHO*>*VHOThrfr*].
20. *VEW-DC* is defined as voltage at t_{VR}=1/2 T_{VR}.
21. V_{EW-AC} is defined as overall peak-to-peak value between t_{VR}=0 and t_{VR}=T_{VR} of all components other than *VEW-DC* (contribution of PCC, keystone correction, corner corrections and S- and W-corrections).

4.7 Dynamic correction outputs section

Table 11. Dynamic correction outputs section (V_{CC} = 12 V, T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
Composite Horizontal and Vertical Dynamic Correction output *HVDyCor*						
$I_{HVDyCor}$	Current delivered by *HVDyCor* output		-2		1	mA
V_{HVD-DC}	DC component of the drive signal on *HVDyCor* output	*HVDyCorPol* = 0 *HVDyCorPol* = 1	TBD TBD	2.1 7.30	TBD TBD	V V
$\frac{\Delta V_{HVD-DC}}{V_{HVD-DC} \cdot \Delta T}$	Temperature drift of DC component of the drive signal on *HVDyCor*			200		ppm/°C
V_{HVD-H}	Amplitude of H-component of the drive signal on *HVDyCor* output	(1) (2) *HDyCorTr* = 0 *HVDC-HSHAP* = min *HVDC-HAMP* (Sadh): x0000000b x1000000b x1111111b *HVDC-HSHAP* = max *HVDC-HAMP* (Sadh): x0000000b x1000000b x1111111b		 4.8 1.8 1 4.5 1.5 1		 V V V V V V
$S_{HVDC-HSHAP}$	Power index of the H-component of the drive signal on *HVDyCor* output	(3) *HVDC-HSHAP* (Sadh) x0000000b x1000000b x1111111b		 2 2.8 4		
$\frac{V_{HVD-H}[TrHSOn]}{V_{HVD-H}[TrHSOff]}$	Impact of horizontal size adjustment on *HVDyCor* H-parabola component (tracking)(4)	*HSIZE* (Sadh): 00000000b 11111111b		 1		
$t_{HVD-Hoffset}/T_H$	Offset (phase) of H-parabola component of the drive signal on *HVDyCor* output (5)	*HVDC-HPH* (Sadh): x0000000b x1000000b (6) x1111111b		 +24.5 0 -24.5		 % % %
$t_{HVD-Hflat}$	Duration of the flat part at the start of H-parabola component of the drive signal on *HVDyCor* output	*fHO*=31kHz *HDCFlatEn* = 0 or/and *HDyCorPh* = 0		850		ns
		HDCFlatEn = 1 *HDyCorPh* = 1		(7)		
V_{HVD-V}	Amplitude of V-parabola component of the drive signal on *HVDyCor* output	(8) *VSIZE* at x1000000b *HVDC-VAMP* (Sadh): x0000000b x1000000b x1111111b *HVDC-VAMP* at max.: *VSIZE* (Sadh): x0000000b x1111111b		 0 0.6 1.2 0.7 1.9		 V V V V V

Table 11. Dynamic correction outputs section (V_{CC} = 12 V, T_{amb} = 25 °C) (continued)

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
$\frac{V_{HVD-V}[t_{VR}=0]}{V_{HVD-V}[t_{VR}=T_{VR}]}$	Tracking of V-parabola component of the drive signal on *HVDyCor* output with vertical position	*HVDC-VAMP* at max.: *VPOS* (Sadh): x0000000b x1111111b		 0.5 2.0		
Vertical Dynamic Correction output *VDyCor*						
I_{VDyCor}	Current delivered by *VDyCor* output		-1.5		0.1	mA
V_{VD-DC}	DC component of the drive signal on *VDyCor* output	$R_{L(VDyCor)}$=10 kΩ		4		V
V_{VD-V}	Amplitude of V-parabola on *VDyCor* output(9)	*VSIZE* at medium *VDC-AMP* (Sadh): x0000000b x1000000b x1111111b *VDC-AMP* at maximum *VSIZE* (Sadh): x0000000b x1111111b		 0 0.5 1 0.6 1.6		 V V V V V
$\frac{V_{VD-V}[t_{VR}=0]}{V_{VD-V}[t_{VR}=T_{VR}]}$	Tracking of V-parabola on *VDyCor* output with vertical position (10)	*VDC-AMP* at maximum *VPOS* (Sadh): x0000000b x1111111b		 0.5 2.0		

1. *HVDC-VAMP* at minimum.
2. *HVDC-HPH* at medium.
3. Value gives the shape characteristics of the H-component. Refer to *Figure 19*.
4. Ratio of the amplitude at *HDyCorTr*=1 to the amplitude at *HDyCorTr*=0 (refer to chapter "I²C bus control register map") as a quadratic function of horizontal size adjustment.
5. Refer to *Figure 18*.
6. Taken for reference at given position of *HDyCorPh* flag.
7. The flat part begins at the start of fly-back and ends at the same moment as for combination *HDCFlatEn* = 0, *HDyCorPh* = 1. Refer to *Figure 18*.
8. (1.38)*SHVDC-HSHAP*
9. Unsigned value. Polarity selection by *VDyCorPol* I²C bus bit. Refer to section I²C bus control register map.
10. Ratio "A/B"of vertical parabola component voltage at t_{VR}=0 versus vertical parabola component voltage at t_{VR}=T_{VR}.

4.8 DC/DC controller section

Table 12. DC/DC controller section (V_{CC} = 12 V, T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Units
			Min.	Typ.	Max.	
R_{B+FB}	Ext. resistance applied between *BComp* output and *BRegIn* input		5			kΩ
A_{OLG}	Open loop gain of error amplifier on *BRegIn* input	Low frequency		100		dB
f_{UGBW}	Unity gain bandwidth of error amplifier on *BRegIn* input			6		MHz
I_{RI}	Bias current delivered by *BRegIn*			-0.2		µA
I_{BComp}	Output current capability of *BComp* output.	*BOut* enabled *BOut* disabled(1)	-0.5	 0.5	2.0	mA mA
$A_{BISense}$	Voltage gain on *BISense* input			3		
$V_{ThrBIsCurr}$	Threshold voltage on *BISense* input corresponding to current limitation	*ThrBIsense* = 0 *ThrBIsense* = 1	TBD TBD	2.1 1.2		V
$I_{BISense}$	Bias current delivered by *BISense*			-1		µA
t_{BOn}	Conduction time of the power transistor				T_H - 300ns	
I_{BOut}	Output current capability of *BOut* output		0		10	mA
V_{BOSat}	Saturation voltage of the internal output transistor on *BOut*	*IBOut*=10mA		0.25		V
V_{BReg}	Regulation reference for *BRegIn* voltage(2)	*VRefO*=8V *BREF* (Sadh): x0000000b x1000000b x1111111b		 3.8 4.9 6.0		 V V V
$t_{BTrigDel}/T_H$	Delay of *BOut* “Off-to-On” edge after middle of flyback pulse(3)	*BOutPh* = 0 and *BOHEdge* = 0		16		%

1. A current sink is provided by the *BComp* output while *BOut* is disabled.
2. Internal reference related to *VRefO*. The same values to be found on pin *BRegIn*, while regulation loop is stabilized.
3. Only applies to configuration specified in "Test conditions" column, i.e. synchronization of *BOut* “Off-to-On” edge with horizontal fly-back signal. Refer to chapter "DC/DC controller" for more details.

4.9 Miscellaneous

Table 13. Miscellaneous (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
Vertical blanking and horizontal lock indication composite output HLckVBk						
$I_{SinkLckBk}$	Sink current to *HLckVBk* pin	(1)		100		µA

Table 13. Miscellaneous (V_{CC} = 12V, T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{OLckBk}	Output voltage on *HLckVBk* output	V. blank / H. lock No / Yes Yes / Yes No / No Yes / No		0.1 1.1 5 6		 V V V V
Horizontal moiré canceller						
$\frac{\Delta T_{H(H-moire)}}{T_H}$	Modulation of T_H by H. moiré function	*HMoiréMode* = 0 *HMOIRE* (Sadh): x0000000b x1111111b *HMoiréMode* = 1 *HMOIRE* (Sadh): x0000000b x1111111b		 0 0.02 0 0.04		 % % % %
Vertical moiré canceller						
$V_{V\text{-}moiré}$	Amplitude of modulation of V-drive signal on *VOut* pin by vertical moiré.	*VMOIRE* (Sadh): x0000000b x1111111b		 0 3		 mV mV
Protection functions						
$V_{ThrXRay}$	Input threshold on *XRay* input (2)		*VRefO* -10mV	*VRefO*	*VRefO* +10mV	
$t_{XRayDelay}$	Delay time between XRay detection event and protection action		T_H		2TH	
$V_{CCXRayEn}$	Minimum *VCC* value for operation of XRay detection and protection(3)			10.2	10.8	V
V_{CCEn}	*VCC* value for start of operation at *VCC* ramp-up(4)			8.0		V
V_{CCDis}	*VCC* value for stop of operation at *VCC* ramp-down			6.8		V
Control voltages on *HPosF* pin and *VCC* for Soft start/stop operation(5)						
V_{HOn}	Threshold for start/stop of H-drive signal			1		V
V_{BOn}	Threshold for start/stop of B-drive signal			1.7		V
V_{HBNorm}	Threshold for full operation duty cycle of H-drive and B-drive signals			2.4		
V_{CCStop}	Minimum supply voltage when voltage on *HPosF* pin reaches *VHOn* threshold(6)(6)			4.8		

1. Current sunk by the pin if the external voltage is higher than one the circuit tries to force.
2. See *VRefO* in *Section 4.2*.
3. When *VCC* is below *VCCXRayEn* XRay detection and protection are disabled.
4. In the regions of *VCC* where the device's operation is disabled, the H-drive, V-drive and B+-drive signals on *HOut*, *VOut* and *BOut* pins, resp., are inhibited, the I²C bus does not accept any data and the *XRayAlarm* flag is reset. Also see *Figure 12*.
5. See *Figure 12*.
6. Minimum momentary supply voltage to ensure a correct performance of Soft stop function at *VCC* fall down is defined at the moment when the voltage on *HPosF* pin reaches *VHOn* threshold.

5 Typical output waveforms

Table 14. Typical output waveforms(1)

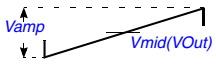
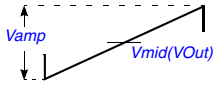
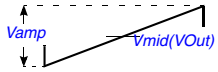
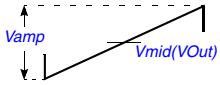
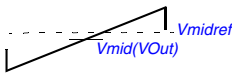
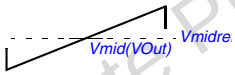
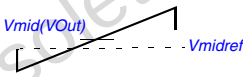
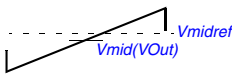
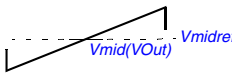
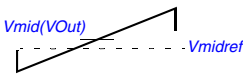
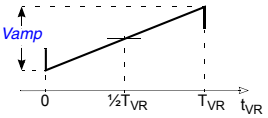
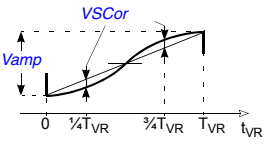
Function	Sad	Pin	Byte	Waveform	Effect on screen
Vertical Size		*VOut* ()	x0000000		
			x1111111		
Vertical Size After Gain		*VOut* ()	x0000000		
			x1111111		
Vertical Position		*VOut* ()	x0000000		
			x1000000		
			x1111111		
Vertical Position Offset		*VOut* ()	x0000000		
			x1000000		
			x1111111		
S-correction		*VOut* ()	x0000000: Null		
			x1111111: Max.		

Table 14. Typical output waveforms(1) (continued)

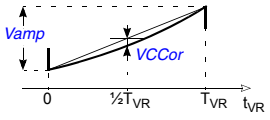
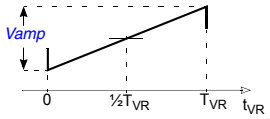
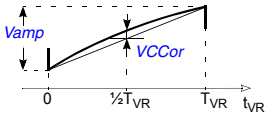
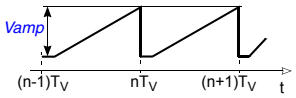
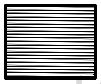
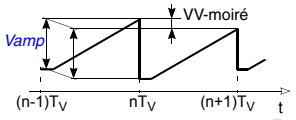
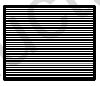
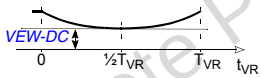
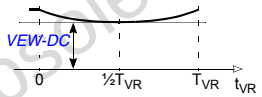
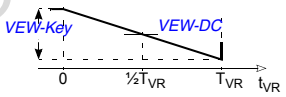
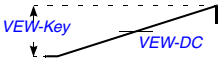
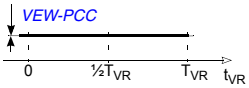
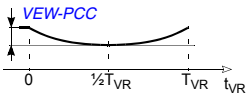
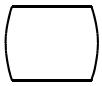
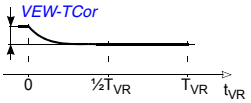
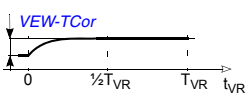
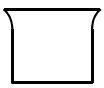
Function	Sad	Pin	Byte	Waveform	Effect on screen
C-correction		*VOut* ()	x0000000		
			x1000000 : Null		
			x1111111		
Vertical moiré amplitude		*VOut* ()	x0000000: Null		
			x1111111: Max.		
Horizontal size	h	*EWOut* ()	00000000		
			11111111		
Keystone correction		*EWOut* ()	x0000000		
			x1111111		
Pin cushion correction		*EWOut* ()	x0000000		
			x1111111		
Top corner correction		*EWOut* ()	x1111111		
			x0000000		

Table 14. Typical output waveforms(1) (continued)

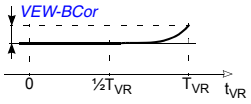
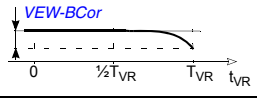
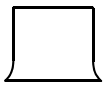
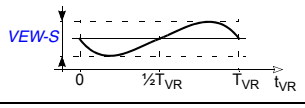
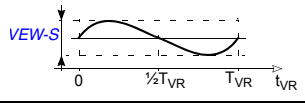
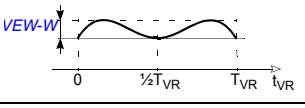
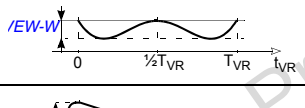
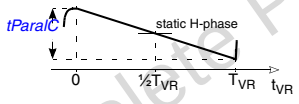
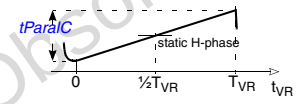
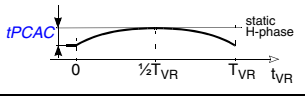
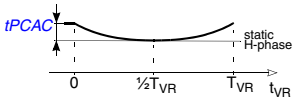
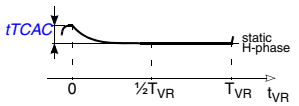
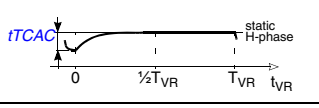
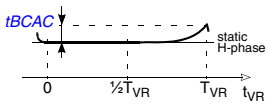
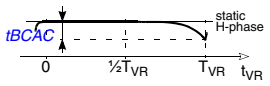
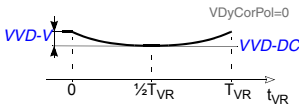
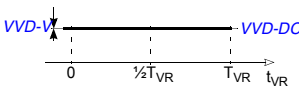
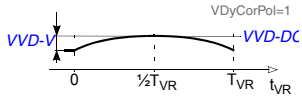
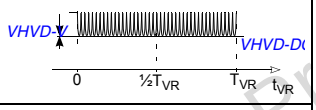
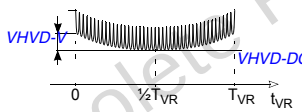
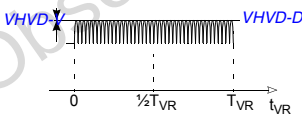
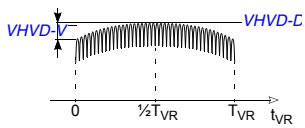
Function	Sad	Pin	Byte	Waveform	Effect on screen
Bottom corner correction		*EWOut* ()	x1111111		
			x0000000		
Pin Cushion S-correction		*EWOut* ()	x1111111		
			x0000000		
Pin Cushion W-correction		*EWOut* ()	x1111111		
			x0000000		
Parallelogram correction	h	Internal	x0000000		
			x1111111		
Pin cushion asymmetry correction	h	Internal	x0000000		
			x1111111		
Top corner asymmetry correction	h	Internal	x0000000		
			x1111111		

Table 14. Typical output waveforms(1) (continued)

Function	Sad	Pin	Byte	Waveform	Effect on screen
Bottom corner asymmetry correction	h	Internal	x0000000		
			x1111111		
Vertical dynamic correction amplitude	h	*VDyCor* ()	01111111		Application dependent
			x0000000		
			11111111		
HVDyCor vertical amplitude		*HVDyCor* () *HVDyCorPol*=0	x0000000		Application dependent
			x1111111		
HVDyCor vertical amplitude		*HVDyCor* () *HVDyCorPol*=1	x0000000		Application dependent
			x1111111		
HVDyCor horizontal adjustments	h	*HVDyCor* ()		See *Figure 18 on page 49*	Application dependent

1. For any H and V correction component of the waveforms on *EWOut* and *VOut* pins and internal waveform for corrections of H asymmetry, displayed in the table, the weight of the other relevant components is nullified (minimum for parabola, S-correction, medium for keystone, all corner corrections, C-correction, S- and W-pin cushion corrections, parallelogram, pin cushion asymmetry correction, written in corresponding registers).

6 I²C bus controlled register map

The device slave address is 8C in write mode and 8D in read mode. The control register map is given below.

Bold weight denotes default value at Power-On-Reset. I²C bus data in the adjustment register is buffered and internally applied with discharge of the vertical oscillator[a].
In order to ensure compatibility with future devices, all “Reserved” bits should be set to 0.

Table 15. I²C bus control registers

Sad	D7	D6	D5	D4	D3	D2	D1	D0
WRITE MODE (SLAVE ADDRESS = 8C)								
00	HDutySyncV	HDUTY			Horizontal duty cycle			
	1: Synchro. **0**: Asynchro.	0	0	0	0	0	0	0
01		HPOS			Horizontal position			
	1	0	0	0	0	0	0	0
02	HMoiréMode	HMOIRE			Horizontal moiré amplitude			
	1: Separated **0**: Combined	0	0	0	0	0	0	0
03	B+SyncV	BREF			B+reference			
	0: Asynchro.	1	0	0	0	0	0	0
04	HDyCorTr	HVDC-HAMP			HVDyCor horizontal amplitude			
	0: Not active	1	0	0	0	0	0	0
05	HDyCorPh	HVDC-HPH			HVDyCor horizontal phase			
	1: Middle **0**: Start	1	0	0	0	0	0	0
06	BOutPol	HVDC-VAMP			HVDyCor vertical amplitude			
	0: Type N	1	0	0	0	0	0	0
07	BOutPh	VSIZE			Vertical size			
	0: H-flyback 1: H-drive	1	0	0	0	0	0	0
08	EWTrHFr	VPOS			Vertical position			
	0: No tracking	1	0	0	0	0	0	0
09	Reserved	SCOR			S-correction			
		1	0	0	0	0	0	0
0A	Reserved	CCOR			C-correction			
		1	0	0	0	0	0	0
0B	Reserved	VMOIRE			Vertical moiré amplitude			
		0	0	0	0	0	0	0
0C	Reserved	PCC			Pin cushion correction			
		1	0	0	0	0	0	0
0D	Reserved	KEYST			Keystone correction			
		1	0	0	0	0	0	0

a. With exception of *Horizontal duty cycleHDUTY* and *BREF* adjustments data that can take effect instantaneously if switches *HDutySyncV* and *B+SyncV* are at 0, respectively.

Table 15. I²C bus control registers (continued)

Sad	D7	D6	D5	D4	D3	D2	D1	D0
0E	Reserved	TCC			Top corner correction			
		1	0	0	0	0	0	0
0F	Reserved	BCC			Bottom corner correction			
		1	0	0	0	0	0	0
10		HSIZE			Horizontal size			
	1	0	0	0	0	0	0	0
11	Reserved	PCAC			Pin cushion asymmetry correction			
		1	0	0	0	0	0	0
12	Reserved	PARAL			Parallelogram correction			
		1	0	0	0	0	0	0
13	Reserved	TCAC			Top corner asymmetry correction			
		1	0	0	0	0	0	0
14	Reserved	BCAC			Bottom corner asymmetry correction			
		1	0	0	0	0	0	0
15	VDyCorPol **0**: "∪"	VDC-AMP			Vertical dynamic correction			
		1	0	0	0	0	0	0
16	XRayReset **0**: No effect 1: Reset	VSyncAuto **1**: On	VSyncSel 0:Comp **1**:Sep	SDetReset **0**: No effect 1: Reset	PLL1Pump 1,1: Fastest **0,0**: Slowest		PLL1InhEn **1**: On	HLockEn **1**: On
17	TV **0**: Off(1)	TH **0**: Off	TVM **0**: Off	THM **0**: Off	BOHEdge **0**: Falling	HBOutEn **0**: Disable	VOutEn **0**: Disable	BlankMode **1**: Perm.
18	Reserved **0**:	HVDC-HSHAP			HVDyCor horizontal shape			
		0	0	0	0	0	0	0
19	Reserved **0**:	EWSC			East-West S-correction			
		1	0	0	0	0	0	0
1A	Reserved **0**:	EWWC			East-West W-correction			
		1	0	0	0	0	0	0
1B	Reserved **0**:	HEHTG			Horizontal EHT compensation gain			
		0	0	0	0	0	0	0
1C	Reserved **0**:	VEHTG			Vertical EHT compensation gain			
		0	0	0	0	0	0	0
1D	Reserved **0**:	VSAG			Vertical size after-gain			
		1	1	1	0	0	0	0
1E	Reserved **0**:	VPOF			Vertical position offset			
		1	0	0	0	0	0	0
1F	ThrBIsense **0:** High	BMute **0**: Off	BSafeEn **0**: Disable	EWTrHSize **0**: Tracking	Ident **0:** No effect	HLockSpeed **0:** Slow	HVDyCorPol **0**: "∪"	HDCFlatEn **0**: Disable
READ MODE (SLAVE ADDRESS = 8D)								
XX(2)	HLock 0: Locked **1**: Not locked	VLock 0: Locked **1**: Not lock.	XRayAlarm 1: On **0**: Off	Polarity detection		Sync detection		
				HVPol **1**: Negative	VPol **1**: Negative	VExtrDet **0**: Not det.	HVDet **0**: Not det.	VDet **0**: Not det.

1. The TV, TH, TVM and THM bits are for testing purposes and must be kept at 0 by application.
2. In Read Mode, the device always outputs data of the status register, regardless of sub address previously selected.

7 Description of I²C bus switches and flags

7.1 Write to bits

7.1.1 Sadh/D7 - *HDutySyncV*

Synchronization of internal application of **H**orizontal **Duty** cycle data, buffered in I²C bus latch, with internal discharge of **V**ertical oscillator.

0: Asynchronous mode, new data applied with ACK bit of I²C bus transfer on this sub address

1: Synchronous mode

7.1.2 Sadh/D7 - *HMoiréMode*

Horizontal **Moiré** characteristics.

0: Adapted to an architecture with EHT generated in deflection section

1: Adapted to an architecture with separated deflection and EHT sections

7.1.3 Sadh/D7 - *B+SyncV*

Same as *HDutySyncV*, applicable for **B+** reference data

7.1.4 Sadh/D7 - *HDyCorTr*

Tracking of **H**orizontal **Dy**namic **Cor**rection waveform amplitude with *HSIZE* adjustment.

0: Not active

1: Active

7.1.5 Sadh/D7 - *HDyCorPh*

Phase of start of **H**orizontal **Dy**namic **Cor**rection waveform in relation to horizontal flyback pulse.

0: Start of the flyback

1: Middle of the flyback

7.1.6 Sadh/D7 - *BOutPol*

Polarity of B+ drive signal on *BOut* pin.

0: adapted to N type of power MOS - high level to make it conductive

1: adapted to P type of power MOS - low level to make it conductive

7.1.7 Sadh/D7 - *BOutPh*

Phase of start of B+ drive signal on *BOut* pin

0: End of horizontal flyback or horizontal frequency divided by 2, see *BOHEdge* bit.

1: With one of edges of line drive signal on *HOut* pin, selected by *BOHEdge* bit

7.1.8 Sadh/D7 - *EWTrHFr*

Tracking of all corrections contained in waveform on pin *EWOut* with **H**orizontal **Fr**equency

0: Not active

1: Active

7.1.9 Sadh/D7 - *VDyCorPol*

Polarity of **V**ertical **Dy**namic **Cor**rection waveform (parabola)

0: Concave (minimum in the middle of the parabola)

1: Convex (maximum in the middle of the parabola)

7.1.10 Sadh/D0 - *HLockEn*

Enable of output of **H**orizontal PLL1 **Lock**/unlock status signal on pin *HLckVBk*

0: Disabled, vertical blanking only on the pin *HLckVBk*

1: Enabled

7.1.11 Sadh/D1 - *PLL1InhEn*

Enable of **Inh**ibition of horizontal **PLL1** during extracted vertical synchronization pulse

0: Disabled, PLL1 is never inhibited

1: Enabled

7.1.12 Sadh/D2 and D3- *PLL1Pump*

Horizontal **PLL1** charge **Pump** current

Table 16. Time constant

D3	D2	Time constant
0	0	Slowest PLL1, lowest current
1	0	Moderate Slow PLL1, low current
0	1	Moderate Fast PLL1, high current
1	1	Fastest PLL1, highest current

7.1.13 Sadh/D4 - *SDetReset*

Reset to 0 of **S**ynchronization **Det**ection flags *VDet*, *HVDet* and *VExtrDet* of status register effected with ACK bit of I²C bus data transfer into register containing the *SDetReset* bit. Also see description of the flags.

0: No effect

1: Reset with automatic return of the bit to 0

7.1.14 Sadh/D5 - *VSyncSel*

Vertical **Sync**hronization input **Sel**ection between the one extracted from composite HV signal on pin *H/HVSyn* and the one on pin *VSyn*. No effect if *VSyncAuto* bit is at 1.

0: V. sync extracted from composite signal on *H/HVSyn* pin selected

1: V. sync applied on *VSyn* pin selected

7.1.15 Sadh/D6 - *VSyncAuto*

Vertical **Sync**hronization input selection **Auto**matic mode. If enabled, the device automatically selects between the vertical sync extracted from composite HV signal on pin *H/HVSyn* and the one on pin *VSyn*, based on detection mechanism. If both are present, the one coming first is kept.

0: Disabled, selection done according to bit *VSyncSel*

1: Enabled, the bit *VSyncSel* has no effect

7.1.16 Sadh/D7 - *XRayReset*

Reset to 0 of **XRay** flag of status register effected with ACK bit of I²C bus data transfer into register containing the *XRayReset* bit. Also see description of the flag.

0: No effect

1: Reset with automatic return of the bit to 0

7.1.17 Sadh/D0 - *BlankMode*

Blanking operation **Mode**

0: Blanking pulse starting with detection of vertical synchronization pulse and ending with end of vertical oscillator discharge (start of vertical sawtooth ramp on the *VOut* pin)

1: Permanent blanking - high blanking level in composite signal on pin *HLckVBk* is permanent

7.1.18 Sadh/D1 - *VOutEn*

Vertical **Out**put **En**able

0: Disabled, *VoffVOut* on *VOut* pin (see *Section 4.5*)

1: Enabled, vertical ramp with vertical position offset on *VOut* pin

7.1.19 Sadh/D2 - *HBOutEn*

Horizontal and **B**+ **Out**put **En**able

0: Disabled, levels corresponding to “power transistor off” on *HOut* and *BOut* pins (high for *HOut*, high or low for *BOut*, depending on *BOutPol* bit).

1: Enabled, horizontal deflection drive signal on *HOut* pin providing that it is not inhibited by another internal event (activated XRay protection). B+ drive signal on *BOut* pin if not inhibited by another internal event.

Programming the bit to 1 after prior value of 0, will initiate soft start mechanism of horizontal drive and, if this is not inhibited by another internal event, also the soft start of B+ DC/DC convertor controller. See also bits *BMute* and *BSafeEn*.

7.1.20 Sadh/D3 - *BOHEdge*

If the bit *BOutPh* is at 1, selection of **Edge** of **H**orizontal drive signal to phase **B**+ drive **O**utput signal on *BOut* pin.

1: Rising edge

0: Falling edge

If the bit *BOutPh* is at 0, selection of signal to phase **B**+ drive output on *BOut* pin:

1: Horizontal frequency divided by 2 signal, top of horizontal VCO

0: End of horizontal flyback

7.1.21 Sadh/D4,D5,D6,D7 - *THM*, *TVM*, *TH*, *TV*

Test bits. They must be kept at 0 level by application S/W.

7.1.22 Sadh/D0 - *HDCFlatEn*

Enlargement of the **Flat** part on **H**orizontal **D**ynamic **C**orrection waveform (starting at the beginning of horizontal flyback).

0: Disable

1: Enable

7.1.23 Sadh/D1 - *HVDyCorPol*

Polarity of **HV Dy**namic **Cor**rection waveform.

0: Concave (minimum in the middle of the parabola)

1: Convex (maximum in the middle of the parabola)

7.1.24 Sadh/D2 - *HLockSpeed*

Response **Speed** of lock-to-unlock transition of H-lock component on **HLock** output and *HLock* I²C bus flag at signal change.

0: Low

1: High

7.1.25 Sadh/D3 - *Ident*

Device **Ident**ification bit.

If *HBOutEn* is at 1, the bit has no effect.

If *HBOutEn* is at 0, then

0: The value of Hlock status bit is 1

1: The value of Hlock status bit is 0

7.1.26 Sadh/D4 - *EWTrHSize*

Tracking of all corrections contained in waveform on pin **EW**Out with **H**orizontal **Size** I²C bus register *HSIZE*.

0: Active

1: Not active

7.1.27 Sadh/D5 - *BSafeEn*

B+ Output **Safe**ty **En**able

0: Disabled

1: Enabled, *BOut* goes off as soon as HLock status of Horizontal PLL1 indicates “unlock” state. Retrieval of “lock” state will initiate soft start mechanism of DC/DC controller on *BOut* output.

7.1.28 Sadh/D6 - *BMute*

B+ Output **Mute**

0: Disabled

1: Enabled, *BOut* goes unconditionally off. Programming this bit back to 0 will initiate soft start mechanism of DC/DC controller on *BOut* output.

7.1.29 Sadh/D7 - *ThrBIsense*

Threshold on *BISense* input corresponding to current limitation.

0: High

1: Low

7.2 Read-out flags

7.2.1 SadXX/D0 - *VDet*[b]

Flag indicating **Det**ection of **V** synchronization pulses on *VSyn* pin.

0: Not detected

1: Detected

7.2.2 SadXX/D1 - *HVDet*

Flag indicating **Det**ection of **H** or H**V** synchronization pulses applied on *H/HVSyn* pin. Once the sync pulses are detected, the flag is set and latched. Disappearance of the sync signal will not lead to reset of the flag.

b. This flag, by its value of 1, indicates an event of detection of at least one synchronization pulse since its last reset (by means of the *SDetReset* I²C bus bit). This is to be taken into account by application S/W in a way that enough time (at least the period between 2 synchronization pulses of analyzed signal) must be provided between reset of the flag through *SDetReset* bit and validation of information provided in the flag after read-out of status register.

0: Not detected

1: Detected.

7.2.3 SadXX/D2 - *VExtrDet*

Flag indicating **Det**ection of **Extr**acted **V**ertical synchronization signal from composite H+V signal applied on *H/HVSyn* pin.

0: Not detected

1: Detected

7.2.4 SadXX/D3 - *VPol*

Flag indicating **Pol**arity of **V** synchronization pulses applied on *VSyn* pin with respect to mean level of the sync signal.

0: Positive

1: Negative

7.2.5 SadXX/D4 - *HVPol*

Flag indicating **Pol**arity of **H** or H**V** synchronization pulses applied on *H/HVSyn* pin with respect to mean level of the sync signal.

0: Positive

1: Negative

7.2.6 SadXX/D5 - *XRayAlarm*

Alarm indicating that an event of excessive voltage has passed on *XRay* pin. Can only be reset to 0 through I²C bus bit *XRayReset* or by power-on reset.

0: No excess since last reset of the bit

1: At least one event of excess appeared since the last reset of the bit, *HOut* inhibited

7.2.7 SadXX/D6 - *VLock*

Status of "**Lock**ing" or stabilizing of **V**ertical oscillator amplitude to an internal reference by AGC regulation loop.

0: Locked (amplitude stabilized)

1: Not locked (amplitude non-stabilized)

7.2.8 SadXX/D7 - *HLock*

Lock status of **H**orizontal PLL1.

0: Locked

1: Not locked

See also bit *Ident* **(**Sadh/D3)

8 Operating description

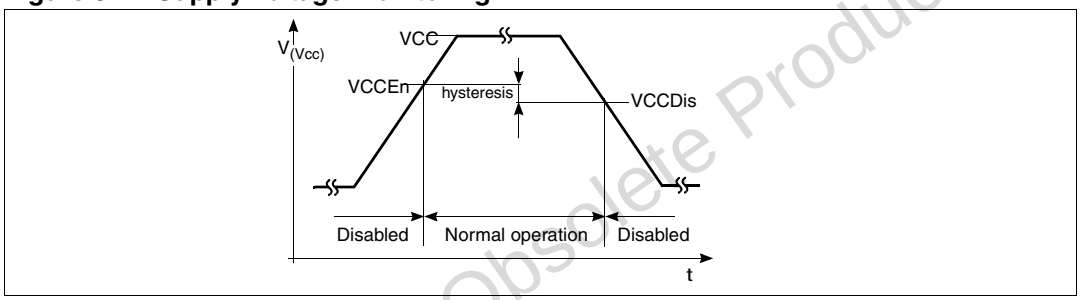
8.1 Supply and control

8.1.1 Power supply and voltage references

The device is designed for a typical value of power supply voltage of 12 V.

In order to avoid erratic operation of the circuit at power supply ramp-up or ramp-down, the value of *VCC* is monitored. See *Figure 3* and electrical specifications. At switch-on, the device enters a “normal operation” as the supply voltage exceeds *VCCEn* and stays there until it decreases bellow *VCCDis*. The two thresholds provide, by their difference, a hysteresis to bridge potential noise. Outside the “normal operation”, the signals on *HOut*, *BOut* and *VOut* outputs are inhibited and the I²C bus interface is inactive (high impedance on *SDA*, *SCL* pins, no ACK), all I²C bus control registers being reset to their default values. The stop of *HOut* and *BOut* drive signals when the *VCC* falls from normal operation below *VCCDis* is not instantaneous. It is only a trigger point of Soft Stop mechanism (see *Section 8.3.6*).

Figure 3. Supply voltage monitoring



Internal thresholds in all parts of the circuit are derived from a common internal reference supply *VRefO* that is lead out to *RefOut* pin for external filtering against ground as well as for external use with load currents limited to *IRefO*. The filtering is necessary to minimize interference in output signals, causing adverse effects like e.g. jitter.

8.1.2 I²C bus control

The I²C bus is a 2 line bidirectional serial communication bus introduced by Philips. For its general description, refer to corresponding Philips I²C bus specification.

This device is an I²C bus slave, compatible with fast (400 kHz) I²C bus protocol, with write mode slave address of 8Ch (read mode slave address 8Dh). Integrators are employed at the *SCL* (Serial Clock) input and at the input buffer of the *SDA* (Serial Data) input/output to filter off the spikes up to 50ns.

The device supports multiple data byte messages (with automatic incrementing of the I²C bus subaddress) as well as repeated Start Condition for I²C bus subaddress change inside the I²C bus messages. All I²C bus registers with specified I²C bus subaddress are of WRITE ONLY type, whereas the status register providing a feedback information to the master I²C bus device has no attributed I²C bus subaddress and is of READ ONLY type. The master I²C bus device reads this register sending directly, after the Start Condition, the READ device I²C bus slave address (8Dh) followed by the register read-out, NAK (No Acknowledge) signal and the Stop Condition. For the I²C bus control register map, refer to *Section 6*.

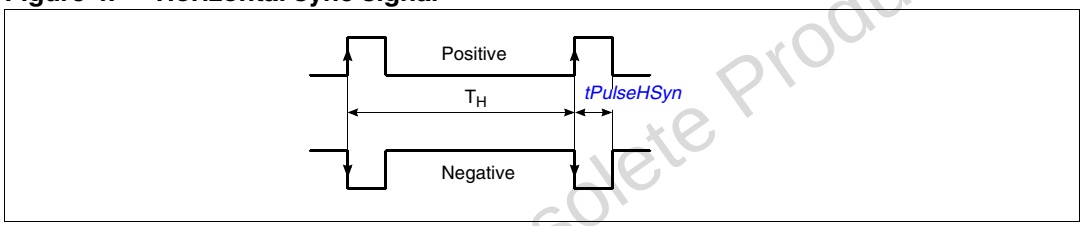
8.2 Synchronization processor

8.2.1 Synchronization signals

The device has two inputs for TTL-level synchronization signals, both with hysteresis to avoid erratic detection and with a pull-down resistor. On *H/HVSyn* input, pure horizontal or composite horizontal/vertical signal is accepted. On *VSyn* input, only pure vertical sync signal is accepted. Both positive and negative polarities may be applied on either input, see *Figure 4*. Polarity detector and programmable inverter are provided on each of the two inputs. The signal applied on *H/HVSyn* pin, after polarity treatment, is directly lead to horizontal part and to an extractor of vertical sync pulses, working on principle of integration, see *Figure 3*. The vertical sync. signal applied to the vertical deflection processor is selected between the signal extracted from the composite signal on *H/HVSyn* input and the one applied on *VSyn* input. The selector is controlled by *VSyncSel* I²C bus bit.

Besides polarity detection, the device is capable of detecting presence of sync. signals on each of the inputs and at the output of vertical sync extractor. The information from all detectors is provided in the I²C bus status register (5 flags: *VDet*, *HVDet*, *VExtrDet*, *VPol*, *HVPol*). The device is equipped with an automatic mode (switched on or off by *VSyncAuto* I²C bus bit) that also uses the detection information.

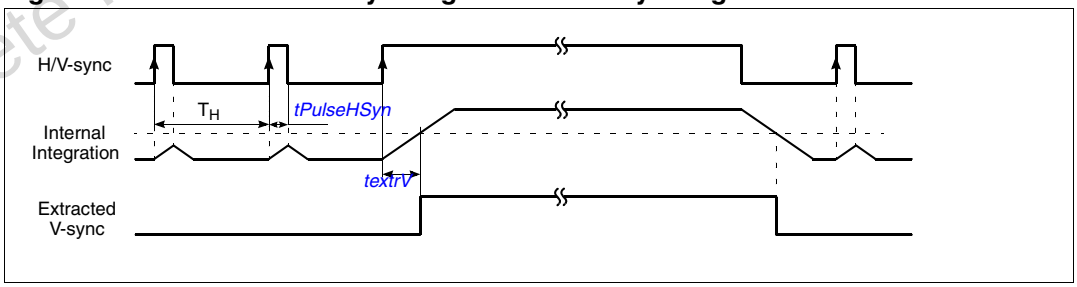
Figure 4. Horizontal sync signal



8.2.2 Sync presence detection flags

The sync signal presence detection flags in the status register (*VDet*, *HVDet*, *VExtrDet*) do not show in real time the presence or absence of corresponding sync signal. They are latched to 1 as soon as a single sync pulse is detected. In order to reset them to 0 (all at once), a 1 must be written into *SDetReset* I²C bus bit, the reset action taking effect with ACK bit of the I²C bus transfer to the register containing *SDetReset* bit. The detection circuits are ready to capture another event (pulse).

Figure 5. Extraction of V-sync signal from H/V-sync signal



8.2.3 MCU controlled sync selection mode

I²C bus bit *VSyncAuto* is set to 0. The MCU reads the polarity and signal presence detection flags, after setting the *SDetReset* bit to 1 and an appropriate delay, to obtain a true information of the signals applied, reads and evaluates this information and controls the vertical signal selector accordingly. The MCU has no access to polarity inverters, they are controlled automatically.

8.2.4 Automatic sync selection mode

I²C bus bit *VSyncAuto* is set to 1. In this mode, the device itself controls the I²C bus bits switching the polarity inverters (*HVPol*, *VPol*) and the vertical sync. signal selector (*VSyncSel*), using the information provided by the detection circuitry. If both extracted and pure vertical sync. signals are present, the one already selected is maintained. No intervention of the MCU is necessary.

8.3 Horizontal section

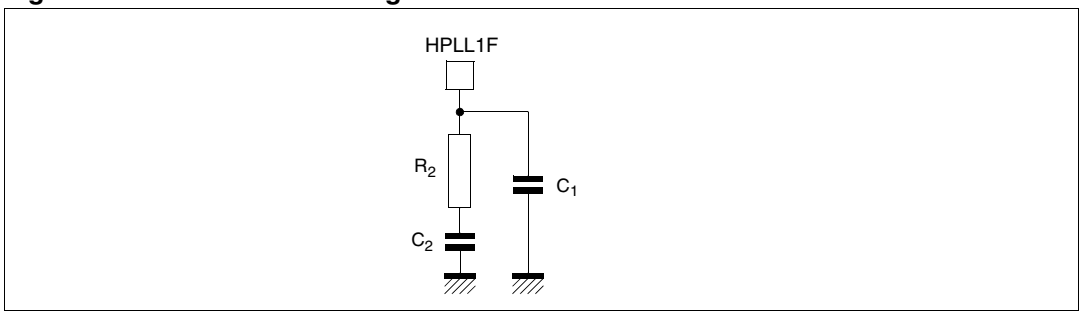
The horizontal section consists of two PLLs with various adjustments and corrections, working on horizontal deflection frequency, then phase shifting and output driving circuitry providing H-drive signal on *HOut* pin. Input signal to the horizontal section is output of the polarity inverter on *H/HVSyn* input. The device ensures automatically that this polarity be always positive.

8.3.1 PLL1

The PLL1 block diagram is in *Figure 5*. It consists of a voltage-controlled oscillator (VCO), a shaper with adjustable threshold, a charge pump with inhibition circuit, a frequency and phase comparator and timing circuitry. The goal of the PLL1 is to make the VCO ramp signal match in frequency the sync. signal and to lock this ramp in phase to the sync. signal. On the screen, this offset results in the change of horizontal position of the picture. The loop, by tuning the VCO accordingly, gets and maintains in coincidence the rising edge of input sync signal with signal REF1, deriving from the VCO ramp by a comparator with threshold adjustable through *HPOS* I²C bus control. The coincidence is identified and flagged by lock detection circuit on pin *HLckVBk* as well as by *HLock* I²C bus flag.

The charge pump provides positive and negative currents charging the external loop filter on *HPLL1F* pin. The loop is independent of the trailing edge of sync signal and only locks to its leading edge. By design, the PLL1 does not suffer from any dead band even while locked. The speed of the PLL1 depends on current value provided by the charge pump. While not locked, the current is very low, to slow down the changes of VCO frequency and thus protect the external power components at sync signal change. In locked state, the currents are much higher, four different values being selectable via *PLL1Pump* I²C bus bits to provide a means to control the PLL1 speed by S/W. Lower value make the PLL1 slower, but more stable. Higher values make it faster and less stable. In general, the PLL1 speed should be higher for high deflection frequencies. The response speed and stability (jitter level) depend on the choice of external components making up the loop filter. A “CRC” filter is generally used (see *Figure 4*).

Figure 6. H-PLL1 filter configuration



The PLL1 is internally inhibited during extracted vertical sync pulse (if any) to avoid taking into account missing or wrong pulses on the phase comparator. Inhibition is obtained by forcing the charge pump output to high impedance state. The inhibition mechanism can be disabled through *PLL1InhEn* I²C bus bit.

The *Figure 7*, in its upper part, shows the position of the VCO ramp signal in relation to input sync pulse for three different positions of adjustment of horizontal position control *HPOS*.

Figure 7. Horizontal PLL1 block diagram

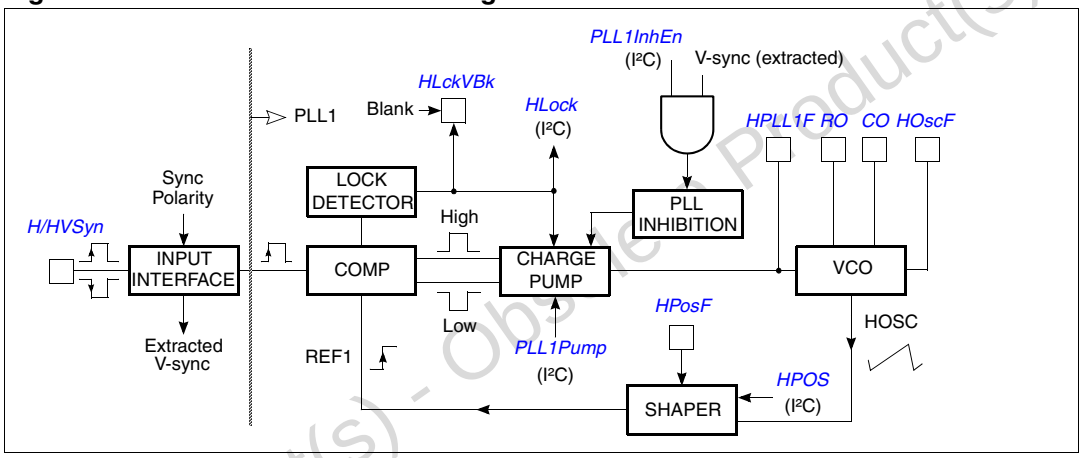
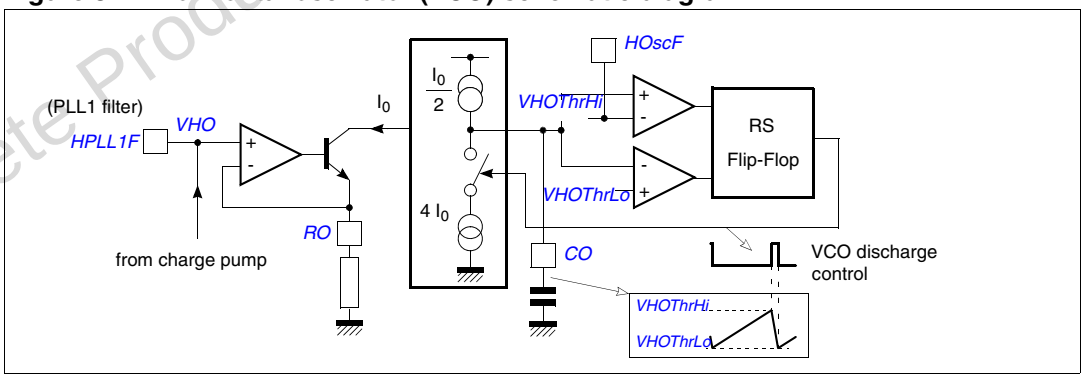


Figure 8. Horizontal oscillator (VCO) schematic diagram



8.3.2 Voltage controlled oscillator

The VCO makes part of both PLL1 and PLL2 loops, being an “output” to PLL1 and “input” to PLL2. It delivers a linear sawtooth. *Figure 8* explains its principle of operation. The linears are obtained by charging and discharging an external capacitor on pin *CO*, with currents proportional to the current forced through an external resistor on pin *RO*, which itself depends on the input tuning voltage *VHO* (filtered charge pump output). The rising and falling linears are limited by *VHOThrLo* and *VHOThrHi* thresholds filtered through *HOscF* pin.

At no signal condition, the *VHO* tuning voltage is clamped to its minimum (see *Section 4.4*), which corresponds to the free-running VCO frequency *fHO(0)*. Refer to *Section 8.4.1* for formula to calculate this frequency using external components values. The ratio between the frequency corresponding to maximum *VHO* and the one corresponding to minimum *VHO* (free-running frequency) is about 4.5. This range can easily be increased in the application. The PLL1 can only lock to input frequencies falling inside these two limits.

8.3.3 PLL2

The goal of the PLL2 is, by means of phasing the signal driving the power deflection transistor, to lock the middle of the horizontal flyback to a certain threshold of the VCO sawtooth. This internal threshold is affected by geometry phase corrections, like e.g., parallelogram. The PLL2 is fast enough to be able to follow the dynamism of phase modulation, this speed is strongly related to the value of the capacitor on *HPLL2C*. The PLL2 control current (see *Figure 9*) is significantly increased during discharge of vertical oscillator (during vertical retrace period) to be able to make up for the difference of dynamic phase at the bottom and at the top of the picture. The PLL2 control current is integrated on the external filter on pin *HPLL2C* to obtain smoothed voltage, used, in comparison with VCO ramp, as a threshold for H-drive rising edge generation.

As both leading and trailing edges of the H-drive signal in the *Figure 9* must fall inside the rising part of the VCO ramp, an optimum middle position of the threshold has been found to provide enough margin for horizontal output transistor storage time as well as for the trailing edge of H-drive signal with maximum duty cycle. Yet, the constraints thereof must be taken into account while considering the application frequency range and H-flyback duration. The *Figure 9* also shows regions for rising and falling edges of the H-drive signal on *HOut* pin. As it is forced high during the H-flyback pulse and low during the VCO discharge period, no edge during these two events takes effect.

The flyback input configuration is in *Figure 10*.

8.3.4 Dynamic PLL2 phase control

The dynamic phase control of PLL2 is used to compensate for picture asymmetry versus vertical axis across the middle of the picture. It is done by modulating the phase of the horizontal deflection with respect to the incoming video (synchronization). Inside the device, the threshold *VS(0)* is compared with the VCO ramp, the PLL2 locking the middle of H-flyback to the moment of their match. The dynamic phase is obtained by modulation of the threshold by correction waveforms. Refer to *Figure 16* and *Section 7*. The correction waveforms have no effect in vertical middle of the screen (for middle vertical position). As they are summed, their effect on the phase tends to reach maximum span at top and bottom of the picture. As all the components of the resulting correction waveform (linear for parallelogram correction, parabola of 2nd order for Pin cushion asymmetry correction and half-parabolas of 4th order for corner corrections independently at the top and at the bottom)

are generated from the output vertical deflection drive waveform, they all track with real vertical amplitude and position, thus being fixed on the screen. Refer to *Section 8* for details on I²C bus controls.

Figure 9. Horizontal timing diagram

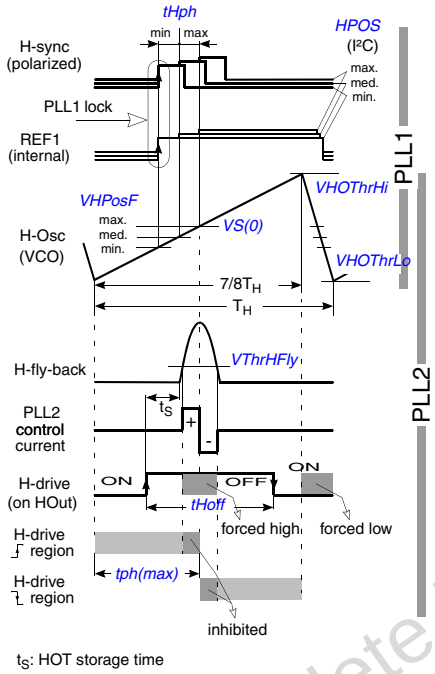
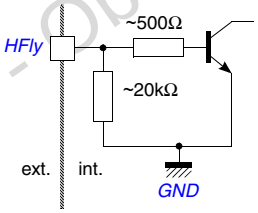


Figure 10. HFly input configuration



8.3.5 Output section

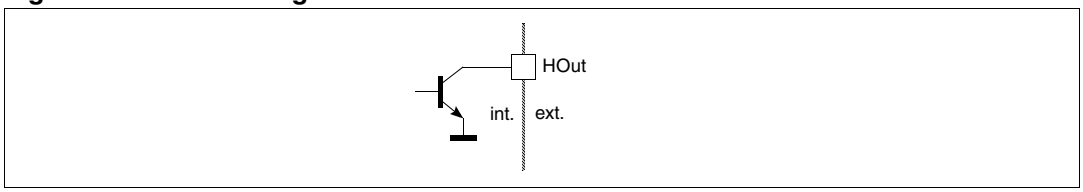
The H-drive signal is inhibited (high level) during flyback pulse, and also when *VCC* is too low, when X-ray protection is activated (*XRayAlarm* I²C bus flag set to 1) and when I²C bus bit *HBOutEn* is set to 0 (default position).

The duty cycle of the H-drive signal is controlled via I²C bus register *HDUTY*. This is overruled during soft-start and soft-stop procedures (see *Section 8.3.6* and *Figure 12*).

The PLL2 is followed by a rapid phase shifting which accepts the signal from H-moiré canceller (see *Section 8.3.7*)

The output stage consists of a NPN bipolar transistor, the collector of which is routed to *HOut* pin (see *Figure 11*).

Figure 11. *HOut* configuration



8.3.6 Soft-start and soft-stop on H-drive

The soft-start and soft-stop procedure is carried out at each switch-on or switch-off of the H-drive signal, either via *HBOutEn* I²C bus bit or after reset of *XRayAlarm* I²C bus flag, to protect external power components. By its second function, the external capacitor on pin *HPosF* is used to time out this procedure, during which the duty cycle of H-drive signal starts at its maximum (*tHoff* for soft start/stop in electrical specifications) and slowly decreases to the value determined by the control I²C bus register *HDUTY* (vice versa at soft-stop). This is controlled by voltage on pin *HPosF*. In case of supply voltage switch off, the transients on *HOut* and *BOut* have different characteristics. See *Figure 12*, *Figure 13* and *Section 8.8.1*.

8.3.7 Horizontal moiré cancellation

The horizontal moiré canceller is intended to blur a potential beat between the horizontal video pixel period and the CRT pixel width, which causes visible moiré patterns in the picture.

It introduces a microscopic indent on horizontal scan lines by injecting little controlled phase shifts to output circuitry of the horizontal section. Their amplitude is adjustable through *HMOIRE* I²C bus control.

The behaviour of horizontal moiré is to be optimized for different deflection design configurations using *HMoiréMode* I²C bus bit. This bit is to be kept at 0 for common architecture (B+ and EHT common regulation) and at 1 for separated architecture (B+ and EHT each regulated separately). The maximum amplitude adjustable though *HMOIRE* I²C bus control is optimized according to selection by *HMoiréMode* I²C bus bit: larger when B+ and EHT are each regulated separately, smaller when B+ and EHT are common regulation.

Figure 12. Control of *HOut* and *BOut* at start/stop at nominal *VCC*

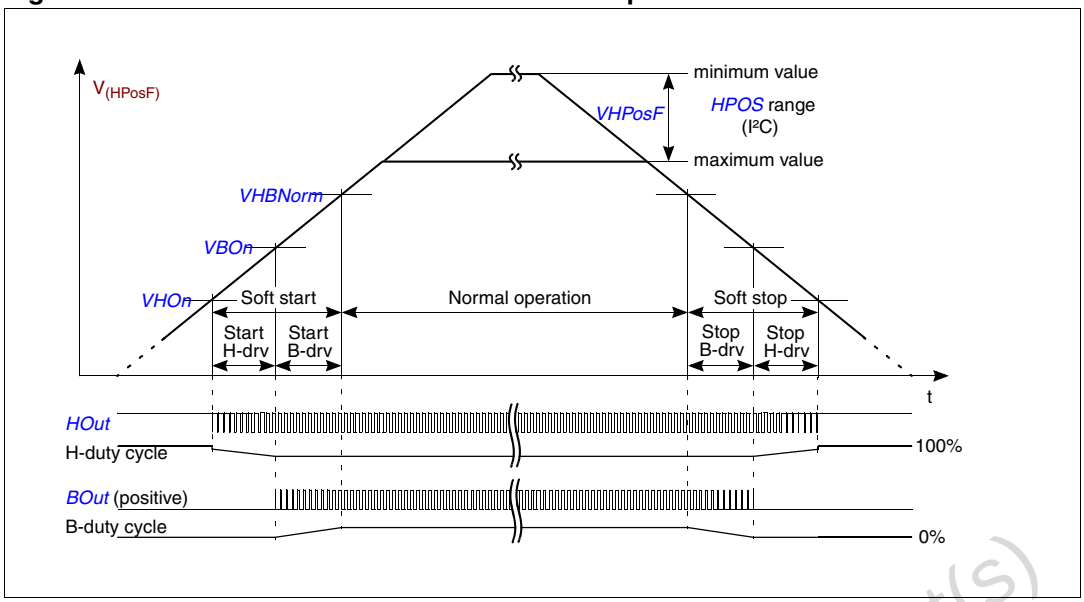
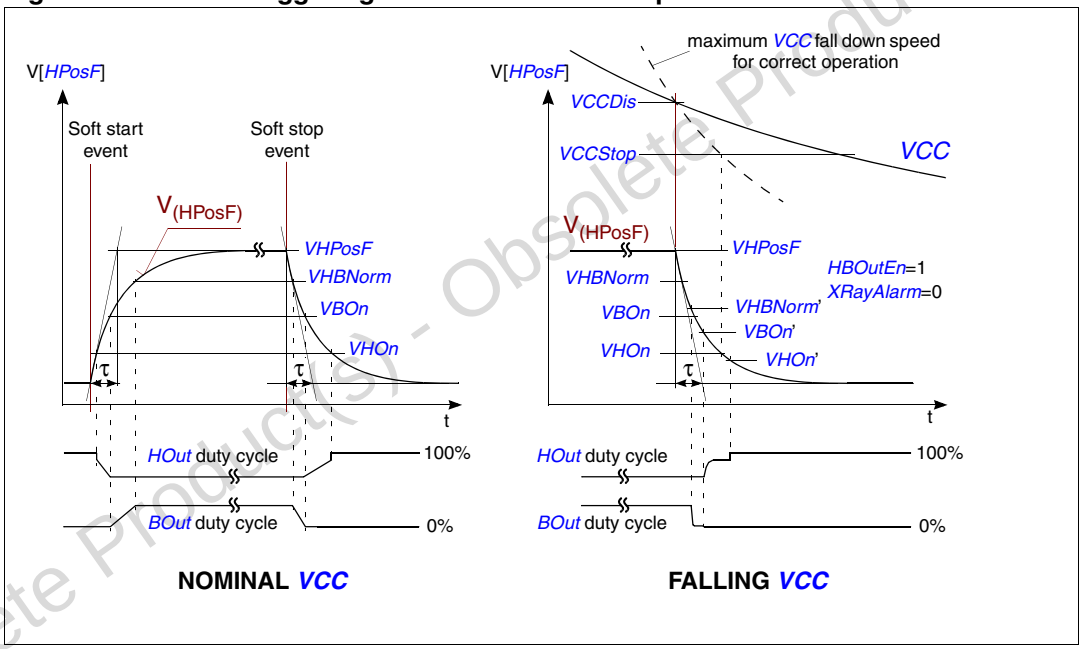


Figure 13. Events triggering soft start and soft stop



8.4 Vertical section

The goal of the vertical section is to drive vertical deflection output stage. It delivers a sawtooth waveform with an amplitude independent of deflection frequency, on which vertical linearity corrections of C- and S-type are superimposed (see *Section 8*).

Block diagram is in *Figure 14*. The sawtooth is obtained by charging an external capacitor on pin *VCap* with controlled current and by discharging it via transistor Q1. This is controlled by the CONTROLLER. The charging starts when the voltage across the capacitor drops

below *VVOB* threshold. The discharging starts either when it exceeds *VVOT* threshold (free run mode) or a short time after arrival of synchronization pulse. This time is necessary for the AGC loop to sample the voltage at the top of the sawtooth. The *VVOB* reference is routed out onto *VOscF* pin in order to allow for further filtration.

The charging current influences amplitude of the sawtooth. Just before the discharge, the voltage across the capacitor on pin *VCap* is sampled and compared to *VVOTref*. The comparison error voltage is stored on a storage capacitor connected on pin *VAGCCap*. This voltage tunes gain of the transconductance amplifier providing the charging current in the next vertical period. Speed of this AGC loop depends on the storage capacitance on pin *VAGCCap*. The *VLock* I²C bus flag is set to 1 when the loop is stabilized, i.e. when the tops of saw tooth on pin *VCap* match *VVOT* value. On the screen, this corresponds to stabilized vertical size of picture. After a change of frequency on the sync. input, the stabilization time depends on the frequency difference and on the capacitor value. The lower its value, the shorter the stabilization time, but on the other hand, the lower the loop stability. A practical compromise is a capacitance of 470 nF. The leakage current of this capacitor results in difference in amplitude between low and high frequencies. The higher its parallel resistance *RL(VAGCCap)*, the lower this difference.

When the synchronization pulse is not present, the charging current is fixed. As a consequence, the free-running frequency fVO(0) only depends on the value of the capacitor on pin *VCap*. It can be roughly calculated using the following formula

$$fVO(0) = \frac{150nF}{C_{(VCap)}} \cdot 100Hz$$

The frequency range in which the AGC loop can regulate the amplitude also depends on this capacitor.

The vertical sawtooth with regulated amplitude is lead to amplitude control stage. The discharge exponential is replaced by *VVOB* level, which, under control of the CONTROLLER, creates a rapid falling edge and a flat part before beginning of new ramp.

The AGC output signal passes through gain and position adjustment stages controlled through *VSIZE* and *VPOS* I²C bus registers. The resulting signal serves as input to all geometry correction circuitry including EW-drive signal, horizontal phase modulation and dynamic correction outputs.

8.4.1 S and C corrections

For the sake of vertical picture linearity, the S- and C-corrections are now superimposed on the linear ramp signal. They both track with *VSIZE* and *VPOS* adjustments to ensure unchanged linearity on the screen at changes of vertical size or vertical position. As these corrections are not included in the AGC loop, their adjustment via *CCOR* and *SCOR* I²C bus registers, controlling shape of vertical output sawtooth affects by principle its peak-to-peak amplitude. However, this stage is conceived in a way that the amplitude be independent of these adjustments if *VSIZE* and *VPOS* registers are set to their medium values.

8.4.2 Vertical breathing compensation

The signal provided with the linearity corrections is amplitude affected in a gain control stage, ruled by the voltage on *VEHTIn* input and its I²C bus control *VEHTG*.

8.4.3 Vertical after-gain and offset control

Another gain control is applied via *VSAG* I²C bus register. Then an offset is added, its amount corresponding to *VPOF* I²C bus register value. These two controls result in size and position changes with no effect on shape of output vertical sawtooth or any geometry correction signal.

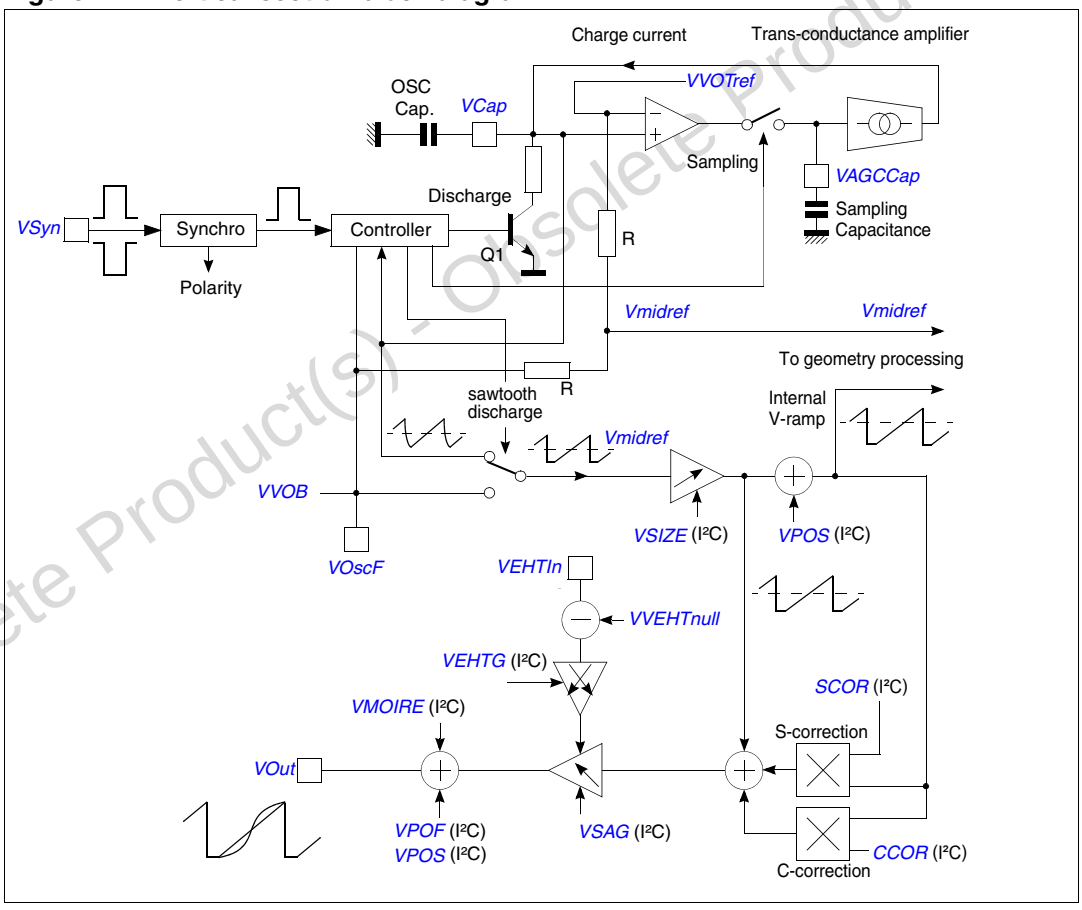
8.4.4 Vertical moiré

To blur potential moiré patterns due to interaction of deflection lines with CRT mask grid, the picture position is to be slightly alternated at frame frequency. For this purpose, a square waveform at half-frame frequency is superimposed on the output waveform. Its amplitude is adjustable through *VMOIRE* I²C bus control.

8.4.5 Biasing of vertical booster

The biasing voltage for external DC-coupled vertical power amplifier is to be derived from *VRefO* voltage provided on pin *RefOut*, using a resistor divider, this to ensure the same temperature drift of mean (DC) levels on both differential inputs and to compensate for spread of *VRefO* value (and so mean output value) between particular devices.

Figure 14. Vertical section block diagram



8.5 EW drive section

The goal of the EW drive section is to provide, on pin *EWOut*, a waveform which, used by an external DC-coupled power stage, serves to compensate for those geometry errors of the picture that are symmetric versus vertical axis across the middle of the screen.

The waveform consists of an adjustable DC value, corresponding to horizontal size, a parabola of 2nd order for “pin cushion” correction, a linear for “keystone” correction, independent half-parabolas of 4th order for top and bottom corner corrections, S- shape for “S” correction and W shape for “W” correction. All of them are adjustable via I²C bus, see *Section 7*.

Refer to *Figure 16*, *Figure 17* and chapter *Section 7*. The adjustments of these correction waveforms have no effect in the middle of the vertical scan period (if the *VPOS* control is adjusted to its medium value). As they are summed, the resulting waveform tends to reach its maximum span at top and bottom of the picture. The voltage at the *EWOut* is top and bottom limited (see parameter VEW). According to *Figure 17*, especially the bottom limitation seems to be critical for maximum horizontal size (minimum DC). Actually it is not critical since the parabola component must always be applied to obtain a picture without pin cushion distortion. As all the components of the resulting correction waveform are generated from an internal linear vertical sawtooth waveform bearing *VSIZE* and *VPOS* adjustments, they all track with vertical amplitude and position, thus being fixed vertically on the screen. They are not affected by C- and S-corrections, by prescale adjustments (*VSAG* and *VPOF*), by vertical breathing compensation and by vertical moire cancellation. The sum of components other than DC is conditionally affected by value in *HSIZE* I²C bus control in reversed sense. Refer to electrical specifications for value. This tracking with *HSIZE* can be switched off by *EWTrHSize* I²C bus bit. The DC value, adjusted via *HSIZE* control, is also affected by voltage on *HEHTIn* input, thus providing a horizontal breathing compensation. The effect of this compensation is controlled by *HEHTG*. The resulting waveform is conditionally multiplied with voltage on *HPLL1F*, which depends on frequency. Refer to electrical specifications for values. This tracking with frequency provides a rough compensation of variation of picture geometry with frequency and allows to fix the adjustment ranges of I²C bus controls throughout the operating range of horizontal frequencies. It can be switched off by *EWTrHFr* I²C bus bit (off by default). The functionality is explained in *Figure 15*. The upper part gives the influence on DC component, the lower part on AC component, showing also the tracking with *HSIZE*. Grey zones give the total span of breathing correction using the whole range of input operating voltage on *HEHTIn* input and whole range of adjustment of *HEHTG* register.

The EW waveform signal is buffered by an NPN emitter follower, the emitter of which is directly routed to *EWOut* output. It is internally biased (see electrical specifications for current value).

Figure 15. Tracking of *EWOut* signal with frequency

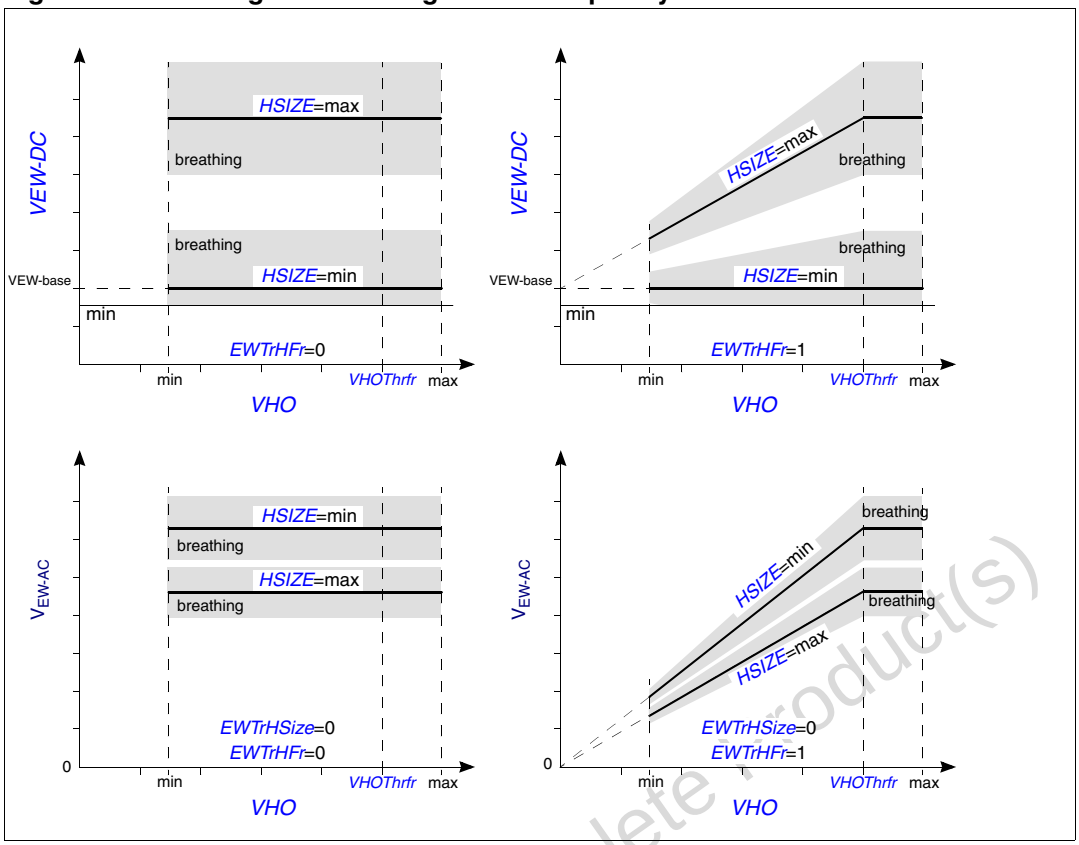


Figure 16. Geometric corrections' schematic diagram

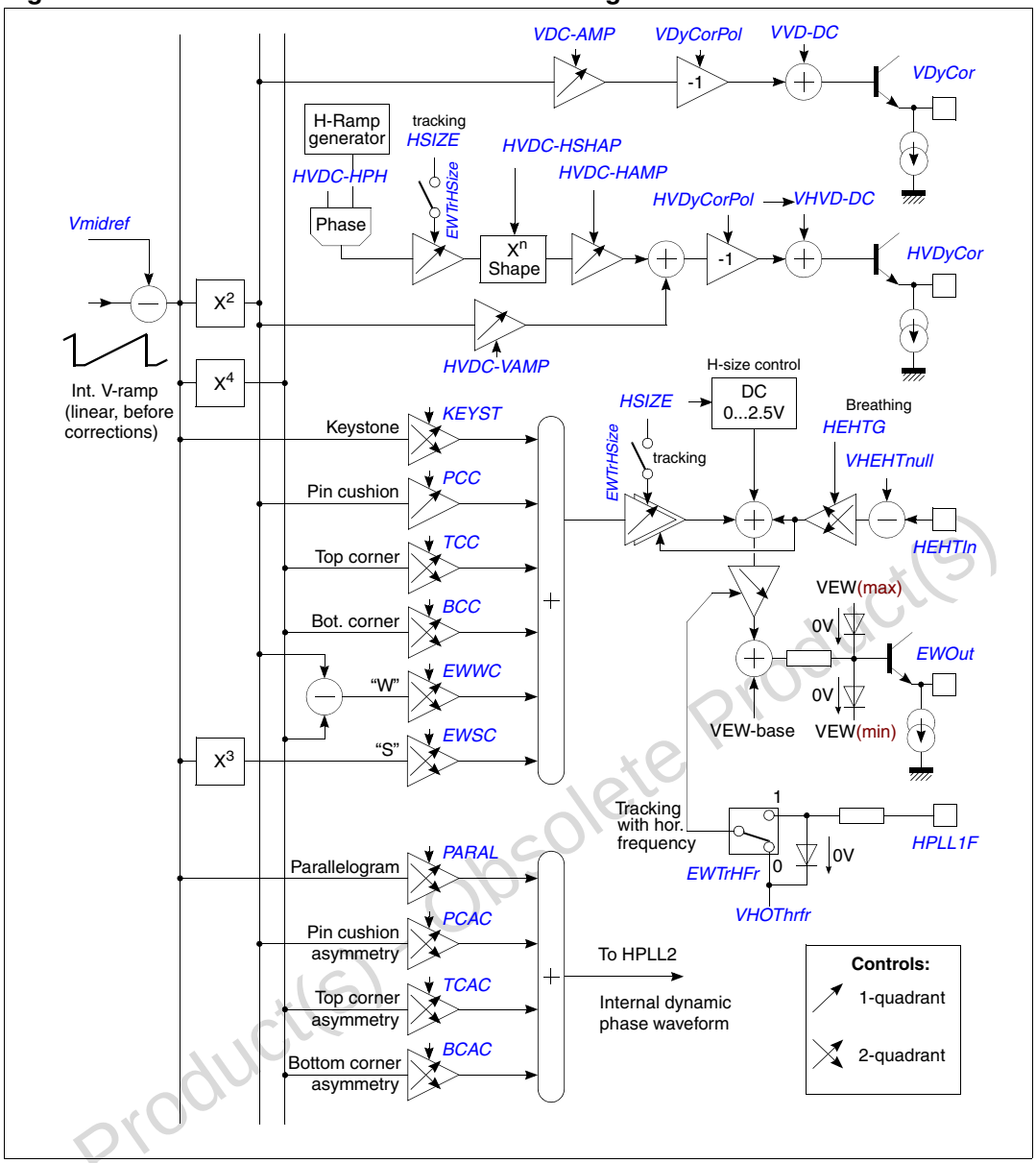
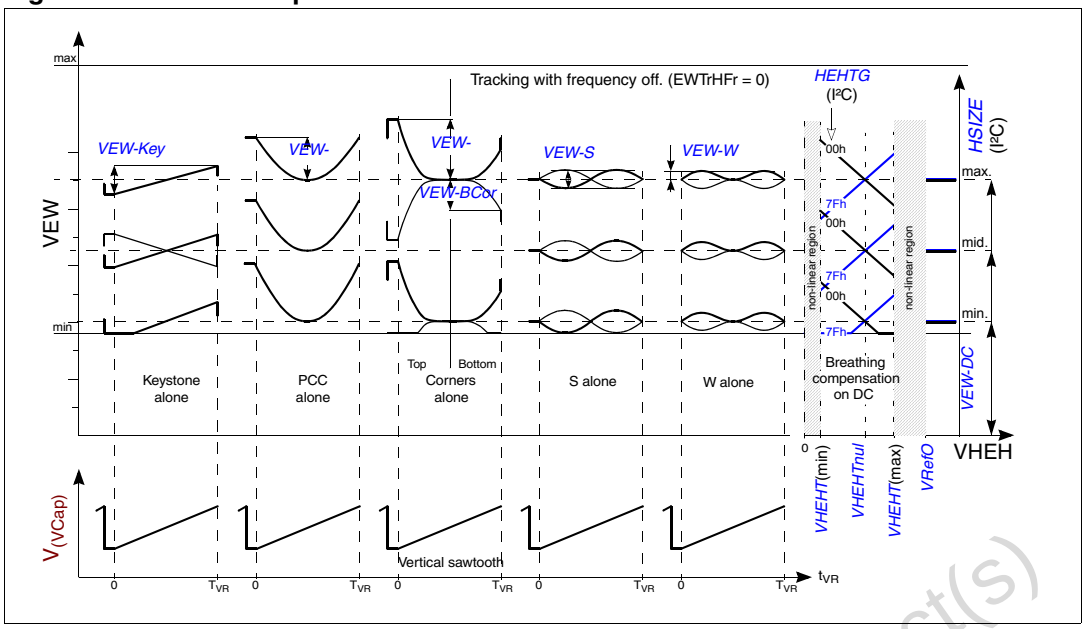


Figure 17. *EWOut* output waveforms



8.6 Dynamic correction outputs section

8.6.1 Composite horizontal and vertical dynamic correction output *HVDyCor*

A composite waveform is output on pin *HVDyCor*. It consists of a parabola of vertical deflection frequency, on which a parabola of horizontal deflection frequency is superimposed. The two parabolic components can independently be adjusted via I²C bus, the vertical parabola in amplitude (*HVDC-VAMP* I²C bus control), the horizontal parabola in amplitude, phase and shape (*HVDC-HAMP*, *HVDC-HPH* and *HVDC-HSHAP* I²C bus controls). The influence of the vertical component can be nullified by adjusting its control to minimum. For horizontal waveform component, refer to *Figure 18* and *Figure 19*. The minimum value in *HVDC-HAMP* I²C bus control does not correspond to null horizontal amplitude. The phase of the horizontal parabola can roughly be adjusted via *HDyCorPh* I²C bus bit for the waveform's start to coincide either with the beginning or the middle of the H-flyback pulse. Moreover, its centre can be offset via *HVDC-HPH* I²C bus control. The shape of the horizontal parabola can be adjusted via *HVDC-HSHAP* I²C bus control from a power-of-two to about a power-of-four. Between the waves of two subsequent lines, a flat is inserted at level corresponding to the beginning of the new wave. Putting *HDCFlatEn* and *HDyCorPh* to "1" will cause the flat part to begin at start of H-flyback and end a delay after its middle. Only this delay (its duration is quasi-constant) is applied when *HDCFlatEn* is at "0". Refer to electrical specifications for values.

The horizontal parabola component tracks with value in *HSIZE* control provided that *HDyCorTr* I²C bit is set to 1 (0 by default).

As the vertical parabola component is generated from the output vertical deflection drive waveform, it tracks with real vertical amplitude and position. It is not affected by C- and S-corrections or vertical breathing compensation. It does not track with *Vertical size after-gain* (Sadh) nor with *Vertical position offset* (Sadh) adjustments.

The polarity of the *HVDyCor* output can be adjusted via *HVDyCorPol* I²C bus bit.

8.6.2 Vertical dynamic correction output *VDyCor*

A parabola at vertical deflection frequency is available on pin *VDyCor*. Its amplitude is adjustable via *VDC-AMP* I²C bus control and polarity controlled via *VDyCorPol* I²C bus bit. It tracks with real vertical amplitude and position. It is not affected by C- and S-corrections or breathing compensation. It does not track with *Vertical size after-gain* (Sadh) nor with *Vertical position offset* (Sadh) adjustments.

The use of both correction waveforms is up to the application (e.g. dynamic focus, dynamic brightness control).

Figure 18. *HVDyCor* output horizontal component waveform

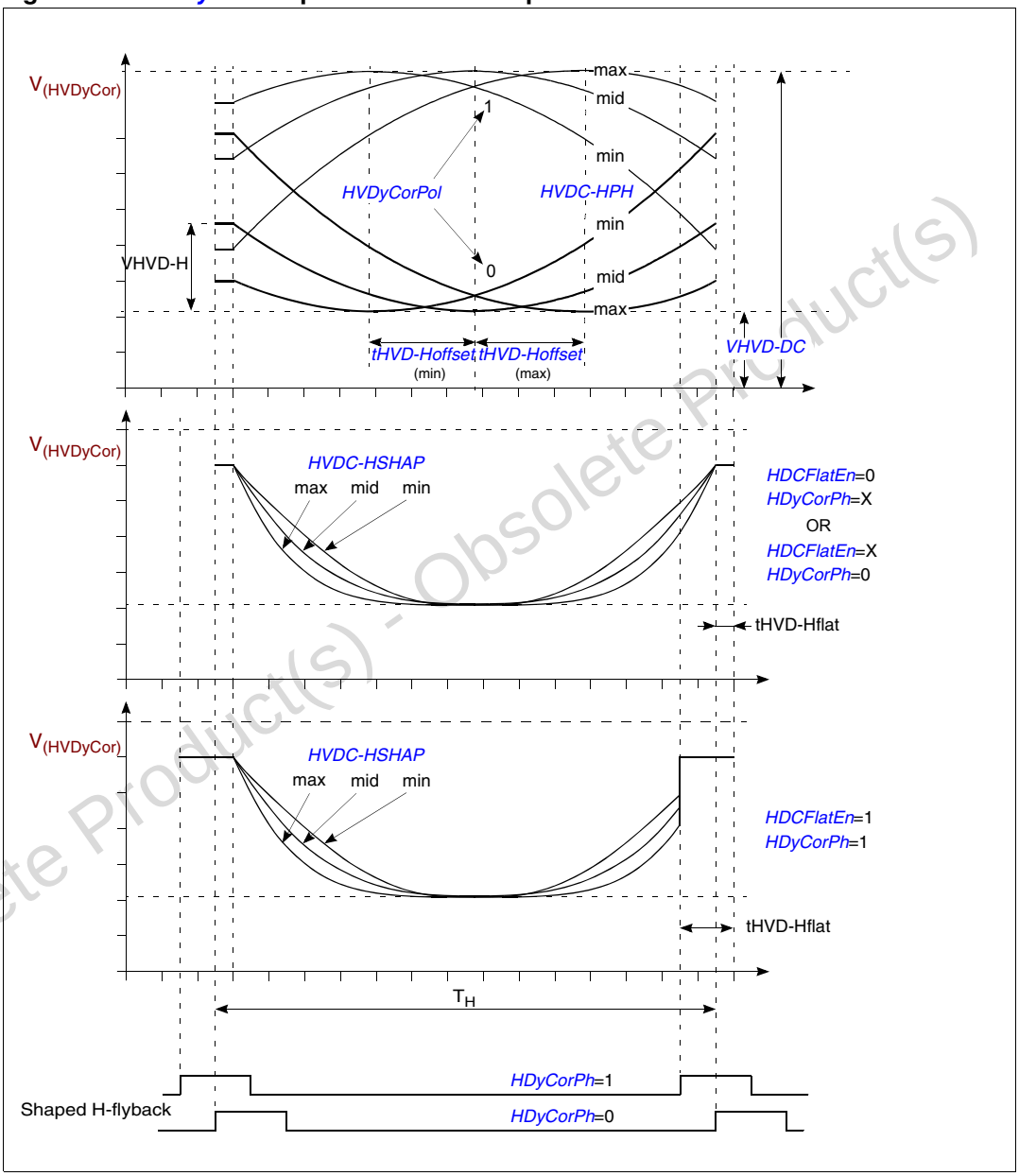
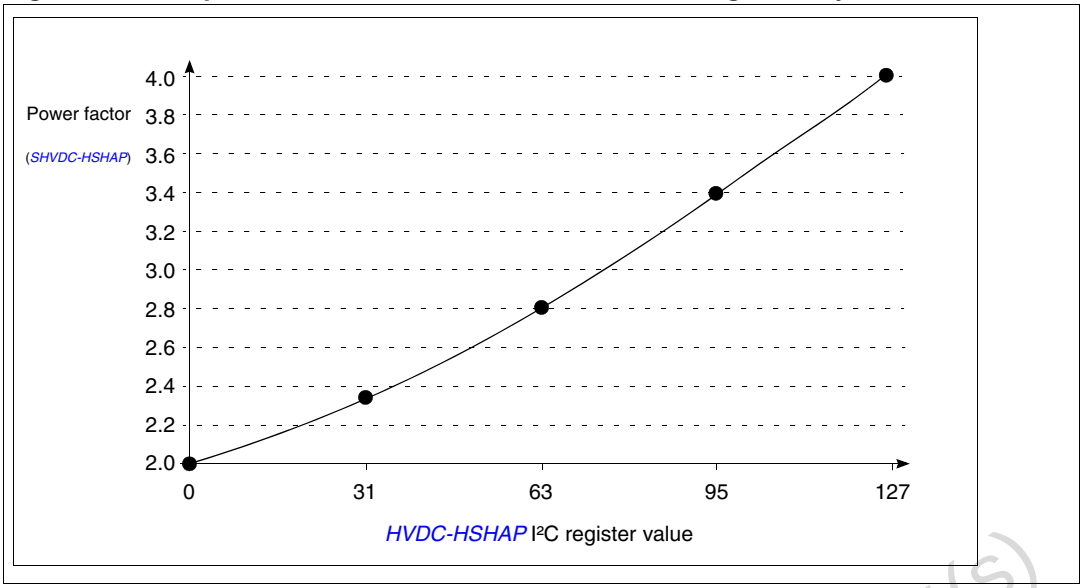


Figure 19. Shape characteristic versus *HVDC-HSHAP* register adjustment



8.7 DC/DC controller section

The section is designed to control a switch-mode DC/DC converter. A switch-mode DC/DC convertor generates a DC voltage from a DC voltage of different value (higher or lower) with little power losses. The DC/DC controller is synchronized to horizontal deflection frequency to minimize potential interference into the picture.

Its operation is similar to that of standard UC3842.

The schematic diagram of the DC/DC controller is in *Figure 20*. The *BOut* output controls an external switching circuit (a MOS transistor) delivering pulses synchronized on horizontal deflection frequency, the phase of which depends on H/W and I²C bus configuration. See the table at the end of this chapter. Their duration depends on the feedback provided to the circuit, generally a copy of DC/DC converter output voltage and a copy of current passing through the DC/DC converter circuitry (e.g. current through external power component). The polarity of the output can be controlled by *BOutPol* I²C bus bit. A NPN transistor open-collector is routed out to the *BOut* pin.

During the operation, a sawtooth is to be found on pin *BISense*, generated externally by the application. According to *BOutPh* I²C bus bit, the R-S flip-flop is set either at H-drive signal edge (rising or falling, depending on *BOHEdge* I²C bus bit), or a certain delay (tBTrigDel) after middle of H-flyback, or at horizontal frequency divided by two (phase corresponding to *VHOThrHi* on the VCO ramp). The output is set On at the end of the short pulse generated by the monostable trigger.

Timing of reset of the R-S flip-flop affects duty cycle of the output square signal and so the energy transferred from DC/DC converter input to its output. A reset edge is provided by comparator C2 if the voltage on pin *BISense* exceeds the internal threshold VThrBIsCurr. This represents current limitation if a voltage proportional to the current through the power component or deflection stage is available on pin *BISense*. This threshold is affected by voltage on pin *HPosF*, which rises at soft start and descends at soft stop. This ensures self-contained soft control of duty cycle of the output signal on pin *BOut*. Refer to *Figure 12*. Another condition for reset of the R-S flip-flop, OR-ed with the one described before, is that

the voltage on pin *BISense* exceeds the voltage V_{C2}, which depends on the voltage applied on input *BRegIn* of the error amplifier O1. The two voltages are compared, and the reset signal generated by the comparator C1. The error amplifier amplifies (with a factor defined by external components) the difference between the input voltage proportional to DC/DC convertor output voltage and internal reference VBReg. The internal reference and so the output voltage is I²C bus adjustable by means of *BREF* I²C bus control.

Both step-up (DC/DC converter output voltage higher than its input voltage) and step-down (output voltage lower than input) can be built.

8.7.1 Synchronization of DC/DC controller

For sake of application flexibility, the output drive signal on *BOut* pin can be synchronized with one of four events in *Table 17*. For the first line case, the synchronization instant is every second top of horizontal VCO saw tooth. See *Figure 9*.

8.7.2 Soft-start and soft-stop on B-drive

The soft-start and soft-stop procedure is carried out at each switch-on or switch-off of the B-drive signal, either via *HBOutEn* I²C bus bit or after reset of *XRayAlarm* I²C bus flag, to protect external power component. See *Figure 12* and sub chapter *Section 8.8.1*.

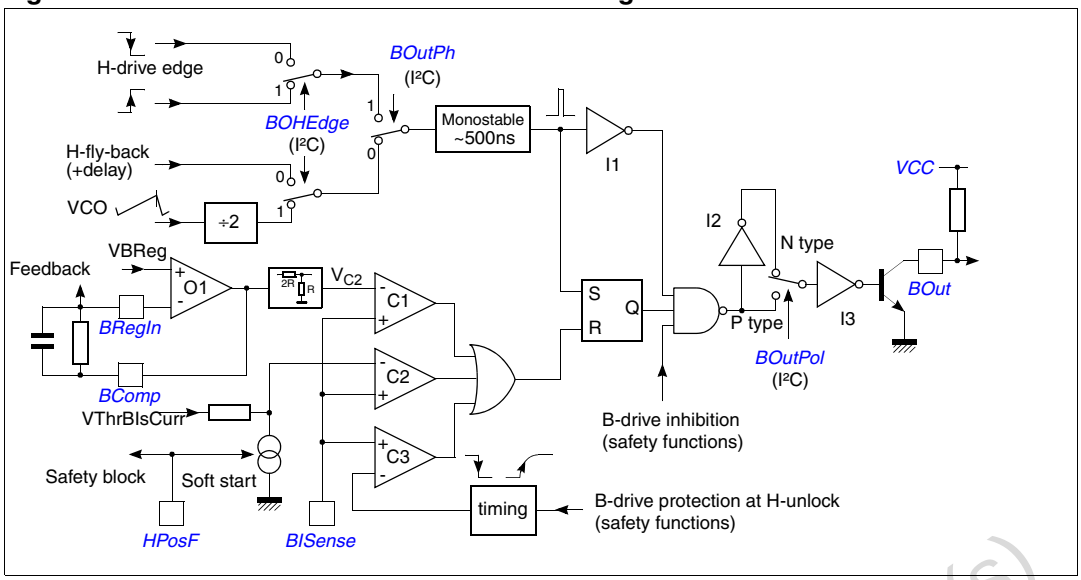
The drive signal on *BOut* pin can be switched off alone by means of *BMute* I²C bus bit, without switching off the drive signal on pin *HOut*. The switch-off is quasi-immediate, without the soft-stop procedure. At switching back on, the soft-start of the DC/DC controller is performed, timed by an internal timing circuit, see *Figure 20*.

When *BSafeEn* I²C bus bit is enabled, the drive signal on *BOut* pin will go off as soon as the horizontal PLL1 indicates unlocked state, without the soft-stop. Resuming of locked state will initiate the soft-start mechanism of the DC/DC controller, timed by an internal timing circuit.

Table 17. IDC/DC controller off-to-on edge timing

BOutPh **(Sadh/D7)**	***BOHEdge*** **(Sadh/D3)**	**Timing of off-to-on transition on *BOut* output**
0	1	VCO ramp top at Horizontal frequency divided by two
0	0	Middle of H-flyback plus tBTrigDel
1	0	Falling edge of H-drive signal
1	1	Rising edge of H-drive signal

Figure 20. DC/DC converter controller block diagram



8.8 Miscellaneous

8.8.1 Safety functions

The safety functions comprise supply voltage monitoring with appropriate actions, soft start and soft stop features on H-drive and B-drive signals on *HOut* and *BOut* outputs, B-drive cut-off at unlock condition and X-ray protection.

For supply voltage supervision, refer to *Section 8.1.1* and *Figure 3*. A schematic diagram putting together all safety functions and composite PLL1 lock and V-blanking indication is in *Figure 21*.

Soft start and soft stop function

For soft start and soft stop features for H-drive and B-drive signal, refer to *Section 8.3.6* and *Section 8.7*, respectively. See also the *Figure 12* and *Figure 13*. Regardless why the H-drive or B-drive signal are switched on or off (I²C bus command, power up or down, X-ray protection), the signals always phase-in and phase-out in the way drawn in the figures, the first to phase-in and last to phase-out being the H-drive signal, which is to better protect the power stages at abrupt changes like switch-on and off. The timing of phase-in and phase-out depends on the capacitance connected to *HPosF* pin which is virtually unlimited for this function. However, as it has a dual function (see *Section 8.3.1*), a compromise thereof is to be found.

The soft stop at power down condition can be considered as a special case. As at this condition the thresholds *VHOn*, *VBOn* and *VHBNorm* depend on the momentary level of supply voltage (marked *VHOn*', *VBOn*', *VHBNorm*' in *Figure 13*), the timing of soft stop mechanism depends, apart from the capacitance on *HPosF*, also on the falling speed of supply voltage. The device is capable of performing a correct soft stop sequence providing that, at the moment the supply voltage reaches *VCCStop*, the voltage on *HPosF* has already fallen below *VHOn* (*Section 8.8*).

B-drive cut-off at unlock condition

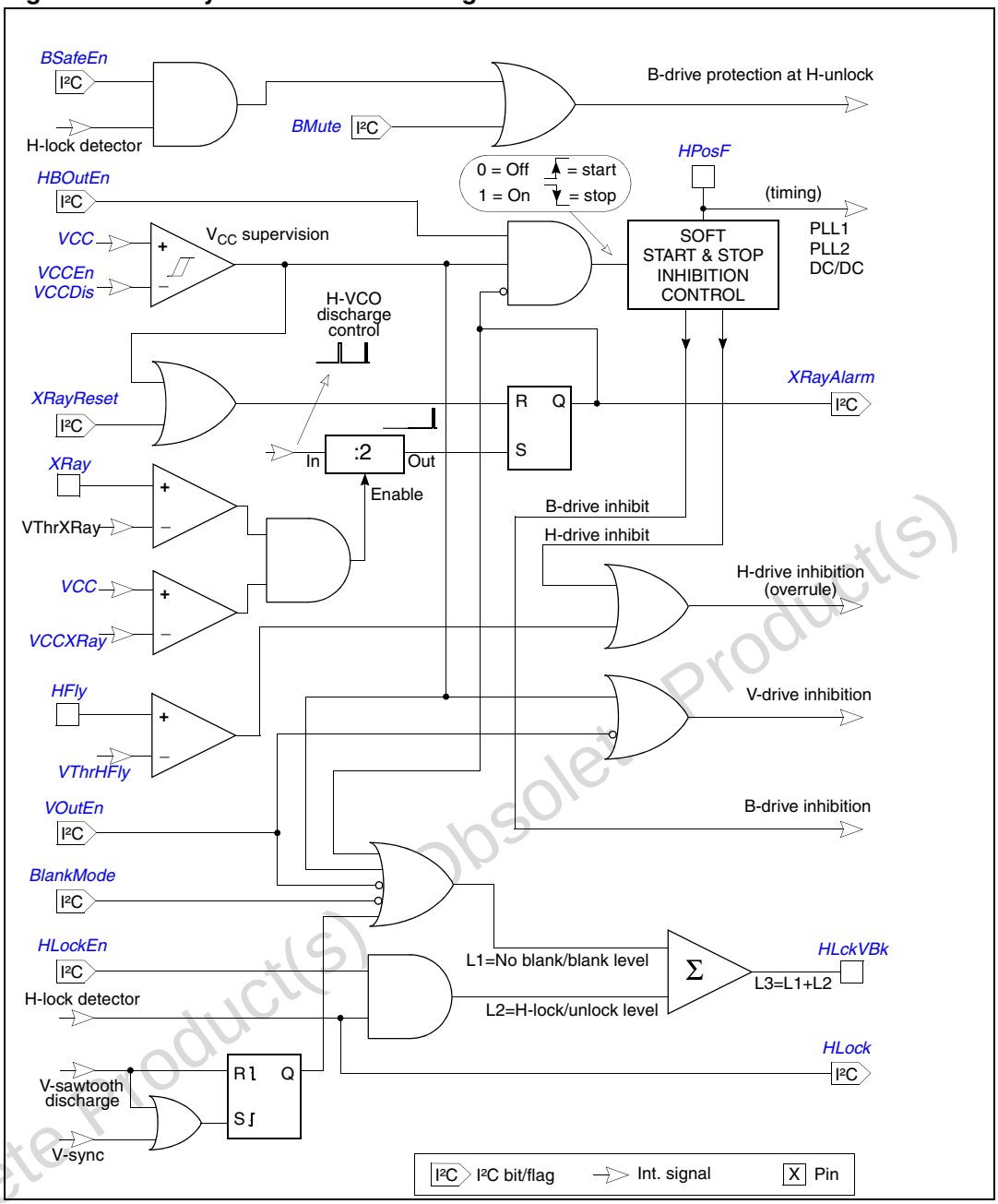
This function is described in *Section 8.7.2*.

X-ray protection

The X-ray protection is activated if the voltage level on *XRay* input exceeds VThrXRay threshold and if the *VCC* is higher than the voltage level *VCCXRayEn*. As a consequence, the H-drive and B-drive signals on *HOut* and *BOut* outputs are inhibited (switched off) after a 2-horizontal deflection line delay provided to avoid erratic excessive X-ray condition detection at short parasitic spikes. The *XRayAlarm* I²C bus flag is set to 1 to inform the MCU.

This protection is latched; it may be reset either by *VCC* drop or by I²C bus bit *XRayReset*.

Figure 21. Safety functions - block diagram



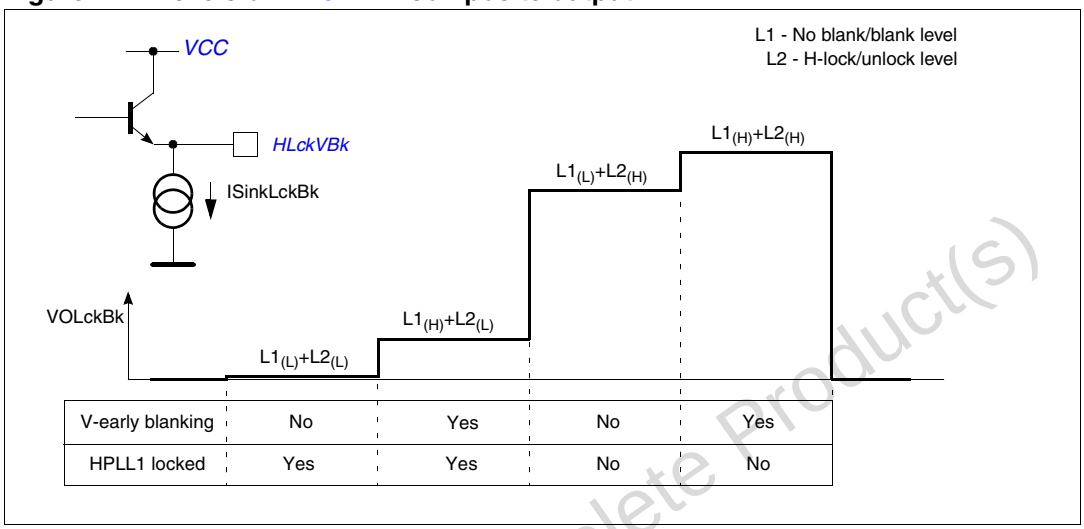
8.8.2 Composite output *HLckVBk*

The composite output *HLckVBk* provides, at the same time, information about lock state of PLL1 and early vertical blanking pulse. As both signals have two logical levels, a four level signal is used to define the combination of the two. Schematic diagram putting together all safety functions and composite PLL1 lock and V-blanking indication is in *Figure 21*, the combinations, their respective levels and the *HLckVBk* configuration in *Figure 22*.

The early vertical blanking pulse is obtained by a logic combination of vertical synchronization pulse and pulse corresponding to vertical oscillator discharge. The

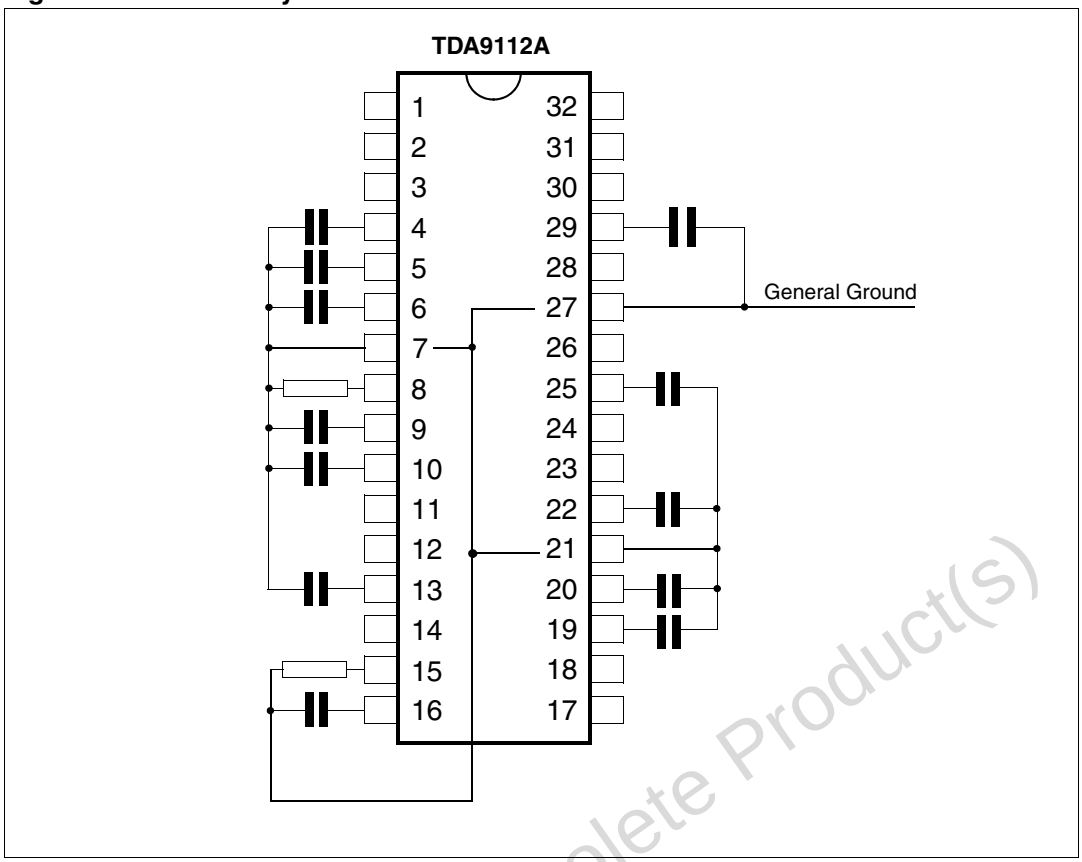
combination corresponds to the drawing in *Figure 22*. The blanking pulse is started with the leading edge of any of the two signals, whichever comes first. The blanking pulse is ended with the trailing edge of vertical oscillator discharge pulse. The device has no information about the vertical retrace time. Therefore, it does not cover, by the blanking pulse, the whole vertical retrace period. By means of *BlankMode* I²C bus bit, when at 1 (default), the blanking level (one of two according to PLL1 status) is made available on the *HLckVBk* permanently. The permanent blanking, irrespective of the *BlankMode* I²C bus bit, is also provided if the supply voltage is low (under *VCCEn* or *VCCDis* thresholds), if the X-ray protection is active or if the V-drive signal is disabled by *VOutEn* I²C bus bit.

Figure 22. Levels on *HLckVBk* composite output



V-early blanking	No	Yes	No	Yes
HPLL1 locked	Yes	Yes	No	No

Figure 23. Ground layout recommendations



9 Revision history

Table 18. Document revision history

Date	Revision	Changes
September 2003	1	Initial release
24-Mar-2009	2	New template applied, *Section 2.1: Environmentally-friendly packages* added

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