

Local Area Network (LIN) Enhanced Physical Interface with Selectable Slew Rate

Local Interconnect Network (LIN) is a serial communication protocol designed to support automotive networks in conjunction with Controller Area Network (CAN). As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The 33661 is a Physical Layer component dedicated to automotive LIN sub-bus applications. It offers slew rate selection for optimized operation at 10 kbps and 20 kbps, fast baud rate (above 100 kbps) for test and programming modes, excellent radiated emission performance, and safe behavior in the event of LIN bus short-to-ground or LIN bus leakage during low-power mode.

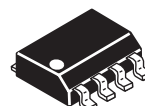
The 33661 is compatible with LIN Protocol Specification 2.0.

Features

- Operational from V_{SUP} 6.0 V to 18 V DC, Functional up to 27 V DC, and Handles 40 V During Load Dump
- Active Bus Waveshaping Offering Excellent Radiated Emission Performance
- 5.0 kV ESD on LIN Bus Pin
- 30 k Ω Internal Pullup Resistor
- LIN Bus Short-to-Ground or High Leakage in Sleep Mode
- -18 V to +40 V DC Voltage at LIN Pin
- 8.0 μ A in Sleep Mode
- Local and Remote Wake-Up Capability Reported by INH and RXD Pins
- 5.0 V and 3.3 V Compatible Digital Inputs Without Any External Components Required
- Pb-Free Packaging Designated by Suffix Code EF

33661

LIN PHYSICAL INTERFACE



D SUFFIX
EF SUFFIX (PB-FREE)
98ASB42564B
8-PIN SOICN

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33661D/R2	-40°C to 125°C	8 SOICN
MCZ33661EF/R2		

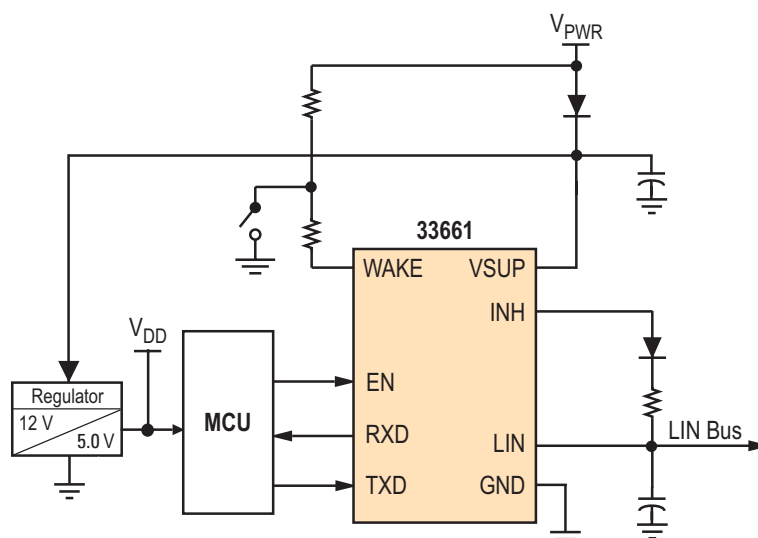


Figure 1. 33661 Simplified Application Diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

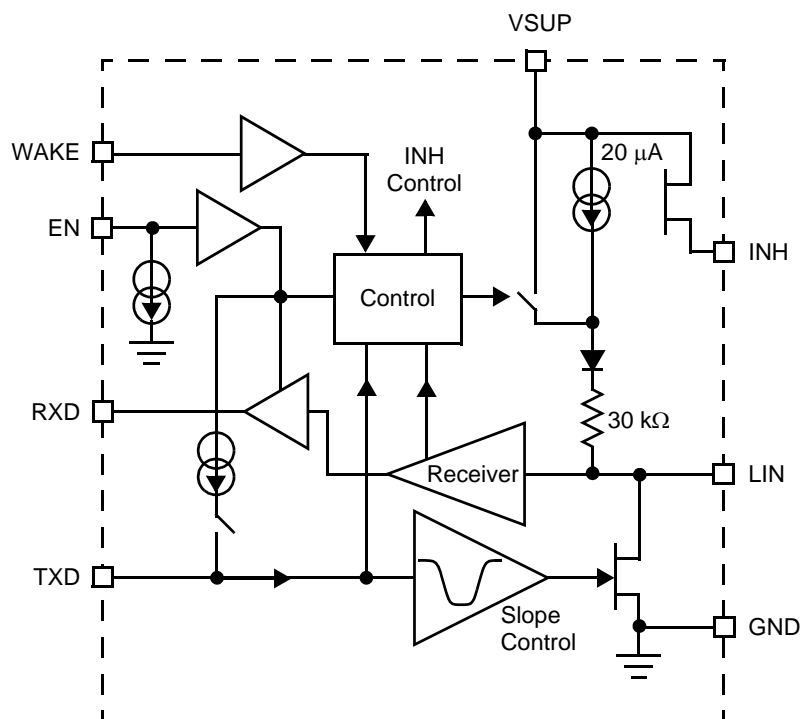


Figure 2. 33661 Simplified Internal Block Diagram

PIN CONNECTIONS

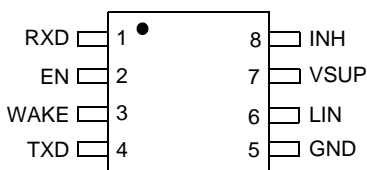


Figure 3. 33661 8-SOICN Pin Connections

Table 1. 33661 8-SOICN Pin Definitions

A functional description of each pin can be found in the [Functional Pin Description](#) section beginning on page [page 12](#).

Pin	Pin Name	Formal Name	Definition
1	RXD	Data Output	MCU interface that reports the state of the LIN bus voltage.
2	EN	Enable Control	Controls the operation mode of the interface.
3	WAKE	Wake Input	High-voltage input used to wake up the device from Sleep mode.
4	TXD	Data Input	MCU interface to control the state of the LIN output.
5	GND	Ground	Device ground pin.
6	LIN	LIN Bus	Bidirectional pin that represents the single-wire bus transmitter and receiver.
7	VSUP	Power Supply	Device power supply pin.
8	INH	Inhibit Output	This pin can have two main functions: controlling an external switchable voltage regulator having an inhibit input or driving a bus external resistor in the master node application.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage Continuous Supply Voltage Transient Voltage (Load Dump)	V _{SUP}	27 40	V
WAKE DC and Transient Voltage (Through a 33 kΩ Serial Resistor)	V _{WAKE}	-18 to 40	V
Logic Voltage (RXD, TXD, EN Pins)	V _{LOG}	-0.3 to 5.5	V
LIN Bus Voltage DC Voltage Transient (Coupled Through 1.0 nF Capacitor)	V _{BUS}	-18 to 40 -150 to 100	V
INH Voltage/Current DC Voltage DC Current	V _{INH} I _{INH}	-0.3 to V _{SUP} + 0.3 40	V mA
ESD Voltage ⁽¹⁾ Human Body Model All Pins LIN Pin with Respect to Ground Machine Model	V _{ESD1} V _{ESD2}	 ±2000 ±5000 ±200	V
THERMAL RATINGS			
Operating Temperature Ambient Junction	T _A T _J	-40 to 125 -40 to 150	°C
Storage Temperature	T _{STG}	-40 to 150	°C
Thermal Resistance, Junction to Ambient	R _{θJA}	150	°C/W
Peak Package Reflow Temperature During Reflow ^{(2), (3)}	T _{PPRT}	Note 3.	°C
Thermal Shutdown Temperature	T _{SHUT}	150 to 200	°C
Thermal Shutdown Hysteresis Temperature	T _{HYST}	8.0 to 20	°C

Notes

- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500$ Ω), ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP} = 220$ pF, $R_{ZAP} = 0$ Ω).
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx)], and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VSUP PIN (DEVICE POWER SUPPLY)					
Supply Voltage Nominal DC Functional DC, $T_A \geq 25^\circ\text{C}$	V_{SUP}	7.0 6.0	13.5 —	18.0 —	V
Supply Current in Sleep Mode $V_{\text{SUP}} \leq 13.5\text{ V}$, Recessive State $13.5\text{ V} < V_{\text{SUP}} < 18\text{ V}$ $V_{\text{SUP}} \leq 13.5\text{ V}$, Dominant State or Shorted to GND	I_{S1} I_{S2} I_{S3}	— — —	8.0 — 300	12 200 —	μA
Supply Current in Normal, Slow, or Fast Mode Bus Recessive, Excluding INH Output Current Bus Dominant, Total Bus Load $> 500\ \Omega$, Excluding INH Output Current	$I_{\text{S(REC)}}$ $I_{\text{S(DOM)}}$	— —	4.0 6.0	6.0 8.0	mA
RXD OUTPUT PIN (LOGIC)					
Low-Level Output Voltage $I_{\text{IN}} \leq 1.5\text{ mA}$	V_{OL}	0	—	0.9	V
High-Level Output Voltage $V_{\text{EN}} = 5.0\text{ V}$, $I_{\text{OUT}} \leq 250\ \mu\text{A}$ $V_{\text{EN}} = 3.3\text{ V}$, $I_{\text{OUT}} \leq 250\ \mu\text{A}$	V_{OH}	4.25 3.0	— —	5.25 3.5	V
TXD INPUT PIN (LOGIC)					
Low-Level Input Voltage	V_{IL}	—	—	1.2	V
High-Level Input Voltage	V_{IH}	2.5	—	—	V
Input Threshold Voltage Hysteresis	V_{INHYST}	100	300	800	mV
Pullup Current Source $V_{\text{EN}} = 5.0\text{ V}$, $1.0\text{ V} < V_{\text{TXD}} < 3.5\text{ V}$	I_{PU}	-60	-35	-20	μA
EN INPUT PIN (LOGIC)					
Low-Level Input Voltage	V_{IL}	—	—	1.2	V
High-Level Input Voltage	V_{IH}	2.5	—	—	V
Input Voltage Threshold Hysteresis	V_{INHYST}	100	300	800	mV
Low-Level Input Current $V_{\text{IN}} = 1.0\text{ V}$	I_{IL}	5.0	20	30	μA
High-Level Input Current $V_{\text{IN}} = 4.0\text{ V}$	I_{IH}	—	20	40	μA

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PIN (VOLTAGE EXPRESSED VERSUS V_{SUP} VOLTAGE)					
Low-Level Bus Voltage (Dominant State) External Bus Pullup $500\ \Omega$	V_{DOM}	—	—	1.4	V
High-Level Bus Voltage (Recessive State) TXD HIGH, $I_{\text{OUT}} = 1.0\ \mu\text{A}$	V_{REC}	$V_{\text{SUP}} - 1.0$	—	—	V
Internal Pullup Resistor to V_{SUP} (Normal Mode)	R_{PU}	20	30	47	$\text{k}\Omega$
Internal Pullup Current Source (Sleep Mode)	I_{PU}	—	20	—	μA
Overcurrent Shutdown Threshold	$I_{\text{OV-CUR}}$	50	75	150	mA
Leakage Current to GND Recessive State, $8.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $8.0\text{ V} \leq V_{\text{LIN}} \leq 18\text{ V}$ GND Disconnected, $V_{\text{GND}} = V_{\text{SUP}}$, V_{LIN} at -18 V V_{SUP} Disconnected, V_{LIN} at $+18\text{ V}$	I_{LEAK}	0 -1.0 —	3.0 — 1.0	20 1.0 10	μA mA μA
LIN Receiver, Low-Level Input Voltage TXD HIGH, RXD LOW	V_{LINL}	$0\ V_{\text{SUP}}$	—	$0.4\ V_{\text{SUP}}$	V
LIN Receiver, High-Level Input Voltage TXD HIGH, RXD HIGH	V_{LINH}	$0.6\ V_{\text{SUP}}$	—	V_{SUP}	V
LIN Receiver Threshold Center $(V_{\text{LINH}} - V_{\text{LINL}})/2$	V_{LINTH}	$0.475\ V_{\text{SUP}}$	$0.5\ V_{\text{SUP}}$	$0.525\ V_{\text{SUP}}$	V
LIN Receiver Input Voltage Hysteresis $V_{\text{LINH}} - V_{\text{LINL}}$	V_{LINHYST}	—	—	$0.175\ V_{\text{SUP}}$	V
LIN Wake-Up Threshold Voltage	V_{LINWU}	—	$0.5\ V_{\text{SUP}}$	—	V
INH OUTPUT PIN					
Driver ON Resistance (Normal Mode)	INH_{ON}	—	35	70	Ω
Leakage Current (Sleep Mode) $0\text{ V} < V_{\text{INH}} < V_{\text{SUP}}$	I_{LEAK}	0	—	5.0	μA
WAKE INPUT PIN					
Typical Wake-Up Threshold Voltage ($\text{EN} = 0\text{ V}$, $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$) ⁽⁵⁾ HIGH-to-LOW Transition LOW-to-HIGH Transition	V_{WUTH}	$0.3\ V_{\text{SUP}}$ $0.4\ V_{\text{SUP}}$	$0.43\ V_{\text{SUP}}$ $0.55\ V_{\text{SUP}}$	$0.55\ V_{\text{SUP}}$ $0.65\ V_{\text{SUP}}$	V
Wake-Up Threshold Voltage Hysteresis	V_{WUHYST}	$0.1\ V_{\text{SUP}}$	$0.16\ V_{\text{SUP}}$	$0.2\ V_{\text{SUP}}$	V
WAKE Input Current $V_{\text{WAKE}} < 27\text{ V}$	I_{WU}	—	1.0	5.0	μA

Notes

- 4 This parameter is guaranteed by design; however, it is not production tested.
- 5 When $V_{\text{SUP}} > 18\text{ V}$, the wake-up voltage thresholds remain identical to the wake-up thresholds at 18 V .

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^{\circ}\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN OUTPUT TIMING CHARACTERISTICS FOR NORMAL MODE					
Dominant Propagation Delay Time TXD to LIN ⁽⁶⁾					μs
Measurement Threshold (50% TXD to 58.1% V_{SUP})	$t_{\text{DOM}}(\text{MIN})$	—	—	50	
Measurement Threshold (50% TXD to 28.4% V_{SUP})	$t_{\text{DOM}}(\text{MAX})$	—	—	50	
Recessive Propagation Delay Time TXD to LIN ⁽⁶⁾					μs
Measurement Threshold (50% TXD to 42.2% V_{SUP})	$t_{\text{REC}}(\text{MIN})$	—	—	50	
Measurement Threshold (50% TXD to 74.4% V_{SUP})	$t_{\text{REC}}(\text{MAX})$	—	—	50	
Propagation Delay Time Symmetry					μs
$t_{\text{DOM}}(\text{MIN})$ to $t_{\text{REC}}(\text{MAX})$	dt_1	-10.44	—	8.12	
$t_{\text{DOM}}(\text{MAX})$ to $t_{\text{REC}}(\text{MIN})$	dt_2	-10.44	—	8.12	
LIN OUTPUT TIMING CHARACTERISTICS FOR SLOW MODE					
Dominant Propagation Delay Time TXD to LIN ⁽⁶⁾					μs
Measurement Threshold (50% TXD to 61.6% V_{SUP})	$t_{\text{DOM}}(\text{MIN})$	—	—	100	
Measurement Threshold (50% TXD to 25.1% V_{SUP})	$t_{\text{DOM}}(\text{MAX})$	—	—	100	
Recessive Propagation Delay Time TXD to LIN ⁽⁶⁾					μs
Measurement Threshold (50% TXD to 38.9% V_{SUP})	$t_{\text{REC}}(\text{MIN})$	—	—	100	
Measurement Threshold (50% TXD to 77.8% V_{SUP})	$t_{\text{REC}}(\text{MAX})$	—	—	100	
Propagation Delay Time Symmetry					μs
$t_{\text{DOM}}(\text{MIN})$ to $t_{\text{REC}}(\text{MAX})$	$dt_{1\text{S}}$	-21.88	—	17.44	
$t_{\text{DOM}}(\text{MAX})$ to $t_{\text{REC}}(\text{MIN})$	$dt_{2\text{S}}$	-21.88	—	17.44	
LIN OUTPUT DRIVER FAST MODE					
LIN Fast Slew Rate (Programming Mode)	dv/dt fast				$\text{V}/\mu\text{s}$
Fast Slew Rate		—	15	—	
LIN PIN					
Overcurrent Shutdown Delay Time ⁽⁷⁾	$t_{\text{OV-DELAY}}$	—	10	—	μs
LIN RECEIVER CHARACTERISTICS					
Receiver Dominant Propagation Delay Time ⁽⁸⁾					μs
LIN LOW to RXD LOW	t_{RL}	—	3.5	6.0	
Receiver Recessive Propagation Delay Time ⁽⁸⁾					μs
LIN HIGH to RXD HIGH	t_{RH}	—	3.5	6.0	
Receiver Propagation Delay Time Symmetry					μs
$t_{\text{RL}} - t_{\text{RH}}$	$t_{\text{R-SYM}}$	-2.0	—	2.0	

Notes

- 6 $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$. Bus load R_0 and C_0 : 1.0 nF/1.0 k Ω , 6.8 nF/660 Ω , 10 nF/500 Ω .
 7 This parameter is guaranteed by design; however, it is not production tested.
 8 Measured between LIN signal threshold V_{LINL} or V_{LINH} and 50% of RXD signal.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SLEEP MODE AND WAKE-UP TIMINGS					
EN Pin Wake-Up Time ⁽⁹⁾	t_{LWUE}	—	5.0	15	μs
WAKE Pin Filter Time ⁽¹⁰⁾	t_{WF}	10	—	70	μs
LIN Pin Wake-Up Filter Time (LIN Bus Wake-Up) ⁽¹¹⁾	t_{WUF}	40	70	120	μs
Sleep Mode Delay Time ⁽¹²⁾ EN HIGH-to-LOW	t_{SD}	50	—	—	μs
Delay for INH Turning off When Device Enters in Sleep Mode ^{(16), (17)} EN HIGH-to-LOW and INH HIGH-to-LOW	$t_{\text{SD_INH}}$	—	—	50	μs
Delay Time Between EN and TXD for Mode Selection ^{(13), (14)}	$t_{\text{D_MS}}$	5.0	—	—	μs
Delay Time Between First TXD after Device Mode Selection ^{(13), (14)}	$t_{\text{D_COM}}$	50	—	—	μs
FAST BAUD RATE TIMING					
Delay Entering Fast Baud Rate Using Toggle Function ⁽¹⁵⁾ EN LOW to EN HIGH	t_1	—	—	35	μs
Delay on EN Pin Resetting Fast Baud Rate to Previous Baud Rate ⁽¹⁵⁾ EN LOW to EN HIGH	t_2	—	—	5.0	μs

Notes

- 9 See [Figures 7](#) and [8, 10](#).
- 10 See [Figures 9](#) and [10, 10](#).
- 11 See [Figures 11](#) and [12, 11](#).
- 12 See [Figure 14a, 11](#).
- 13 See [Figures 7](#) through [12](#), pp. [10–11](#).
- 14 This parameter is guaranteed by design; however, it is not production tested.
- 15 See [Figure 13, 11](#).
- 16 No capacitor is connected to the INH pin. Measurement is done between the EN HIGH-to-LOW transition at 80% of INH voltage.
- 17 See [Figure 14b, 11](#).

TIMING DIAGRAMS

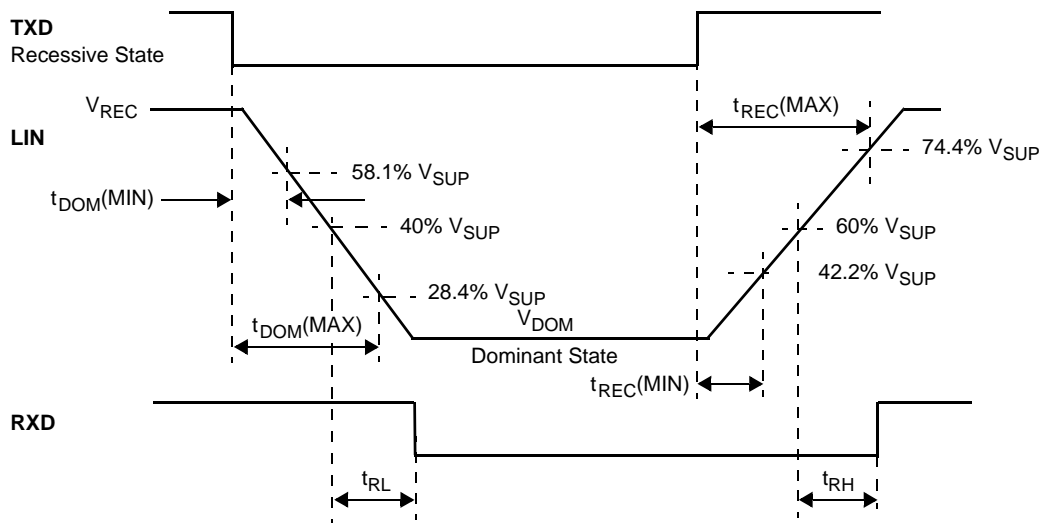


Figure 4. Normal Mode Bus Timing Characteristics

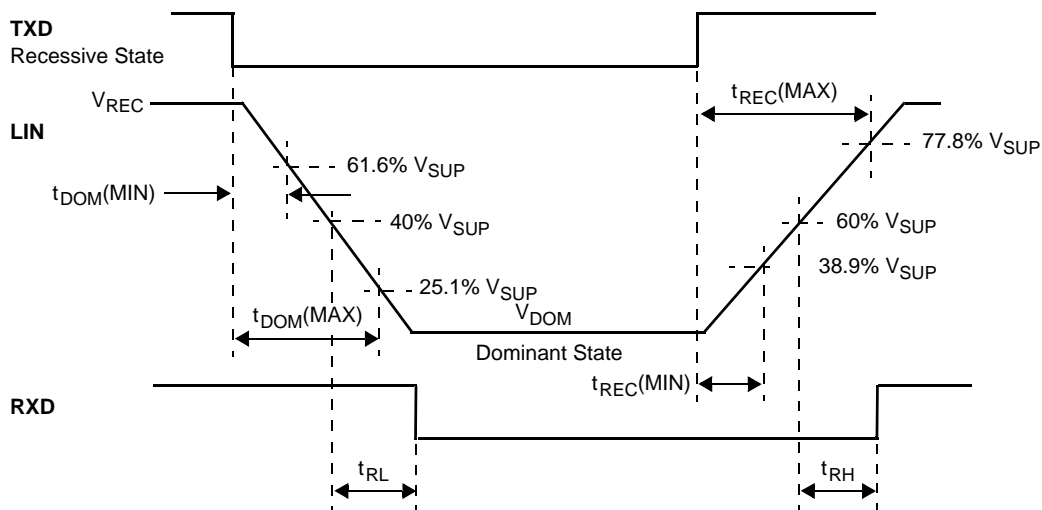
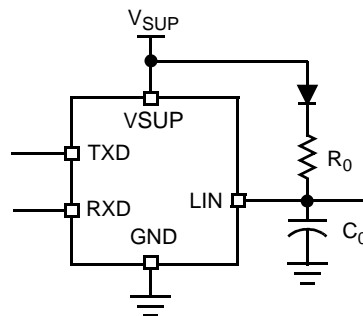


Figure 5. Slow Mode Bus Timing Characteristics



Note R_0 and C_0 : 1.0 k Ω /1.0 nF, 660 Ω /6.8 nF, and 500 Ω /10 nF.

Figure 6. Test Circuit for Timing Measurements

FUNCTIONAL DIAGRAMS

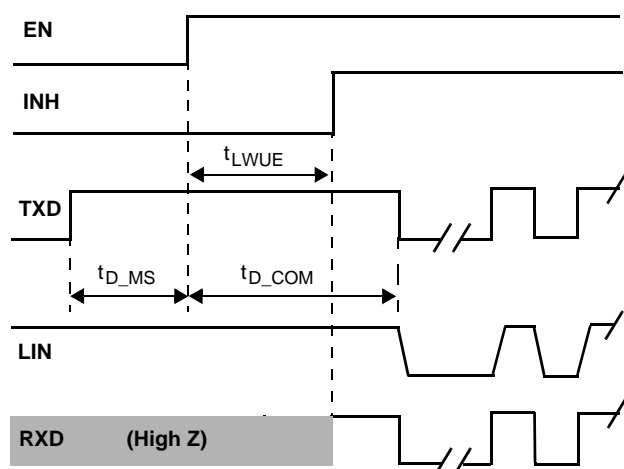


Figure 7. EN Pin Wake-Up and Normal Baud Rate Selection (1.0 kbps to 20 kbps)

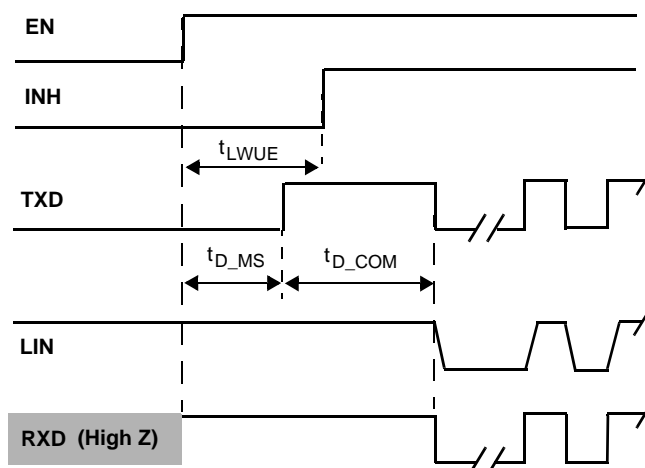


Figure 8. EN Pin Wake-Up and Slow Baud Rate Selection (1.0 kbps to 10 kbps)

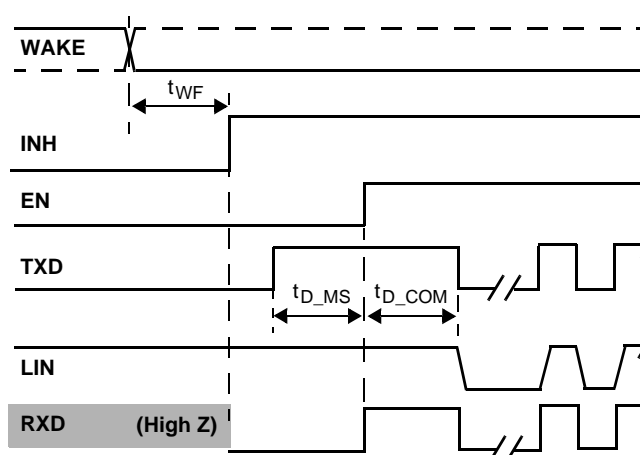


Figure 9. WAKE Pin Wake-Up and Normal Baud Rate Selection (1.0 kbps to 20 kbps)

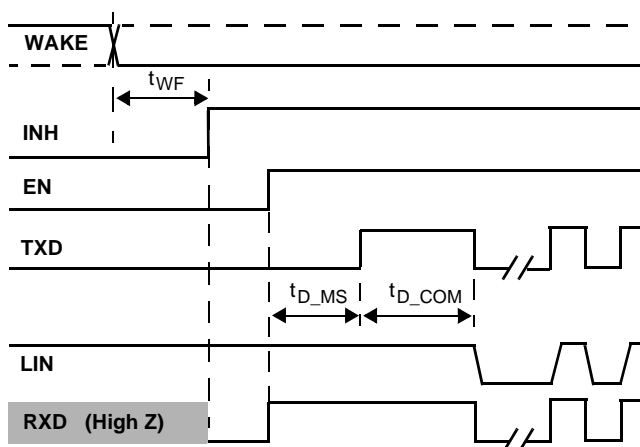


Figure 10. WAKE Pin Wake-Up and Slow Baud Rate Selection (1.0 kbps to 10 kbps)

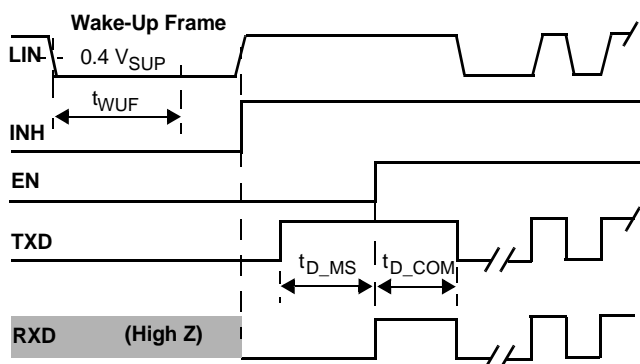


Figure 11. LIN Bus Wake-Up and Normal Baud Rate Selection (1.0 kbps to 20 kbps)

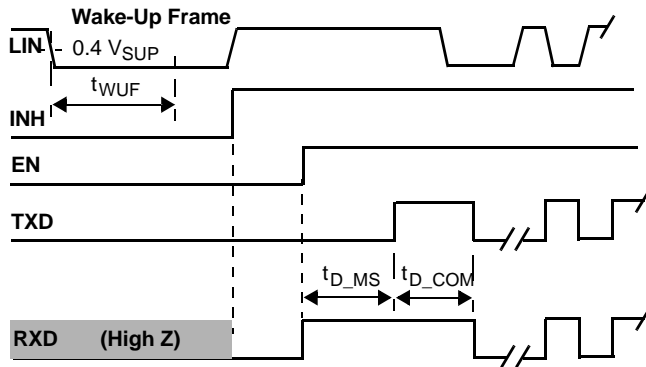


Figure 12. LIN Bus Wake-Up and Slow Baud Rate Selection (1.0 kbps to 10 kbps)

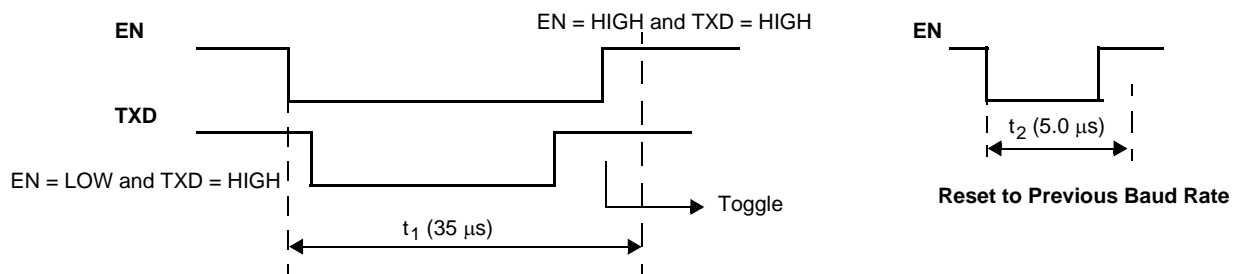


Figure 13. Fast Baud Rate Selection (Toggle Function)

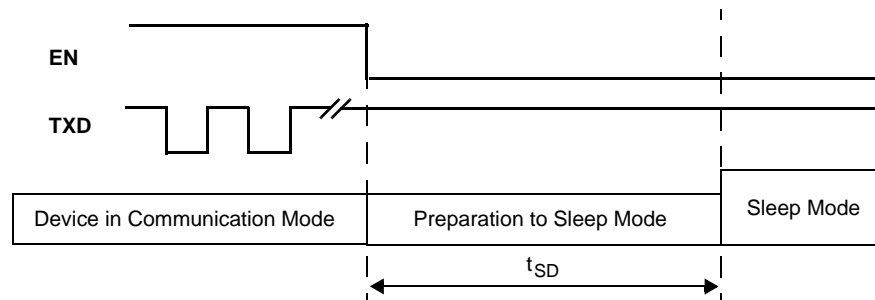


Figure 14a

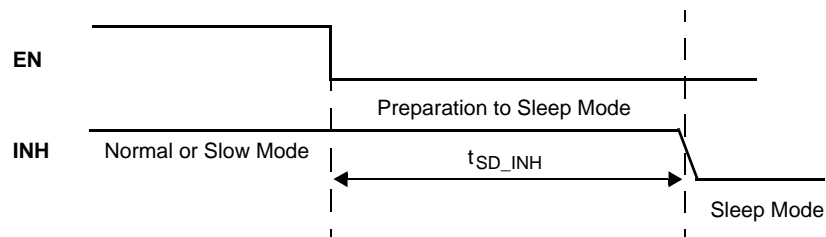


Figure 14b

Figure 14. Sleep Mode Enter

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33661 is a Physical Layer component dedicated to automotive LIN sub-bus applications.

The 33661 features include slew rate selection for optimized operation at 10 kbps and 20 kbps, fast baud rate for test and programming modes, excellent radiated emission

performance, and safe behavior in case of LIN bus short-to-ground or LIN bus leakage during low power mode.

Digital inputs are 5.0 V and 3.3 V compatible without any external component required.

The INH output may be used to control an external voltage regulator or to drive a LIN bus pullup resistor.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY PIN (VSUP)

The VSUP supply pin is the power supply pin for the 33661. The pin is connected to a battery through a serial diode for reverse battery protection. The DC operating voltage is from 7.0 V to 27 V. This pin sustains standard automotive voltage conditions such as 27 V DC during jump-start conditions and 40 V during load dump. Supply current in the Sleep mode is typically 8.0 μ A.

GROUND PIN (GND)

In case of a ground disconnection at the module level, the 33661 does not have significant current consumption on the LIN bus pin when in the recessive state. (Less than 100 μ A is sourced from LIN bus pin, which creates 100 mV drop voltage from the 1.0 k Ω LIN bus pullup resistor.)

LIN BUS PIN (LIN)

This I/O pin represents the single-wire bus transmitter and receiver.

Transmitter Characteristics

The LIN driver is a low-side MOSFET with internal overcurrent thermal shutdown. An internal pullup resistor with a serial diode structure is integrated so no external pullup components are required for the application in a slave node. An additional pullup resistor of 1.0 k Ω must be added when the device is used in the master node.

Voltage can go from -18 V to 40 V without current other than the pullup resistance. The LIN pin exhibits no reverse current from the LIN bus line to VSUP, even in the event of GND shift or V_{PWR} disconnection.

The transmitter has two slew rate selections: 20 kbps (normal slew rate) and 10 kbps (slow slew rate). The slow slew rate can be used to improve radiated emissions.

Receiver Characteristics

The receiver thresholds are ratiometric with the device supply pin.

DATA INPUT PIN (TXD)

The TXD input pin is the MCU interface to control the state of the LIN output. When TXD is LOW, LIN output is LOW; when TXD is HIGH, the LIN output transistor is turned OFF. The threshold is 3.3 V and 5.0 V compatible. The baud rate selection (normal or Slow mode) is done at device wake-up by the state of the TXD pin prior to a HIGH level at the EN pin (see [Figures 7](#) through [12](#), pp. [10–11](#)).

DATA OUTPUT PIN (RXD)

The RXD output pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive) is reported by a high voltage on RXD; LIN LOW (dominant) is reported by a low voltage on RXD. The RXD output structure is a CMOS-type push-pull output stage.

The low level is fixed. The high level is dependant on the EN voltage. If EN is set at 3.3 V, RXD V_{OH} is 3.3 V. If EN is set at 5.0 V, RXD V_{OH} is 5.0 V.

In the Sleep mode, RXD is high impedance. When a wake-up event is recognized from WAKE pin or from the LIN bus pin, RXD is pulled LOW to report the wake-up event. An external pullup resistor may be needed.

ENABLE INPUT PIN (EN)

The EN input pin controls the operation mode of the interface. If EN = 1, the interface is in Normal mode, with transmission path from TXD to LIN and from LIN to RXD both active. The threshold is 3.3 V and 5.0 V compatible. The high level at EN defines the V_{OH} at RXD. The Sleep mode is entered by setting EN LOW while TXD is HIGH. Sleep mode is active after the t_{SD} filter time (see [Figure 14](#), [11](#)).

INHIBIT OUTPUT PIN (INH)

The INH output pin may have two main functions. It may be used to control an external switchable voltage regulator having an inhibit input. The high drive capability also allows it to drive the bus external resistor in the master node application. This is illustrated in [Figures 18](#) and [19](#), [17](#).

In Sleep mode, INH is turned OFF. If a voltage regulator inhibit input is connected to INH, the regulator will be disabled. If the master node pullup resistor is connected to INH, the pullup resistor will be disabled from the LIN bus.

WAKE INPUT PIN (WAKE)

The WAKE pin is a high-voltage input used to wake up the device from the Sleep mode. WAKE is usually connected to an external switch in the application. The typical wake thresholds are $V_{SUP}/2$.

The WAKE pin has a special design structure and allows wake-up from both HIGH-to-LOW or LOW-to-HIGH transitions. When entering into Sleep mode, the LIN monitors the state of the WAKE pin and stores it as a reference state. The opposite state of this reference state will be the wake-up event used by the device to enter again into Normal mode.

An internal filter is implemented (40 μ s typical filtering time delay). WAKE pin input structure exhibits a high impedance, with extremely low input current when voltage at this pin is below 14 V. When voltage at the WAKE pin exceeds 14 V, input current starts to sink into the device. A series resistor should be inserted in order to limit the input current mainly during transient pulses. Recommended resistor value is 33 k Ω .

Important The WAKE pin should *not* be left open. If the wake-up function is not used, WAKE should be connected to ground to avoid false wake-up.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

As described below and depicted in [Figure 15](#) and [Table 5](#) on [15](#), the 33661 has two operational modes, Normal and Sleep. Normal mode may be adjusted to improve radiated emissions by changing the slew rate of the LIN bus output to Fast or Slow mode. In addition, there are two transitional modes: Awake Mode, which allows the device to go in Normal or Slow mode, and Wait Slow mode, which is a temporary state before the device enters the Slow mode.

NORMAL MODE

In the Normal mode, the 33661 has slew rate and timing compatible with the LIN protocol specification and operates from 1.0 kbps to 20 kbps. This mode is selected after Sleep mode by setting the TXD pin HIGH prior to setting EN from LOW to HIGH. Once Normal mode is selected, it is impossible to select the Slow mode unless the 33661 is set to Sleep mode.

Slow Mode

In the Slow mode, the slew rate is around half the normal slew rate, and bus speed operation ranges from 1.0 kbps to 10 kbps. The radiated emission is significantly reduced compared to the already excellent emission level of the Normal mode. Slow mode is entered after Sleep mode by setting the TXD pin LOW prior to setting EN from LOW to HIGH. Once the Slow mode is selected, it is impossible to select the Normal mode unless the device is set to Sleep mode.

Fast Mode

In the Fast mode, the slew rate is around 10 times faster than the Normal mode. This allows very fast data transmission (>100 kbps)—for instance, for electronic control unit (ECU) tests and microcontroller program download. The bus pullup resistor might be reduced to ensure a correct RC time constant in line with the high baud rate used.

Fast mode can be selected from either Normal or Slow mode. Fast mode is entered via a special sequence (called toggle function) as follows: TXD and EN pins set LOW, then TXD pulled HIGH, and at the EN pin LOW-to-HIGH transition, the device enters into the Fast Baud Rate. The duration of this sequence must be less than 35 μ s. The toggle function is described in [Figure 13](#), [11](#). Once in the Fast mode, two different procedures will bring the device back to the previously selected mode (Normal or Slow):

- The toggle function already described.
- A glitch on EN where $t_2 < 5.0 \mu$ s also resets the device to the previously selected mode (Normal or Slow) ([Figure 13](#)).

SLEEP MODE

In the Sleep mode, the transmission path is disabled and the 33661 is in low power mode. Supply current from V_{SUP} is very low. Wake-up can occur from LIN bus activity from node internal wake-up through the EN pin and from the WAKE input pin.

In the Sleep mode, the 33661 has an internal 20 μ A pullup source to V_{SUP} . This avoids the high current path from the battery to ground in the event the bus is shorted to ground. (Refer to succeeding paragraphs describing wake-up behavior.)

DEVICE POWER-UP (AWAKE TRANSITIONAL MODE)

At power-up (V_{SUP} rises from zero), the 33661 automatically switches to the Awake transitional mode. It switches the INH pin to HIGH state and RXD to LOW state. The MCU of the application will then confirm Normal or Slow mode by setting the TXD and EN pins appropriately.

DEVICE WAKE-UP EVENTS

The 33661 can be awakened from Sleep mode by three wake-up events:

- Remote wake-up via LIN bus activity
- Internal node wake-up via the EN pin
- Toggling the WAKE pin

Remote Wake from LIN Bus (Awake Transitional Mode)

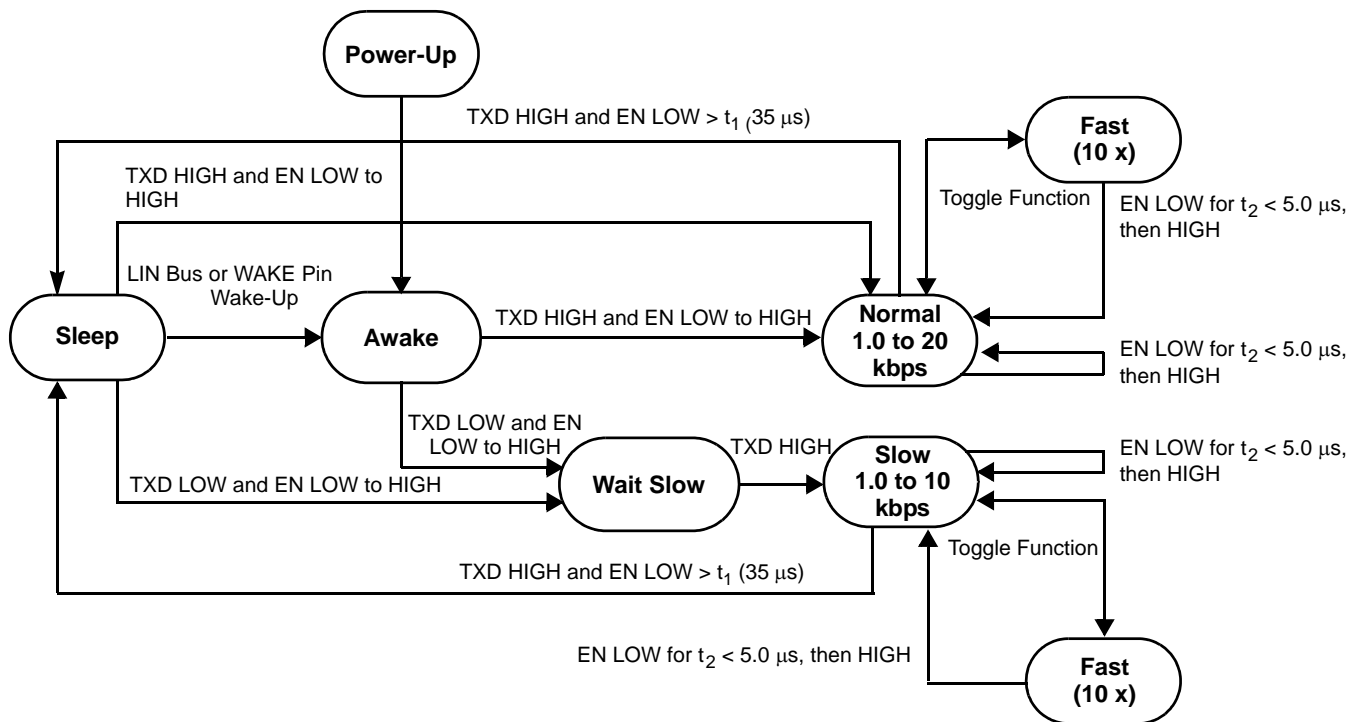
The LIN bus wake-up is recognized by a recessive-to-dominant transition, followed by a dominant level with a duration greater than 70 μ s, followed by a dominant-to-recessive transition. This is illustrated in [Figures 11](#) and [12](#) on [11](#). Once the wake-up is detected, the 33661 enters the Awake transitional mode, with INH HIGH and RXD pulled LOW.

Wake-Up from Internal Node Activity (Normal or Wait Slow Mode)

The 33661 can wake up by internal node activity through a LOW-to-HIGH transition of the EN pin. When EN is switched from LOW to HIGH, the device is awakened and enters either the Normal or the Wait Slow transitional mode depending on the level of TXD input. The MCU must set the TXD pin LOW or HIGH prior to waking up the device through the EN pin.

Wake-Up from WAKE Pin (Awake Transitional Mode)

If the WAKE input pin is toggled, the 33661 enters the Awake transitional mode, with INH HIGH and RXD pulled LOW.



Note Refer to Table 5 for explanation.

Figure 15. Operational and Transitional Modes State Diagram

Table 5. Explanation of Operational and Transitional Modes State Diagram

Operational/ Transitional	LIN	INH	EN	TXD	RXD
Sleep Mode	Recessive state, driver off. 20 μ A pullup current source.	LOW	LOW	X	High impedance. HIGH if external pullup to V_{DD} .
Awake	Recessive state, driver off. 30 k Ω pullup active.	HIGH	LOW	X	LOW. If external pullup, HIGH-to-LOW transition reports wake-up.
Normal Mode	Driver active. 30 k Ω pullup active. Slew rate normal (20 kbps).	HIGH	HIGH	HIGH to enter Normal mode. Once in Normal mode: LOW to drive LIN bus in dominant, HIGH to drive LIN bus in recessive.	Report LIN bus level: • Low LIN bus dominant • High LIN bus recessive
Wait Slow	Recessive state. Driver off. 30 k Ω pullup active.	HIGH	HIGH	LOW	HIGH
Slow	Driver active. 30 k Ω pullup active. Slew rate slow (10 kbps).	HIGH	HIGH	LOW to enter Slow mode. Once in Slow mode: LOW to drive LIN bus in dominant, HIGH to drive LIN bus in recessive.	Report LIN bus level: • Low LIN bus dominant • High LIN bus recessive
Fast	Driver active. 30 k Ω pullup active. Slew rate fast (> 100 kbps).	HIGH	HIGH	LOW to drive LIN bus in dominant, HIGH to drive LIN bus in recessive.	Report LIN bus level: • Low LIN bus dominant • High LIN bus recessive

X = Don't care.

ELECTROMAGNETIC COMPATIBILITY

RADIATED EMISSION IN NORMAL AND SLOW MODES

The 33661 has been tested for radiated emission

performances. [Figures 16](#) and [17](#) show the results in the frequency range 100 kHz to 2.0 MHz. Test conditions are in accordance with CISPR25 recommendations, bus length of

1.5 meters, device loaded with 10 nF and 500 Ω bus impedance.

[Figure 16](#) displays the results when the device is set in the Normal mode, optimized for baud rate up to 20 kbps.

[Figure 17](#) displays the results when the device is set in the Slow mode, optimized for baud rate up to 10 kbps. The level of emissions is significantly reduced compared to the already excellent level of the Normal mode.

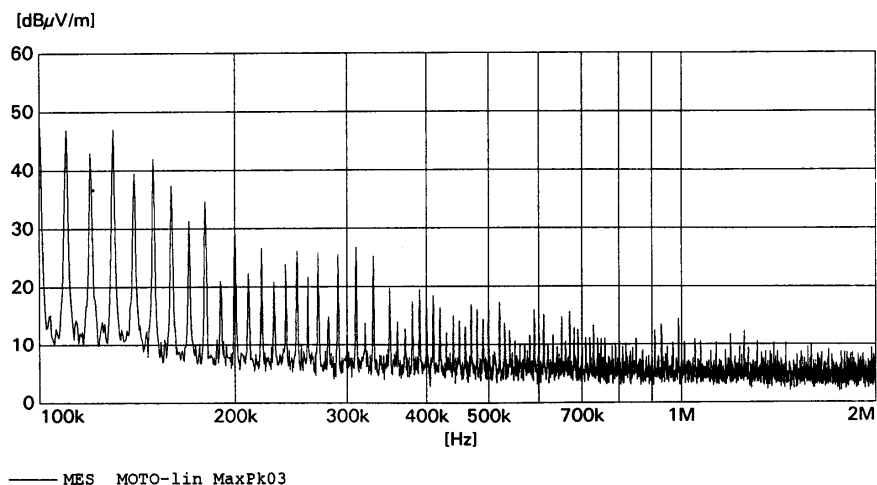


Figure 16. Radiated Emission in Normal Mode

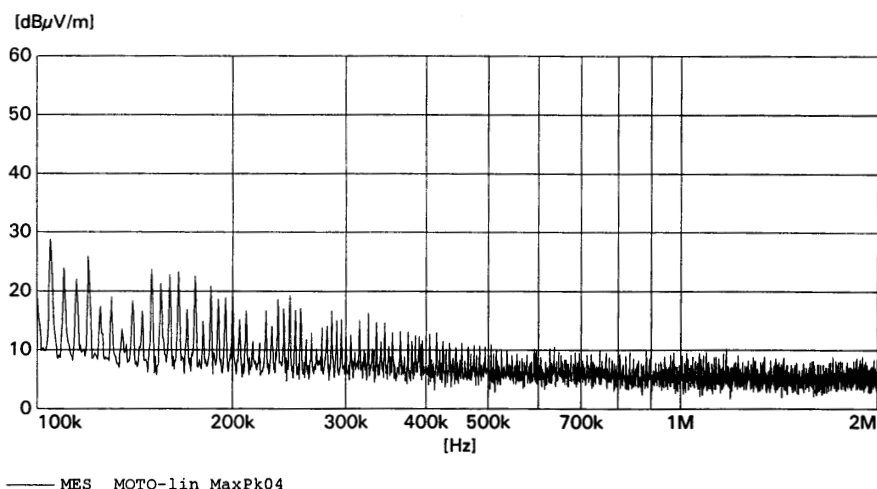


Figure 17. Radiated Emission in Slow Mode

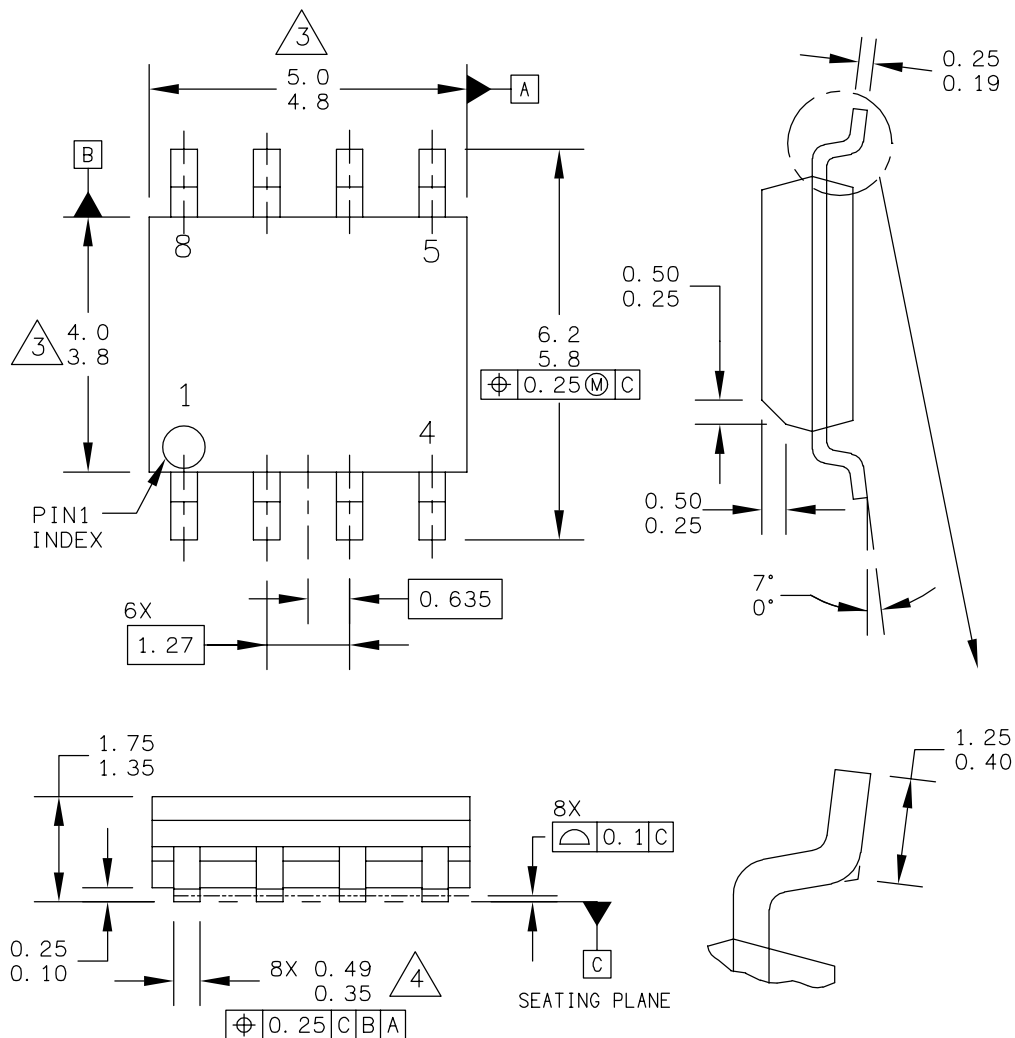
An additional pullup resistor of 1.0 kΩ in series with a diode must be added when the device is used in the master node.



PACKAGING

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98A drawing number below.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: 8LD SOIC NARROW BODY		DOCUMENT NO: 98ASB42564B		REV: U	
		CASE NUMBER: 751-07		07 APR 2005	
		STANDARD: JEDEC MS-012AA			

D SUFFIX
EF SUFFIX (PB-FREE)
8-PIN SOIC NARROW BODY
PLASTIC PACKAGE
98ASB42564B
ISSUE U

REFERENCE DOCUMENTS**Table 6. Reference Documents**

Title	Literature Number
Local Interconnect Network (LIN) Physical Interface: Difference Between MC33399 and MC33661	EB215

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
5.0	10/2006	<ul style="list-style-type: none">• Implemented Revision History page• Updated the Freescale format and style• Added MCZ33661EF/R2 to the part number Ordering Information
6.0	11/2006	<ul style="list-style-type: none">• Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from MAXIMUM RATINGS on page 4. Added note with instructions from www.freescale.com.

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2006. All rights reserved.