MC68360

Preliminary Information

MC68360 New Features on REV C.1

March 7, 1995

Some new features have been added to the XC68360 Revision C.1 device. The uses of these new features are not required with an exception of hardware device errata fixes. The main purpose of the revision C.1 device is to fix the errata items that is described on the QUICC Device Errata as "will be fixed on rev C.1".

Revision C.1 device is visually marked with mask number 1E68C. The RISC revision number in the XC68360 at address (MiscBase+$00) has the value $0003.

NOTE

The following information is not described in the MC68360 User's Manual (MC68360UM/AD). The use of this document along with the QUICC Device Errata, QUICC Users Manual Errata, Changes in Rev B, the Centronics Controller Manual and the User's Manual will fully describe revision C.1 device operation. All of this information will be incorporated into a future revision of the User's Manual.

CPM

DUAL PORT RAM

256 Bytes of memory have been added to the internal RAM of the part. The memory map on page 3-3 of the User's Manual should now reflect that the area from DPRBASE + $700 to DPRBASE + $7FF now contains 256 bytes of memory in Dual-Port RAM which contains User Data / BDs / Microcode Scratch.

NOTE

This extra memory will not be available if a RAM microcode package is installed in the QUICC.

SMC

UART MODE

SMC Event Register (SMCE)

The SMC UART event register has one new bit. The width and the location of the register has not changed. The definition of the new bits is as follows:

Bit 6 BRKe (End of Break Sequence Received)

This bit is set when the end of a break sequence is received on the SMC UART receiver.

PARALLEL I/O PORTS

PORT A

Two new multiplexing options have been added to Port A. Table 7-16 on page 7-351 should show the following new options:

PAPAR(0)=1 and PADIR(0)=1 results in Signal PA0 being used as RXD4 (Only if PA6 is not being used as RXD4)

PAPAR(1)=1 and PADIR(1)=1 results in Signal PA1 being used as TXD4

SERIAL INTERFACE

SI RAM ENTRIES

A loop back option has been added in each time slot in the SI. This option is set by a new bit in each entry in the SI RAM. The width of the entry has not changed. The definition of the new bits is as follows

Bit 15 LOOP (Loop back this time slot)

Set this bit when you wish to perform a loop back on this time slot

0 = normal mode
1 = loop back mode for this time slot

SERIAL INTERFACE SYNCHRONIZATION

In previous versions of the QUICC, the SI would reset itself if an unexpected sync pulse was seen during the middle of a time frame. This would cause the SI to sync again on the following sync pulse but it would also lead to an unresolved loss of synchronization of an SCC or SMC operating in Transparent or GCI modes (assuming that SCC or SMC was receiving data from the SI).

In revision C.1 and later of the QUICC, the SI will ignore this unexpected sync pulse and synchronize on the next sync pulse (it will not reset itself). This may lead to a reception of one or two “bad” slots but the SCC or SMC will remain synchronized.

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