Data Sheet | May 21, 2008 | FN6337.3

## 4.5MHz, Single Dual and Quad Precision Rail-to-Rail Input-Output (RRIO) Op Amps with Very Low Input Bias Current

The ISL28148, ISL28248 and ISL28448 are 4.5MHz low-power single, dual and quad operational amplifiers. The parts are optimized for single supply operation from 2.4V to 5.5V, allowing operation from one lithium cell or two Ni-Cd batteries.

The single, dual and quad feature an Input Range Enhancement Circuit (IREC) which enables them to maintain CMRR performance for input voltages greater than the positive supply. The input signal is capable of swinging 0.25V above the positive supply and to 100mV below the negative supply with only a slight degradation of the CMRR performance. The output operation is rail-to-rail.

The parts draw minimal supply current (900µA per amplifier) while meeting excellent DC accuracy, AC performance, noise and output drive specifications. The ISL28148 features an enable pin that can be used to turn the device off and reduce the supply current to a maximum of 16µA. Operation is guaranteed over -40°C to +125°C temperature range.

## Features

- 4.5MHz gain bandwidth product
- 900µA supply current (per amplifier)
- 1.8mV maximum offset voltage
- 1pA typical input bias current
- Down to 2.4V single supply operation
- Rail-to-rail input and output
- Enable pin (ISL28148 SOT-23 package only)
- -40°C to +125°C operation
- Pb-free (RoHS compliant)

## Applications

- Low-end audio
- 4mA to 20mA current loops
- Medical devices
- Sensor amplifiers
- ADC buffers
- DAC output amplifiers

## Ordering Information

| PART NUMBER | PART MARKING | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|
| ISL28148FHZ-T7* (Note 1) | GABT | 6 Ld SOT-23 (Tape and Reel) | MDP0038 |
| ISL28148FHZ-T7A* (Note 1) | GABT | 6 Ld SOT-23 (Tape and Reel) | MDP0038 |
| ISL28148FIZ-T7 (Note 2) | 178Z | 6 Ld WLCSP (1.5mmx1.0mm) | W3x2.6C |
| ISL28248FBZ (Note 1) | 28248BZ | 8 Ld SOIC | MDP0027 |
| ISL28248FBZ-T7* (Note 1) | 28248BZ | 8 Ld SOIC (Tape and Reel) | MDP0027 |
| ISL28248FUZ (Note 1) | 8248Z | 8 Ld MSOP | MDP0043 |
| ISL28248FUZ-T7* (Note 1) | 8248Z | 8 Ld MSOP (Tape and Reel) | MDP0043 |
| *Coming Soon,* ISL28448FVZ (Note 1) | MXZ | 14 Ld TSSOP | M14.173 |
| *Coming Soon,* ISL28448FVZ-T7* (Note 1) | MXZ | 14 Ld TSSOP (Tape and Reel) | M14.173 |

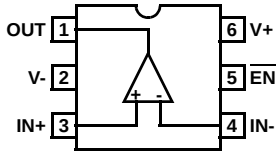
*Please refer to TB347 for details on reel specifications.

NOTES:

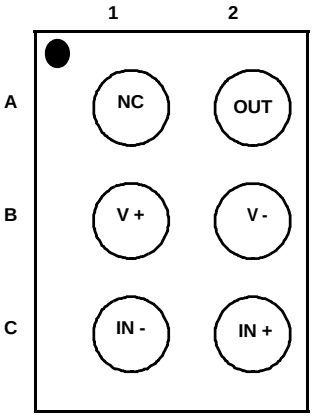
1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free WLCSP and BGA packaged products products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Pinouts

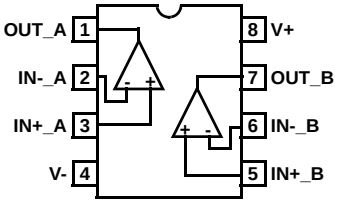
**ISL28148**
**(6 LD SOT-23)**
TOP VIEW



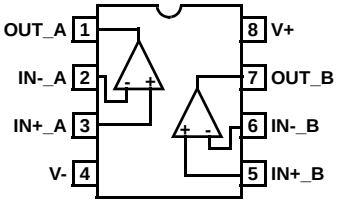

**ISL28148**
**(6 LD WLCSP)**
TOP VIEW



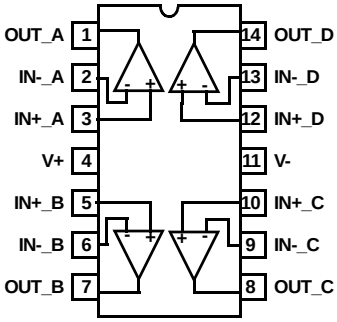

**ISL28248**
**(8 LD SOIC)**
TOP VIEW




**ISL28248**
**(8 LD MSOP)**
TOP VIEW




**ISL28448**
**(14 LD TSSOP)**
TOP VIEW



## Absolute Maximum Ratings ($T_A$ = +25°C)

Supply Voltage . . . . . 5.75V
Supply Turn On Voltage Slew Rate . . . . . 1V/µs
Differential Input Current . . . . . 5mA
Differential Input Voltage . . . . . 0.5V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD Rating
Human Body Model . . . . . .3kV
Machine Model . . . . . .300V
Charged Device Model . . . . . .1200V

## Thermal Information

| Thermal Resistance (Typical, Note 3) | $\theta_{JA}$ (°C/W) |
|---|---|
| 6 Ld SOT-23 Package | 230 |
| 6 Ld WLCSP Package | 130 |
| 8 Ld SO Package | 125 |
| 8 Ld MSOP Package | 175 |
| 14 Ld TSSOP Package | 115 |

Ambient Operating Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTE:

3. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## Electrical Specifications

V+ = 5V, V- = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open, $T_A$ = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 4) | TYP | MAX (Note 4) | UNIT |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | ISL28148 | **-**1.8<br>**-2** | 0 | 1.8<br>**2** | mV |
| | | ISL28148 CSP package | **-**1.0<br>**-1.2** | -0.1 | 1.0<br>**1.2** | |
| | | ISL28248 and ISL28448 | **-**1.8<br>**-2.8** | 0 | 1.8<br>**2.8** | |
| $\frac{\Delta V_{OS}}{\Delta T}$ | Input Offset Voltage vs Temperature | | | 0.03 | | µV/°C |
| $I_{OS}$ | Input Offset Current | $T_A$ = -40°C to +85°C | -35<br>**-80** | ±5 | 35<br>**80** | pA |
| $I_B$ | Input Bias Current | $T_A$ = -40°C to +85°C | -30<br>**-80** | ±1 | 30<br>**80** | pA |
| | | CSP package<br>$T_A$ = -40°C to +85°C | -40<br>**-90** | ±1 | 30<br>**80** | |
| CMIR | Common-Mode Voltage Range | Guaranteed by CMRR | **0** | | **5** | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = 0V to 5V | 75<br>**70** | 98 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_+$ = 2.4V to 5.5V | 80<br>**75** | 98 | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = 0.5V to 4.5V, $R_L$ = 100kΩ to $V_{CM}$ | 200<br>**150** | 580 | | V/mV |
| | | $V_O$ = 0.5V to 4.5V, $R_L$ = 1kΩ to $V_{CM}$ | | 50 | | V/mV |
| $V_{OUT}$ | Maximum Output Voltage Swing | Output low, $R_L$ = 100kΩ to $V_{CM}$ | | 3 | 6<br>**8** | mV |
| | | Output low, $R_L$ = 1kΩ to $V_{CM}$ | | 50 | 70<br>**110** | mV |
| | | Output high, $R_L$ = 100kΩ to $V_{CM}$ | 4.994<br>**4.99** | 4.998 | | V |
| | | Output high, $R_L$ = 1kΩ to $V_{CM}$ | 4.93<br>**4.89** | 4.95 | | V |
| $I_{S,ON}$ | Quiescent Supply Current, Enabled | Per Amplifier | | 0.9 | 1.25<br>**1.4** | mA |

**Electrical Specifications** $V+ = 5V$, $V- = 0V$, $V_{CM} = 2.5V$, $R_L$ = Open, $T_A = +25°C$ unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 4) | TYP | MAX (Note 4) | UNIT |
|---|---|---|---|---|---|---|
| $I_{S,OFF}$ | Quiescent Supply Current, Disabled | ISL28148 SOT-23 package only | | 10 | 14<br>**16** | µA |
| $I_O+$ | Short-Circuit Output Source Current | $R_L = 10\Omega$ to $V_{CM}$ | 48<br>**45** | 75 | | mA |
| $I_O-$ | Short-Circuit Output Sink Current | $R_L = 10\Omega$ to $V_{CM}$ | | -68 | -48<br>**-45** | mA |
| $V_{SUPPLY}$ | Supply Operating Range | V+ to V- | **2.4** | | **5.5** | V |
| $V_{ENH}$ | $\overline{EN}$ Pin High Level | ISL28148 SOT-23 package only | **2** | | | V |
| $V_{ENL}$ | $\overline{EN}$ Pin Low Level | ISL28148 SOT-23 package only | | | **0.8** | V |
| $I_{ENH}$ | $\overline{EN}$ Pin Input High Current | $V_{\overline{EN}} = V+$, ISL28148 SOT-23 package only | | 1 | 1.5<br>**1.6** | µA |
| $I_{ENL}$ | $\overline{EN}$ Pin Input Low Current | $V_{\overline{EN}} = V-$, ISL28148 SOT-23 package only | | 12 | 25<br>**30** | nA |
| **AC SPECIFICATIONS** | | | | | | |
| GBW | Gain Bandwidth Product | $A_V = 100$, $R_F = 100k\Omega$, $R_G = 1k\Omega$, $R_L = 10k\Omega$ to $V_{CM}$ | | 4.5 | | MHz |
| Unity Gain Bandwidth | -3dB Bandwidth | $A_V = 1$, $R_F = 0\Omega$, $V_{OUT} = 10mV_{P-P}$, $R_L = 10k\Omega$ to $V_{CM}$ | | 13 | | MHz |
| $e_N$ | Input Noise Voltage Peak-to-Peak | f = 0.1Hz to 10Hz | | 2 | | $\mu V_{PP}$ |
| | Input Noise Voltage Density | $f_O$ = 1kHz | | 28 | | $nV/\sqrt{Hz}$ |
| $i_N$ | Input Noise Current Density | $f_O$ = 1kHz | | 0.016 | | $pA/\sqrt{Hz}$ |
| CMRR @ 60Hz | Input Common Mode Rejection Ratio | $V_{CM} = 1V_{P-P}$, $R_L = 10k\Omega$ to $V_{CM}$ | | 85 | | dB |
| PSRR- @ 120Hz | Power Supply Rejection Ratio ($V_-$) | $V_+$, $V_-$ = ±1.2V and ±2.5V, $V_{SOURCE} = 1V_{P-P}$, $R_L = 10k\Omega$ to $V_{CM}$ | | -82 | | dB |
| PSRR+ @ 120Hz | Power Supply Rejection Ratio ($V_+$) | $V_+$, $V_-$ = ±1.2V and ±2.5V $V_{SOURCE} = 1V_{P-P}$, $R_L = 10k\Omega$ to $V_{CM}$ | | -100 | | dB |
| **TRANSIENT RESPONSE** | | | | | | |
| SR | Slew Rate | | | ±4 | | V/µs |
| $t_r$, $t_f$, Large Signal | Rise Time, 10% to 90%, $V_{OUT}$ | $A_V = +2$, $V_{OUT} = 3V_{P-P}$, $R_G = R_F = 10k\Omega$ $R_L = 10k\Omega$ to $V_{CM}$ | | 530 | | ns |
| | Fall Time, 90% to 10%, $V_{OUT}$ | $A_V = +2$, $V_{OUT} = 3V_{P-P}$, $R_G = R_F = 10k\Omega$ $R_L = 10k\Omega$ to $V_{CM}$ | | 530 | | ns |
| $t_r$, $t_f$, Small Signal | Rise Time, 10% to 90%, $V_{OUT}$ | $A_V = +2$, $V_{OUT} = 10mV_{P-P}$, $R_G = R_F = R_L = 10k\Omega$ to $V_{CM}$ | | 50 | | ns |
| | Fall Time, 90% to 10%, $V_{OUT}$ | $A_V = +2$, $V_{OUT} = 10mV_{P-P}$, $R_G = R_F = R_L = 10k\Omega$ to $V_{CM}$ | | 50 | | ns |
| $t_{\overline{EN}}$ | Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% $V_{OUT}$, (ISL28148) | $\overline{EN}$ = 5V to 0V, $A_V = +2$, $R_G = R_F = R_L = 1k$ to $V_{CM}$ | | 5 | | µs |
| | Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% $V_{OUT}$, (ISL28148) | $V_{\overline{EN}}$ = 0V to 5V, $A_V = +2$, $R_G = R_F = R_L = 1k$ to $V_{CM}$ | | 0.2 | | µs |

NOTE:

4. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

## Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open$

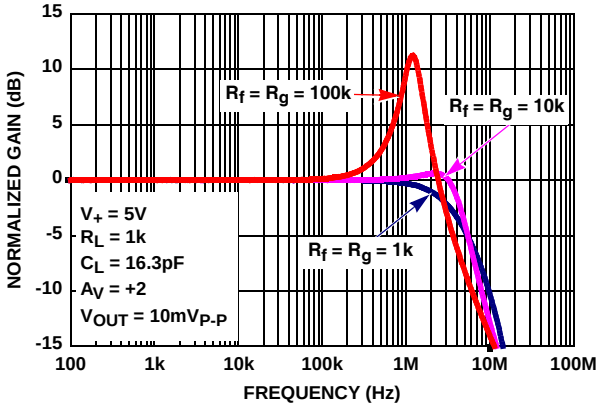



FIGURE 1. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES $R_f/R_g$

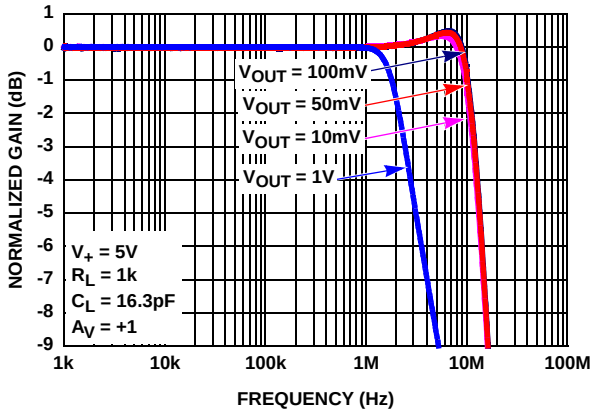



FIGURE 2. GAIN vs FREQUENCY vs $V_{OUT}$, $R_L$ = 1k

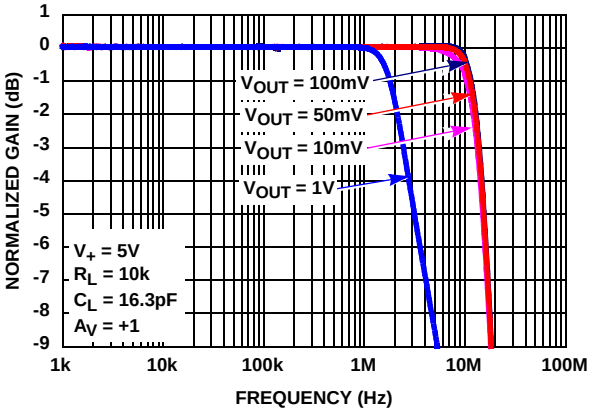



FIGURE 3. GAIN vs FREQUENCY vs $V_{OUT}$, $R_L$ = 10k

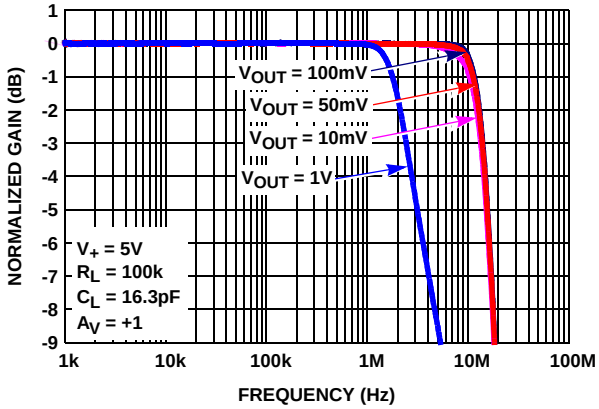



FIGURE 4. GAIN vs FREQUENCY vs $V_{OUT}$, $R_L$ = 100k

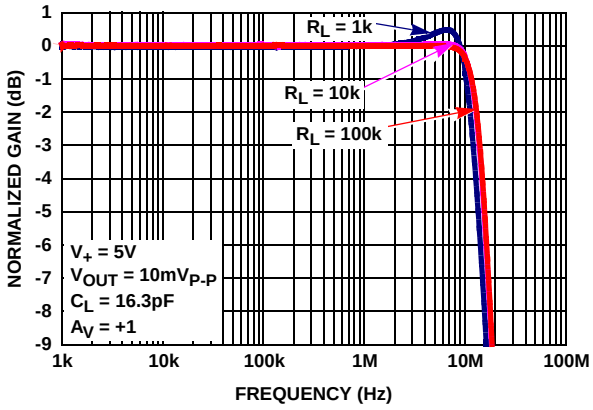



FIGURE 5. GAIN vs FREQUENCY vs $R_L$

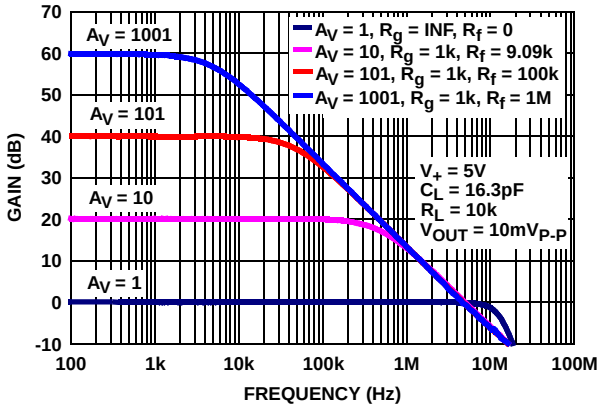



FIGURE 6. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

## Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

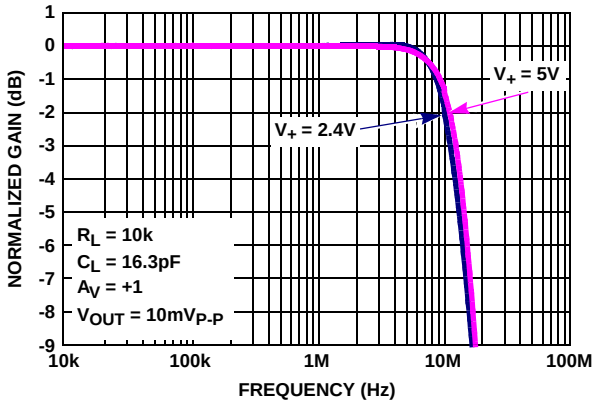



FIGURE 7. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

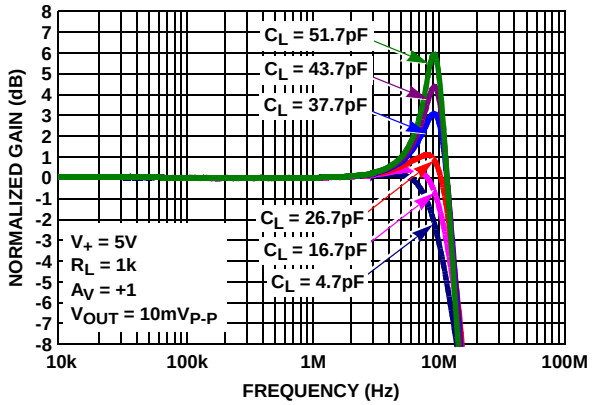



FIGURE 8. GAIN vs FREQUENCY vs $C_L$

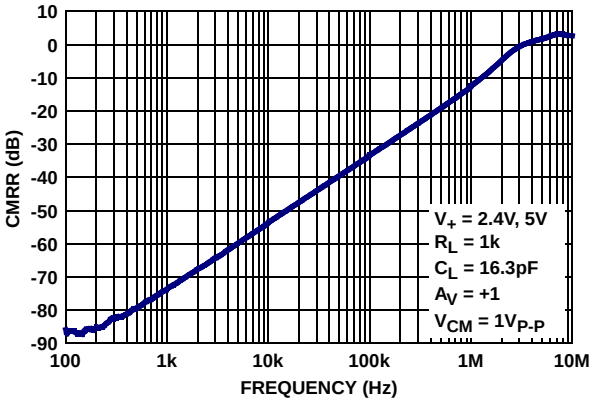



FIGURE 9. CMRR vs FREQUENCY; $V_+$ = 2.4V AND 5V

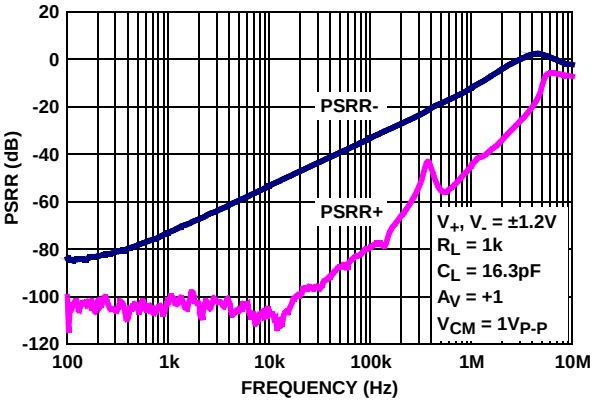



FIGURE 10. PSRR vs FREQUENCY, $V_+$, $V_-$ = ±1.2V

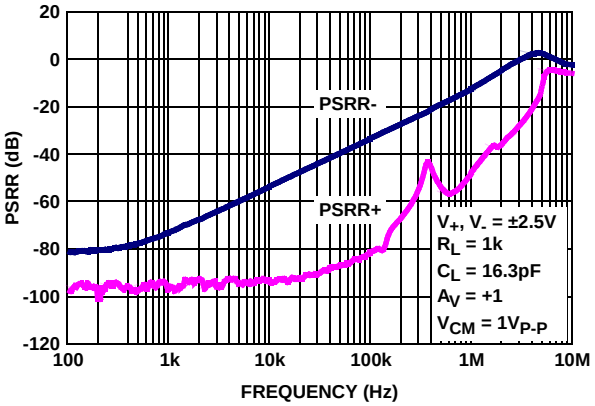



FIGURE 11. PSRR vs FREQUENCY $V_+$, $V_-$ = ±2.5V

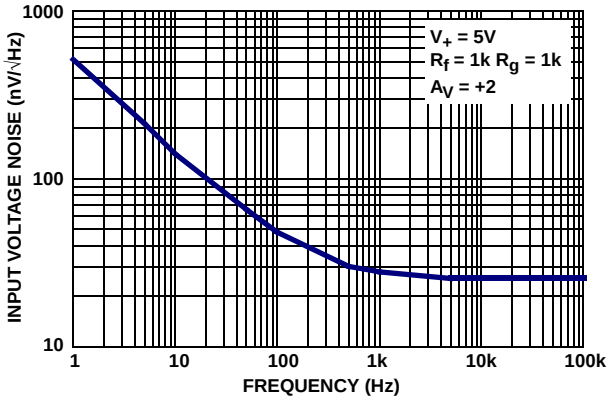



FIGURE 12. INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

## Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

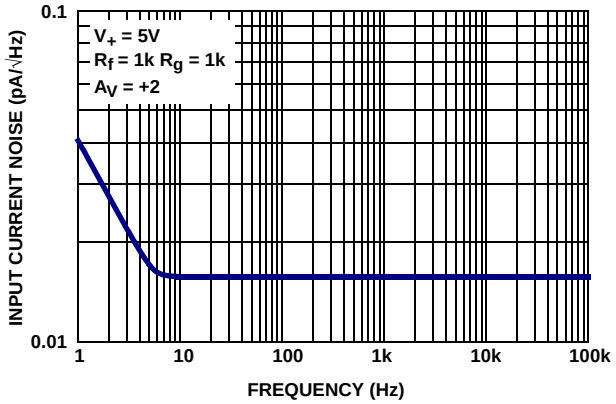



FIGURE 13. INPUT CURRENT NOISE DENSITY vs FREQUENCY

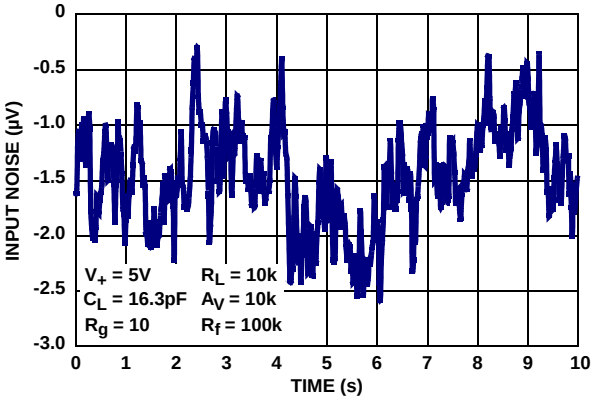



FIGURE 14. INPUT VOLTAGE NOISE 0.1Hz TO 10Hz

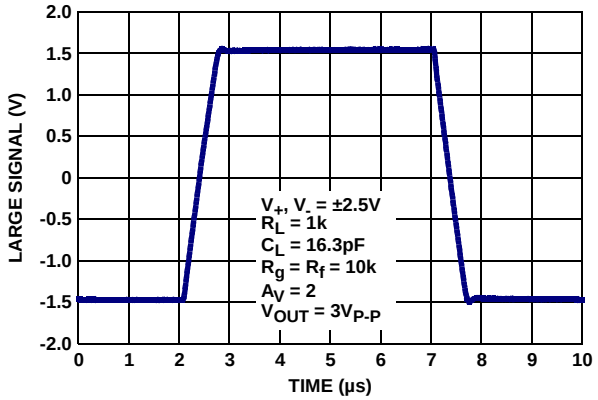



FIGURE 15. LARGE SIGNAL STEP RESPONSE

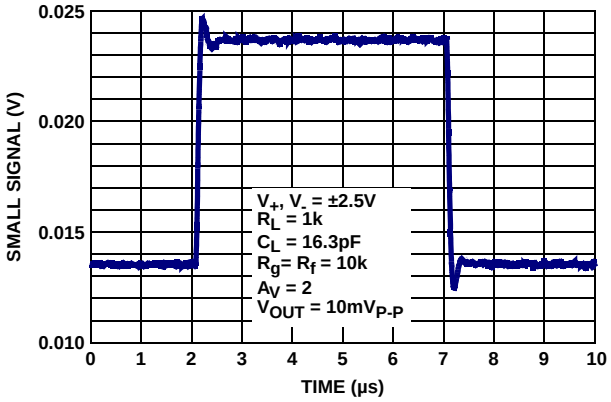



FIGURE 16. SMALL SIGNAL STEP RESPONSE

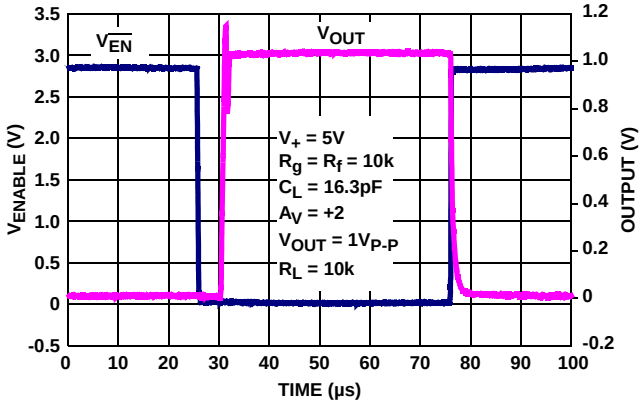



FIGURE 17. ISL28148 ENABLE TO OUTPUT RESPONSE

## Typical Performance Curves V+ = 5V, V- = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open (Continued)

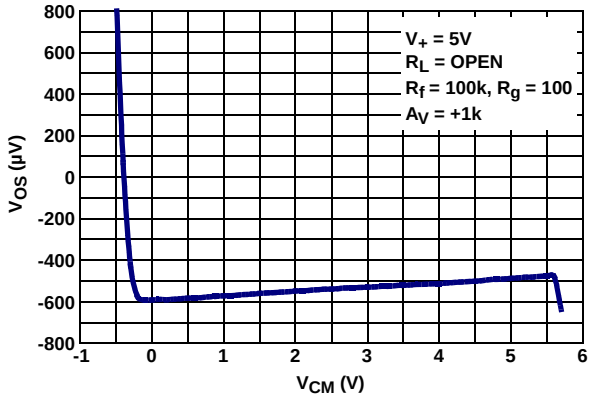



FIGURE 18. INPUT OFFSET VOLTAGE vs COMMON MODE INPUT VOLTAGE

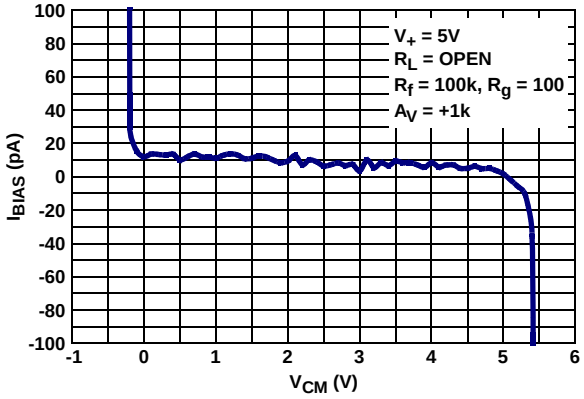



FIGURE 19. INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE

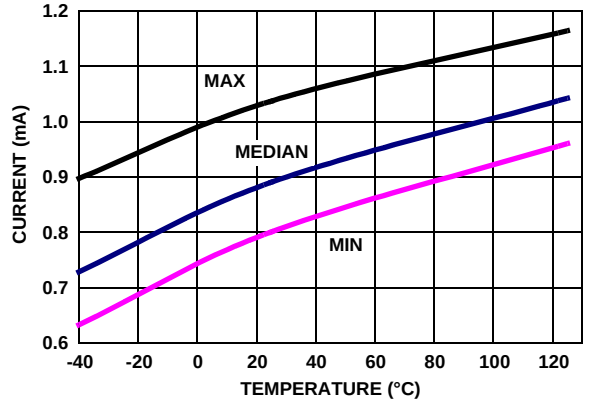



FIGURE 20. SUPPLY CURRENT ENABLED vs TEMPERATURE $V_+$, $V_-$ = ±2.5V

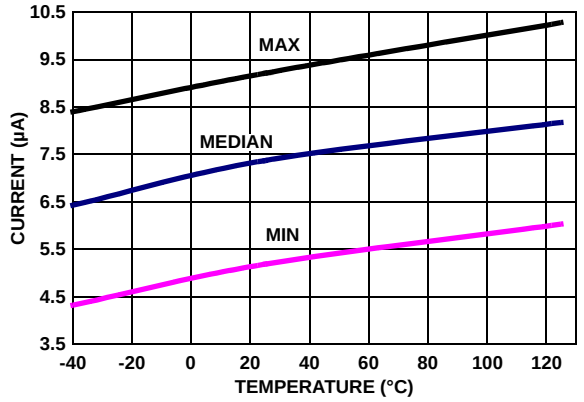



FIGURE 21. SUPPLY CURRENT DISABLED vs TEMPERATURE $V_+$, $V_-$ = ±2.5V

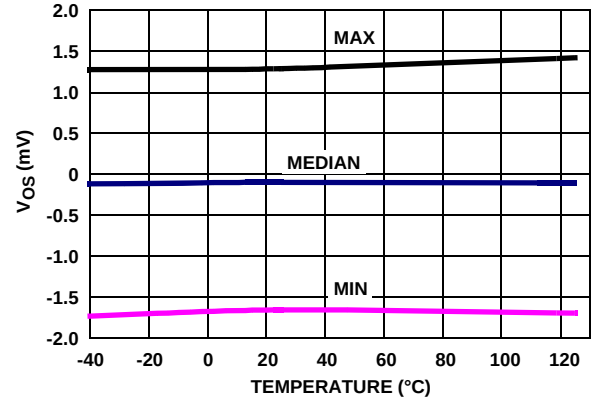



FIGURE 22. $V_{OS}$ vs TEMPERATURE $V_{IN}$ = 0V, $V_+$, $V_-$ = ±2.75V

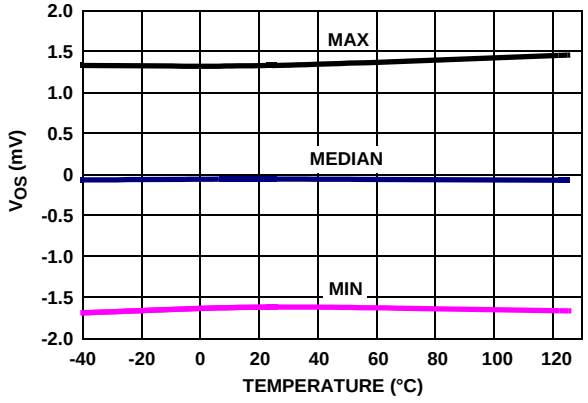



FIGURE 23. $V_{OS}$ vs TEMPERATURE $V_{IN}$ = 0V, $V_+$, $V_-$ = ±2.5V

## Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

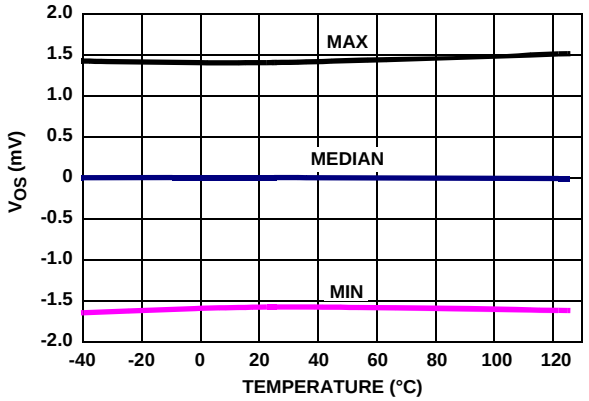



FIGURE 24. $V_{OS}$ vs TEMPERATURE $V_{IN}$ = 0V, $V_+$, $V_-$ = ±1.2V

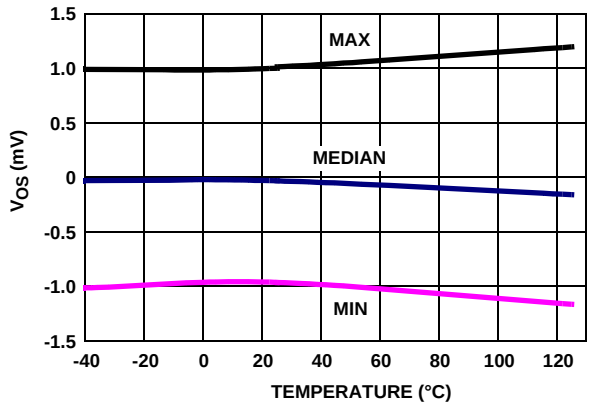



FIGURE 25. CSP PACKAGE $V_{OS}$ vs TEMPERATURE $V_{IN}$ = 0V, $V_+$, $V_-$ = ±2.75V

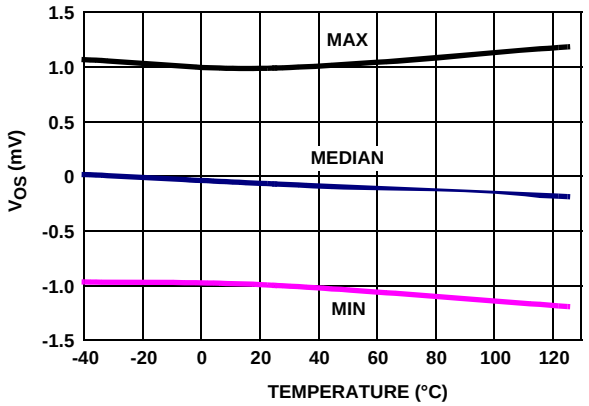



FIGURE 26. CSP PACKAGE $V_{OS}$ vs TEMPERATURE $V_{IN}$ = 0V, $V_+$, $V_-$ = ±2.5V

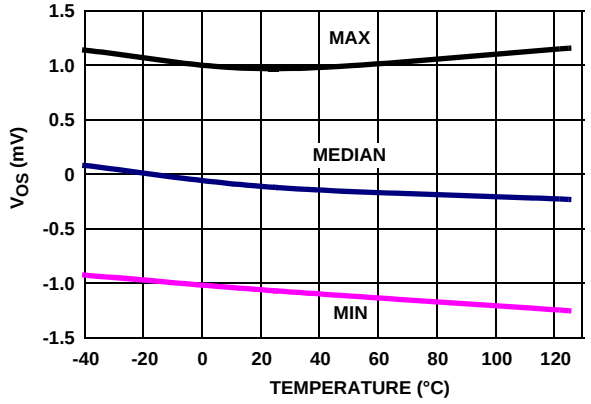



FIGURE 27. CSP PACKAGE $V_{OS}$ vs TEMPERATURE $V_{IN}$ = 0V, $V_+$, $V_-$ = ±1.2V

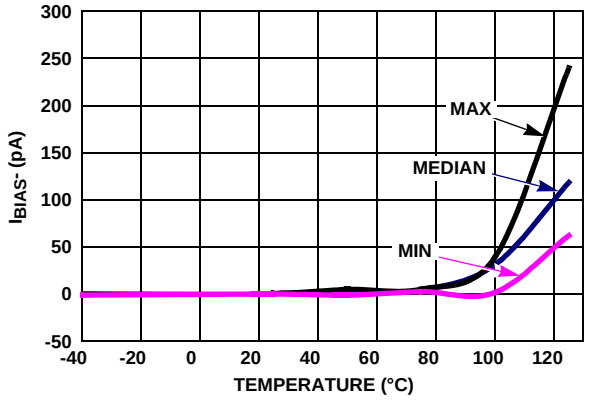



FIGURE 28. $I_{BIAS-}$ vs TEMPERATURE $V_+$, $V_-$ = ±2.5V

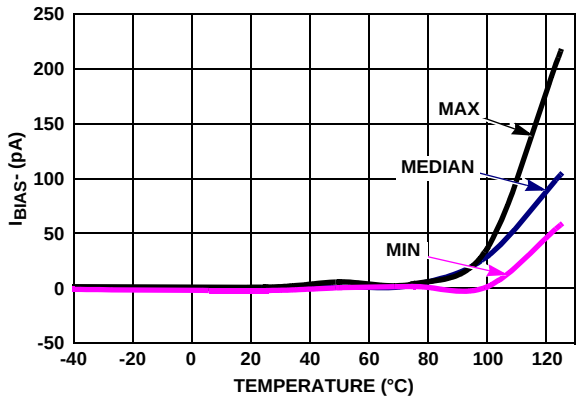



FIGURE 29. $I_{BIAS-}$ vs TEMPERATURE $V_+$, $V_-$ = ±1.2V

## Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

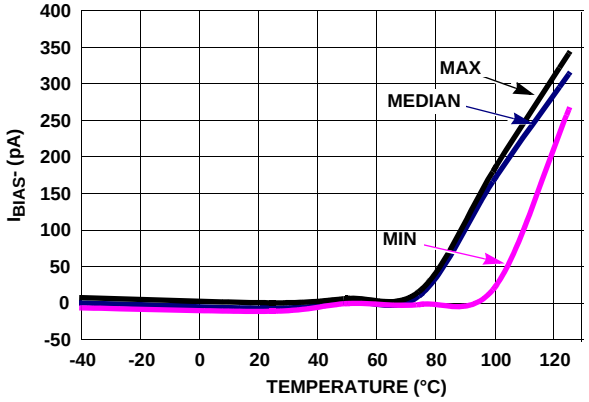



FIGURE 30. CSP PACKAGE $I_{BIAS-}$ vs TEMPERATURE $V_+, V_- = \pm 2.5V$

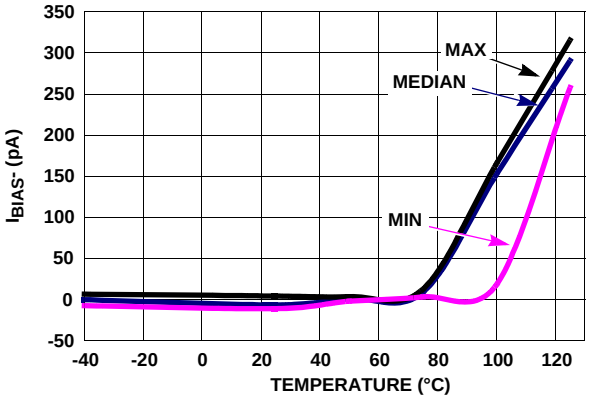



FIGURE 31. CSP PACKAGE $I_{BIAS-}$ vs TEMPERATURE $V_+, V_- = \pm 1.2V$

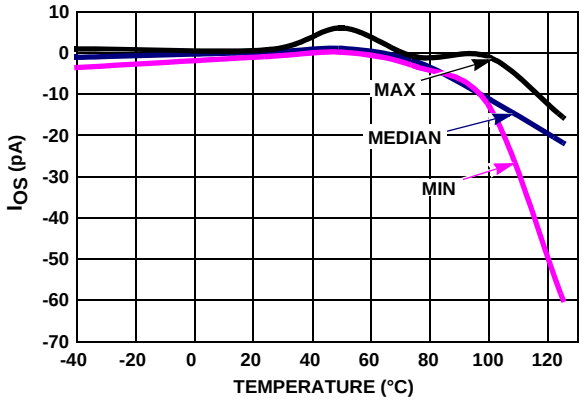



FIGURE 32. $I_{OS}$ vs TEMPERATURE $V_+, V_- = \pm 2.5V$

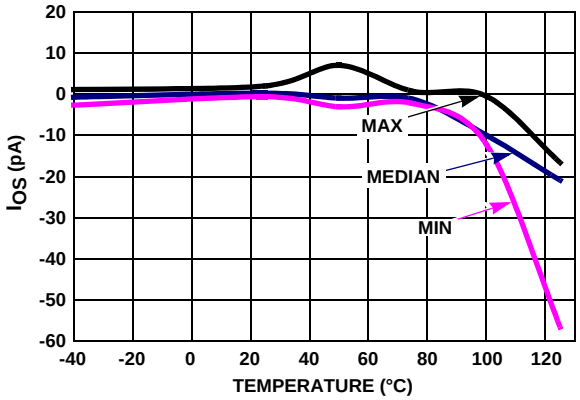



FIGURE 33. $I_{OS}$ vs TEMPERATURE $V_+, V_- = \pm 1.2V$

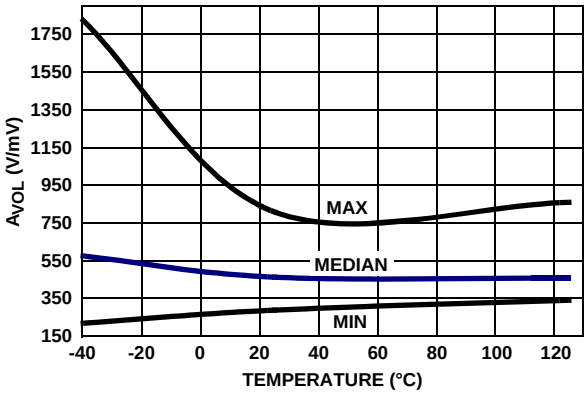



FIGURE 34. $A_{VOL}$ vs TEMPERATURE $R_L = 100k, V_+, V_- = \pm 2.5V, V_O$ = -2V TO +2V

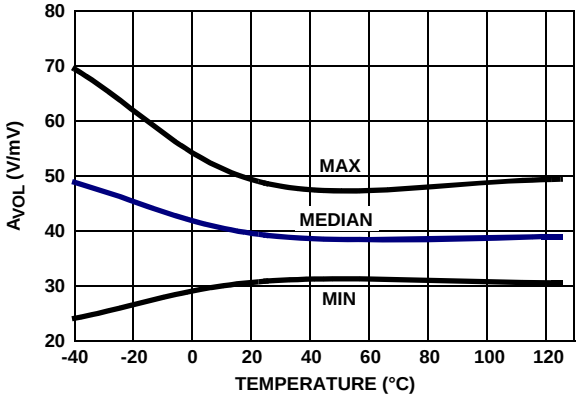



FIGURE 35. $A_{VOL}$ vs TEMPERATURE $R_L = 1k, V_+, V_- = \pm 2.5V, V_O$ = -2V TO +2V

## Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

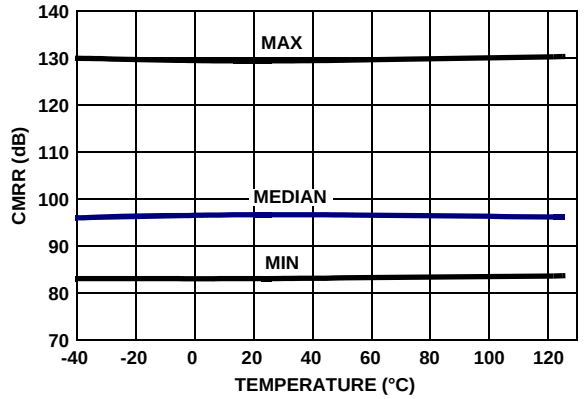



FIGURE 36. CMRR vs TEMPERATURE $V_{CM}$ = -2.5V TO +2.5V, $V_+$, $V_-$ = ±2.5V

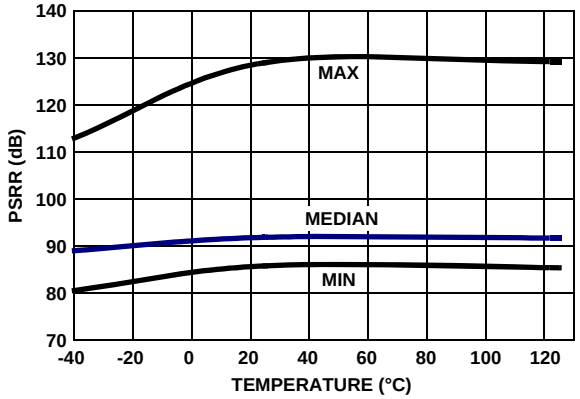



FIGURE 37. PSRR vs TEMPERATURE $V_+$, $V_-$ = ±1.2V TO ±2.75V

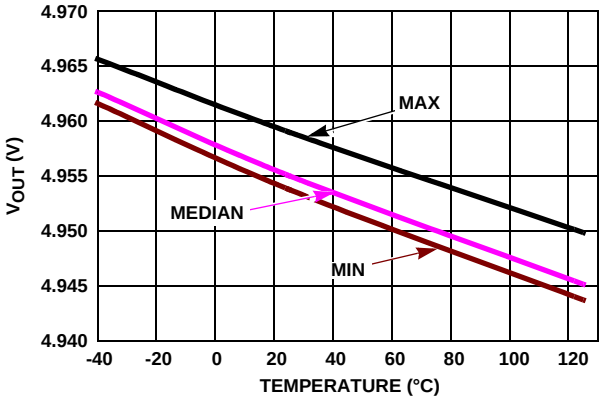



FIGURE 38. $V_{OUT}$ HIGH vs TEMPERATURE $R_L$ = 1k, $V_+$, $V_-$ = ±2.5V

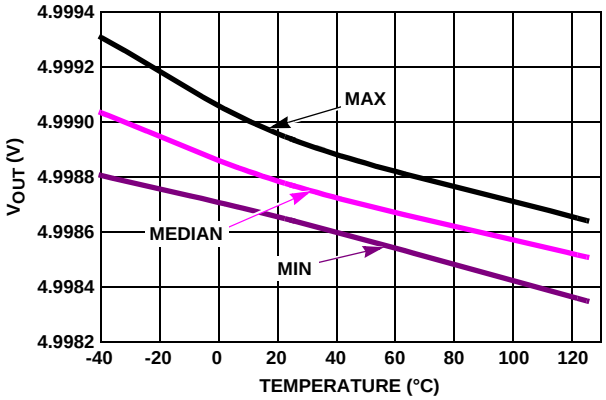



FIGURE 39. $V_{OUT}$ HIGH vs TEMPERATURE $R_L$ = 100k, $V_+$, $V_-$ = ±2.5V

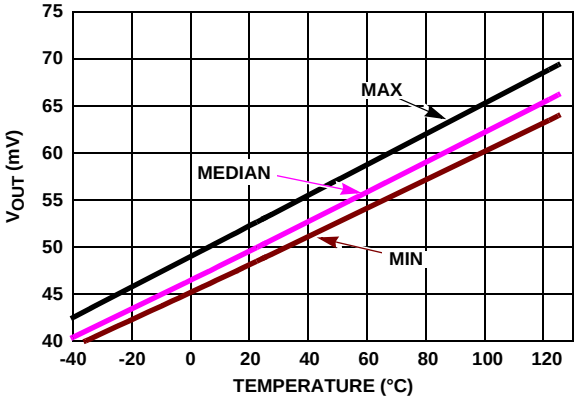



FIGURE 40. $V_{OUT}$ LOW vs TEMPERATURE $R_L$ = 1k, $V_+$, $V_-$ = ±2.5V

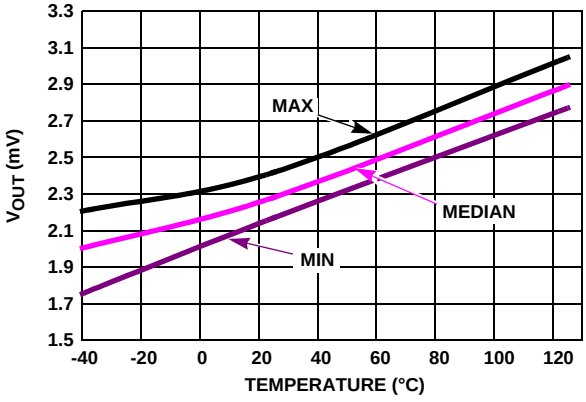



FIGURE 41. $V_{OUT}$ LOW vs TEMPERATURE $R_L$ = 100k, $V_+$, $V_-$ = ±2.5V

## Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

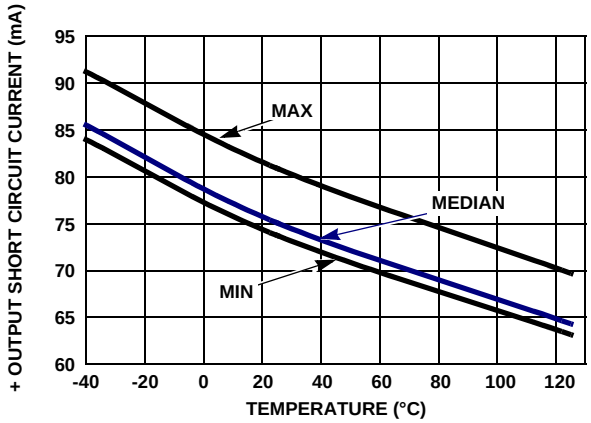



**FIGURE 42. + OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE $V_{IN}$ = 2.55V, $R_L$ = 10, $V_+$, $V_-$ = ±2.5V**

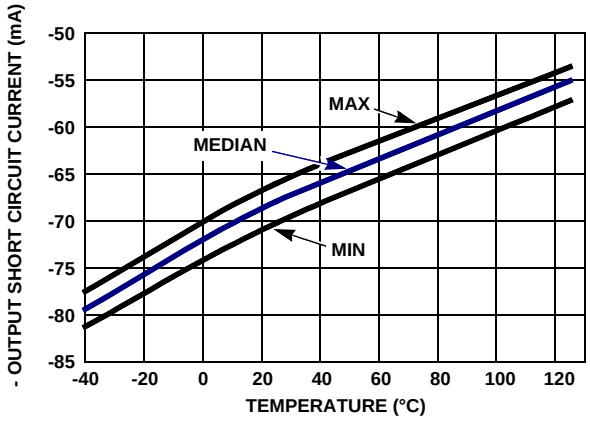
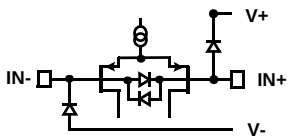
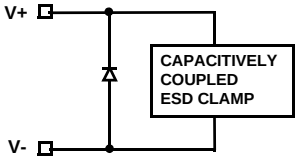
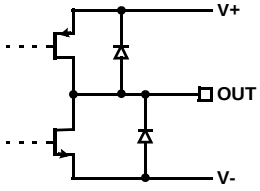
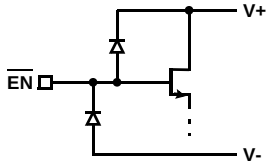



**FIGURE 43. - OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE $V_{IN}$ = -2.55V, $R_L$ = 10, $V_+$, $V_-$ = ±2.5V**

## Pin Descriptions

| ISL28148 (6 Ld SOT-23) | ISL28148 6 Ld WLCSP | ISL28248 (8 Ld SO) (8 Ld MSOP) | ISL28448 (14 Ld TSSOP) | PIN NAME | FUNCTION | EQUIVALENT CIRCUIT |
|---|---|---|---|---|---|---|
| | | | | NC | Not connected | |
| 4 | C1 | 2 (A)<br>6 (B) | 2 (A)<br>6 (B)<br>9 (C)<br>13 (D) | IN-<br>IN-_A<br>IN-_B<br>IN-_C<br>IN-_D | inverting input |  Circuit 1 |
| 3 | C2 | 3 (A)<br>5 (B) | 3 (A)<br>5 (B)<br>10 (C)<br>12 (D) | IN+<br>IN+_A<br>IN+_B<br>IN+_C<br>IN+_D | Non-inverting input | (See circuit 1) |
| 2 | B2 | 4 | 11 | V- | Negative supply |  Circuit 2 |
| 1 | A2 | 1 (A)<br>7 (B) | 1 (A)<br>7 (B)<br>8 (C)<br>14 (D) | OUT<br>OUT_A<br>OUT_B<br>OUT_C<br>OUT_D | Output |  Circuit 3 |
| 6 | B1 | 8 | 4 | V+ | Positive supply | (See circuit 2) |

## Pin Descriptions (Continued)

| ISL28148 (6 Ld SOT-23) | ISL28148 6 Ld WLCSP | ISL28248 (8 Ld SO) (8 Ld MSOP) | ISL28448 (14 Ld TSSOP) | PIN NAME | FUNCTION | EQUIVALENT CIRCUIT |
|---|---|---|---|---|---|---|
| 5 | | | - | $\overline{EN}$ | Chip enable |  Circuit 4 |
| | A1 | | | NC | Connect pin to the most Negative Supply | |

## Applications Information

### Introduction

The ISL28148, ISL28248 and ISL28448 are single, dual and quad channel CMOS rail-to-rail input, output (RRIO) micropower precision operational amplifiers. The parts are designed to operate from single supply (2.4V to 5.5V) or dual supply (±1.2V to ±2.75V). The parts have an input common mode range that extends 0.25V above the positive rail and 100mV below the negative supply rail. The output can swing within about 3mV of the supply rails with a 100kΩ load.

### Rail-to-Rail Input

Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The parts achieve input rail-to-rail operation without sacrificing important precision specifications and degrading distortion performance. The devices' input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current vs the common-mode voltage range gives us an undistorted behavior from typically 100mV below the negative rail and 0.25V higher than the V+ rail.

### Rail-to-Rail Output

A pair of complementary MOS devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The devices' with a 100kΩ load will swing to within 3mV of the positive supply rail and within 3mV of the negative supply rail.

### Results of Over-Driving the Output

Caution should be used when over-driving the output for long periods of time. Over-driving the output can occur in two ways:

1. The input voltage times the gain of the amplifier exceeds the supply voltage by a large value or
2. The output current required is higher than the output stage can deliver. These conditions can result in a shift in the Input Offset Voltage ($V_{OS}$) as much as 1µV/hr. of exposure under these condition.

### IN+ and IN- Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. They also contain back-to-back diodes across the input terminals ("Pin Descriptions" table - Circuit 1 on page 12). For applications where the input differential voltage is expected to exceed 0.5V, an external series resistor must be used to ensure the input currents never exceed 5mA (Figure 44).

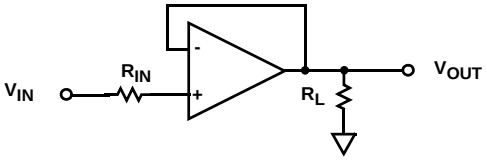



**FIGURE 44. INPUT CURRENT LIMITING**

### Enable/Disable Feature

The ISL28148 offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 10µA at room temperature. By disabling the part, multiple ISL28148 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together. Note that feed through from the IN+ to IN- pins occurs on any Mux Amp disabled channel where the input differential voltage exceeds 0.5V (e.g., active channel $V_{OUT}$ = 1V, while disabled channel $V_{IN}$ = GND), so the mux

implementation is best suited for small signal applications. If large signals are required, use series IN+ resistors, or large value $R_F$, to keep the feed through current low enough to minimize the impact on the active channel. See “Limitations of the Differential Input Protection” on page 14 for more details.The $\overline{EN}$ pin also has an internal pull-down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default. When not used, the $\overline{EN}$ pin should either be left floating or connected directly to the V- pin.

### Limitations of the Differential Input Protection

If the input differential voltage is expected to exceed 0.5V, an external current limiting resistor must be used to ensure the input current never exceeds 5mA. For non-inverting unity gain applications the current limiting can be via a series IN+ resistor, or via a feedback resistor of appropriate value. For other gain configurations, the series IN+ resistor is the best choice, unless the feedback ($R_F$) and gain setting ($R_G$) resistors are both sufficiently large to limit the input current to 5mA.

Large differential input voltages can arise from several sources:

- During open loop (comparator) operation. Used this way, the IN+ and IN- voltages don’t track, so differentials arise.
- When the amplifier is disabled but an input signal is still present. An $R_L$ or $R_G$ to GND keeps the IN- at GND, while the varying IN+ signal creates a differential voltage. Mux Amp applications are similar, except that the active channel $V_{OUT}$ determines the voltage on the IN- terminal.
- When the slew rate of the input pulse is considerably faster than the op amp’s slew rate. If the $V_{OUT}$ can’t keep up with the IN+ signal, a differential voltage results, and visible distortion occurs on the input and output signals. To avoid this issue, keep the input slew rate below 4.8V/µs, or use appropriate current limiting resistors.

Large (>2V) differential input voltages can also cause an increase in disabled $I_{CC}$.

### Using Only One Channel

If the application does not use all channels, then the user must configure the unused channel(s) to prevent them from oscillating. The unused channel(s) will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 45).

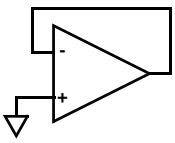



**FIGURE 45. PREVENTING OSCILLATIONS IN UNUSED CHANNELS**

### Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 46 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

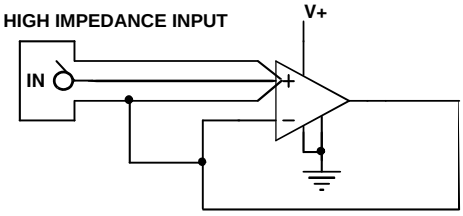



**FIGURE 46. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER**

### Current Limiting

These devices have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

### Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature ($T_{JMAX}$) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

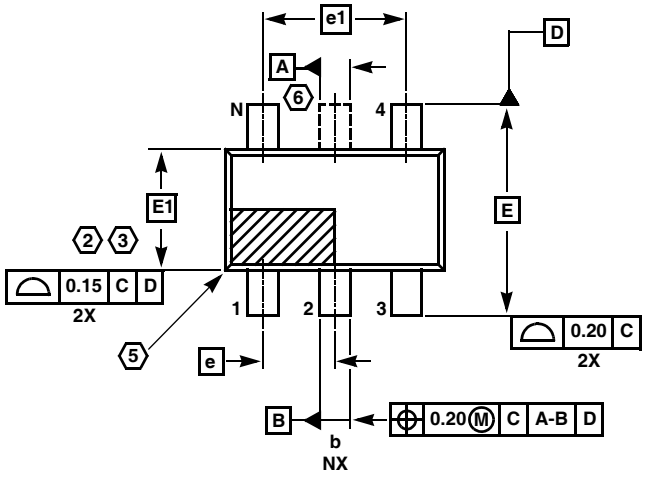
- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package ($PD_{MAX}$)
- $PD_{MAX}$ for each amplifier can be calculated as shown in Equation 2:

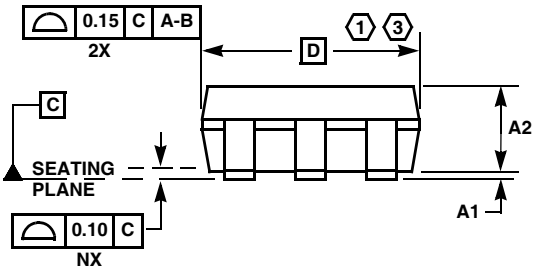
$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

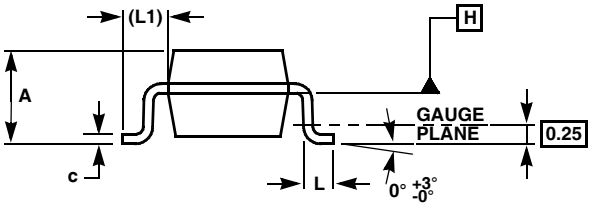
where:

- $T_{MAX}$ = Maximum ambient temperature
- $\theta_{JA}$ = Thermal resistance of the package
- $PD_{MAX}$ = Maximum power dissipation of 1 amplifier
- $V_S$ = Supply voltage (Magnitude of $V_+$ and $V_-$)
- $I_{MAX}$ = Maximum supply current of 1 amplifier
- $V_{OUTMAX}$ = Maximum output voltage swing of the application
- $R_L$ = Load resistance

## SOT-23 Package Family




### MDP0038

**SOT-23 PACKAGE FAMILY**

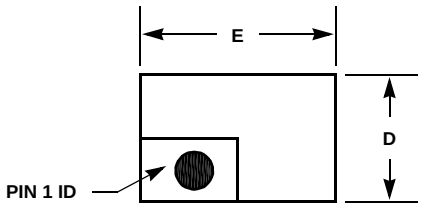
| SYMBOL | MILLIMETERS | | TOLERANCE |
|---|---|---|---|
| | SOT23-5 | SOT23-6 | |
| A | 1.45 | 1.45 | MAX |
| A1 | 0.10 | 0.10 | ±0.05 |
| A2 | 1.14 | 1.14 | ±0.15 |
| b | 0.40 | 0.40 | ±0.05 |
| c | 0.14 | 0.14 | ±0.06 |
| D | 2.90 | 2.90 | Basic |
| E | 2.80 | 2.80 | Basic |
| E1 | 1.60 | 1.60 | Basic |
| e | 0.95 | 0.95 | Basic |
| e1 | 1.90 | 1.90 | Basic |
| L | 0.45 | 0.45 | ±0.10 |
| L1 | 0.60 | 0.60 | Reference |
| N | 5 | 6 | Reference |

Rev. F 2/07

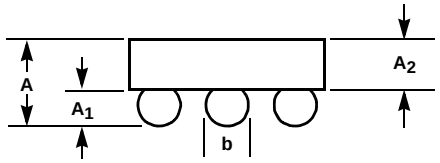
NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

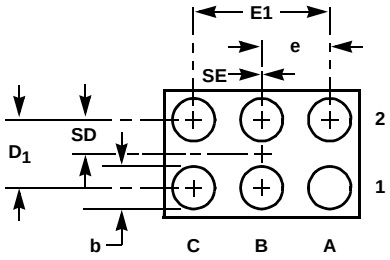
## Wafer Level Chip Scale Package (WLCSP)




TOP VIEW




SIDE VIEW




BOTTOM VIEW

### W3x2.6C

**3x2 ARRAY 6 BALL WAFER LEVEL CHIP SCALE PACKAGE**

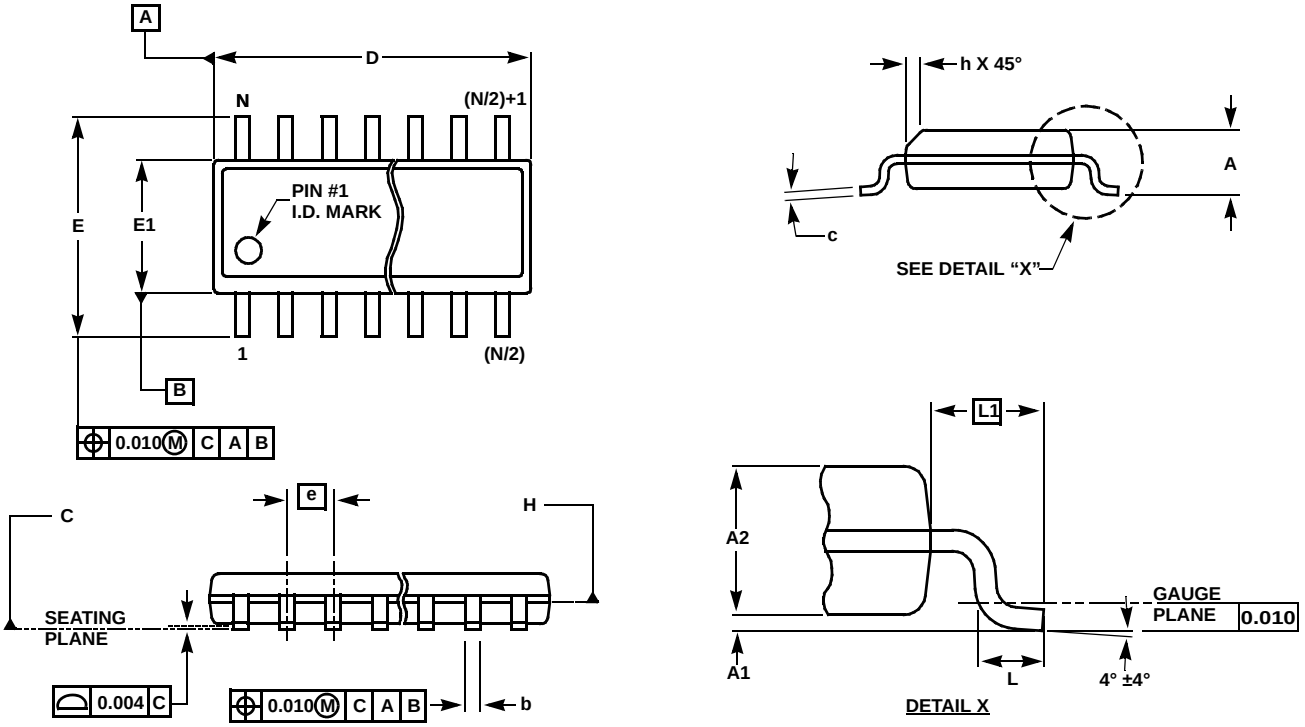
| SYMBOL | MILLIMETERS |
|---|---|
| A | 0.51 Min, 0.55 Max |
| $A_1$ | 0.225 ±0.015 |
| $A_2$ | 0.305 ±0.013 |
| b | Φ0.323 ±0.025 |
| D | 0.955 ±0.020 |
| $D_1$ | 0.50 BASIC |
| E | 1.455 ±0.020 |
| $E_1$ | 1.00 BASIC |
| e | 0.50 BASIC |
| SD | 0.25 BASIC |
| SE | 0.00 BASIC |

Rev. 3 03/08

NOTES:

1. All dimensions are in millimeters.

## Small Outline Package Family (SO)




## MDP0027

**SMALL OUTLINE PACKAGE FAMILY (SO)**

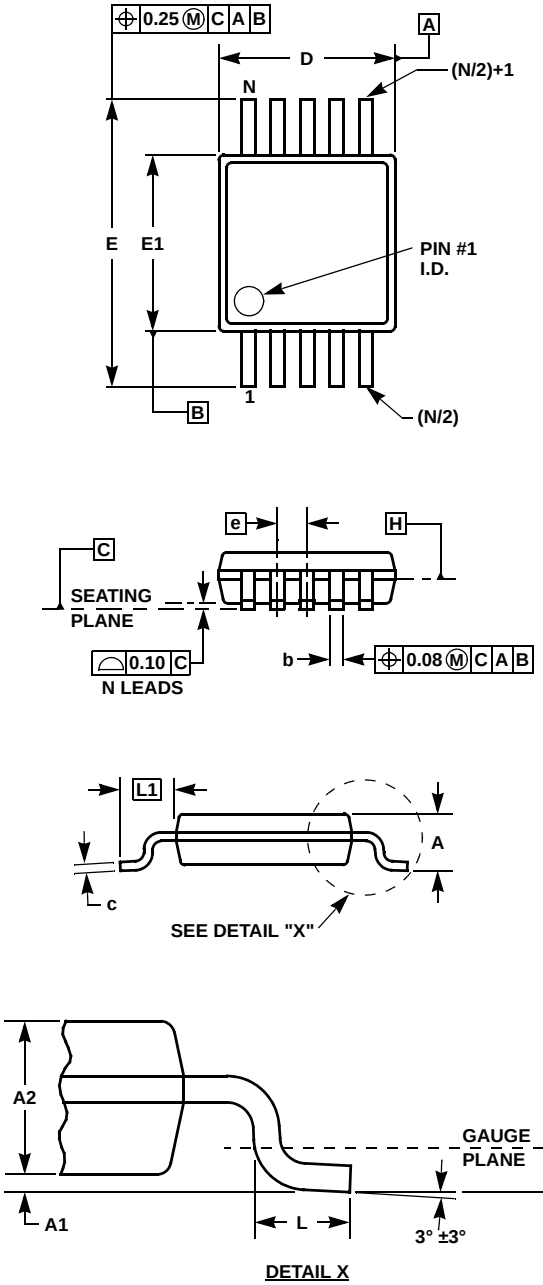
| SYMBOL | INCHES | | | | | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | SO-8 | SO-14 | SO16 (0.150") | SO16 (0.300") (SOL-16) | SO20 (SOL-20) | SO24 (SOL-24) | SO28 (SOL-28) | | |
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | ±0.003 | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | ±0.002 | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | ±0.003 | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | ±0.004 | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

## Mini SO Package Family (MSOP)




### MDP0043

**MINI SO PACKAGE FAMILY**

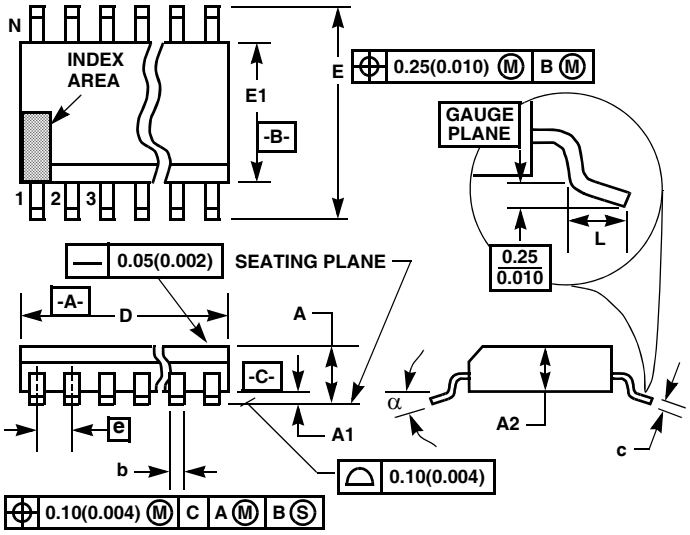
| SYMBOL | MILLIMETERS | | TOLERANCE | NOTES |
|---|---|---|---|---|
| | MSOP8 | MSOP10 | | |
| A | 1.10 | 1.10 | Max. | - |
| A1 | 0.10 | 0.10 | ±0.05 | - |
| A2 | 0.86 | 0.86 | ±0.09 | - |
| b | 0.33 | 0.23 | +0.07/-0.08 | - |
| c | 0.18 | 0.18 | ±0.05 | - |
| D | 3.00 | 3.00 | ±0.10 | 1, 3 |
| E | 4.90 | 4.90 | ±0.15 | - |
| E1 | 3.00 | 3.00 | ±0.10 | 2, 3 |
| e | 0.65 | 0.50 | Basic | - |
| L | 0.55 | 0.55 | ±0.15 | - |
| L1 | 0.95 | 0.95 | Basic | - |
| N | 8 | 10 | Reference | - |

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

## Thin Shrink Small Outline Plastic Packages (TSSOP)




NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

### M14.173

**14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.047 | - | 1.20 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.031 | 0.041 | 0.80 | 1.05 | - |
| b | 0.0075 | 0.0118 | 0.19 | 0.30 | 9 |
| c | 0.0035 | 0.0079 | 0.09 | 0.20 | - |
| D | 0.195 | 0.199 | 4.95 | 5.05 | 3 |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 | 4 |
| e | 0.026 BSC | | 0.65 BSC | | - |
| E | 0.246 | 0.256 | 6.25 | 6.50 | - |
| L | 0.0177 | 0.0295 | 0.45 | 0.75 | 6 |
| N | 14 | | 14 | | 7 |
| α | $0^o$ | $8^o$ | $0^o$ | $8^o$ | - |

Rev. 2 4/06