Data Sheet | October 12, 2005 | FN611.7

Dual High Frequency Differential Amplifier For Low Power Applications Up to 500MHz

The CA3102 consists of two independent differential amplifiers with associated constant current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 1GHz. These features make the CA3102 useful from DC to 500MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3102 provides close electrical and thermal matching of the amplifiers. This feature makes this device particularly useful in dual channel applications where matched performance of the two channels is required.

The CA3102 has a separate substrate connection for greater design flexibility.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. DWG. #
CA3102E (CA3102E)	-55 to 125	14 Ld PDIP	E14.3
CA3102M (3102)	-55 to 125	14 Ld SOIC	M14.15
CA3102MZ (CA3102MZ) (Note)	-55 to 125	14 Ld SOIC (Pb-free)	M14.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

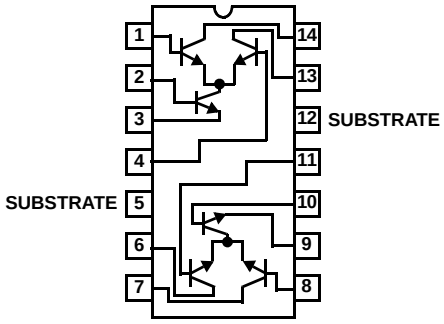
- Power Gain 23dB (Typ) 200MHz
- Noise Figure 4.6dB (Typ) 200MHz
- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Full Military Temperature Range . . . . . -55^oC to 125^oC
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations - RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Balanced Mixers
- Synthesizers
- Balanced (Push-Pull) Cascode Amplifiers
- Sense Amplifiers

Pinout

CA3102
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, I_C 50mA

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	110
SOIC Package	205

Maximum Power Dissipation (Any One Transistor) 300mW
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3102 is isolated from the substrate by an integral diode. The substrate (Terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER							
Input Offset Voltage (Figures 1, 4)	V_{IO}			-	0.25	5.0	mV
Input Offset Current (Figure 1)	I_{IO}	$I_3 = I_9 = 2mA$		-	0.3	3.0	μA
Input Bias Current (Figures 1, 5)	I_B			-	13.5	33	μA
Temperature Coefficient Magnitude of Input Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			-	1.1	-	$\mu V/^oC$
DC CHARACTERISTICS FOR EACH TRANSISTOR							
DC Forward Base-to-Emitter Voltage (Figure 6)	VBE	$V_{CE} = 6V$, $I_C = 1mA$		674	774	874	mV
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 6V$, $I_C = 1mA$		-	-0.9	-	$mV/^oC$
Collector Cutoff Current (Figure 7)	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$		-	0.0013	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$		15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$		20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_B = I_E = 0$		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$		5	7	-	V
DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER							
1/f Noise Figure (For Single Transistor) (Figure 12)	NF	$f = 100kHz$, $R_S = 500\Omega$, $I_C = 1mA$		-	1.5	-	dB
Gain Bandwidth Product (For Single Transistor) (Figure 11)	f_T	$V_{CE} = 6V$, $I_C = 5mA$		-	1.35	-	GHz
Collector-Base Capacitance (Figure 8)	C_{CB}	$I_C = 0$, $V_{CB} = 5V$	Note 3	-	0.28	-	pF
			Note 4	-	0.15	-	pF
Collector-Substrate Capacitance (Figure 8)	C_{CI}	$I_C = 0$, $V_{CI} = 5V$		-	1.65	-	pF
Common Mode Rejection Ratio	CMRR	$I_3 = I_9 = 2mA$		-	100	-	dB
AGC Range, One Stage (Figure 2)	AGC	Bias Voltage = -6V		-	75	-	dB
Voltage Gain, Single-Ended Output (Figures 2, 9, 10)	A	Bias Voltage = -4.2V, f = 10MHz		18	22	-	dB

Electrical Specifications $T_A = 25^oC$ (Continued)

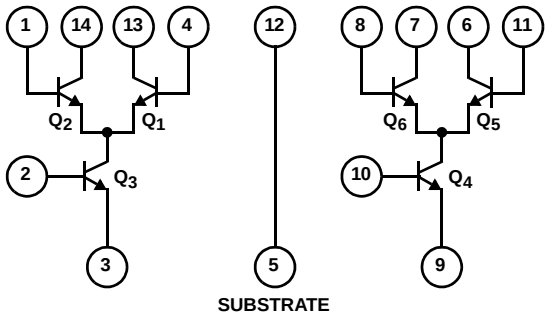
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Insertion Power Gain (Figure 3)	G_P	V_{CC} = 12V, for Cascode Configuration $I_3 = I_9$ = 2mA. For Diff. Amp. Configuration $I_3 = I_9$ = 4mA (Each Collector $I_C \cong$ 2mA) f = 200MHz	Cascode	-	23	-	dB
Noise Figure (Figure 3)	NF		Cascode	-	4.6	-	dB
Input Admittance	Y_{11}		Cascode (Figures 14, 16, 18)	-	1.5 + j2.45	-	mS
			Diff. Amp. (Figures 15, 17, 19)	-	0.878 + j1.3	-	mS
Reverse Transfer Admittance	Y_{12}		Cascode	-	0.0 - j0.008	-	mS
			Diff. Amp.	-	0.0 - j0.013	-	mS
Forward Transfer Admittance	Y_{21}		Cascode (Figures 26, 28, 30)	-	17.9 - j30.7	-	mS
			Diff. Amp. (Figures 27, 29, 31)	-	-10.5 + j13	-	mS
Output Admittance	Y_{22}		Cascode (Figures 20, 22, 24)	-	-0.503 - j15	-	mS
			Diff. Amp. (Figures 21, 23, 25)	-	0.071 + j0.62	-	mS

NOTES:

3. Terminals 1 and 14 or 7 and 8.
4. Terminals 13 and 4 or 6 and 11.

Schematic Diagram

CA3102E, CA3102M



Test Circuits

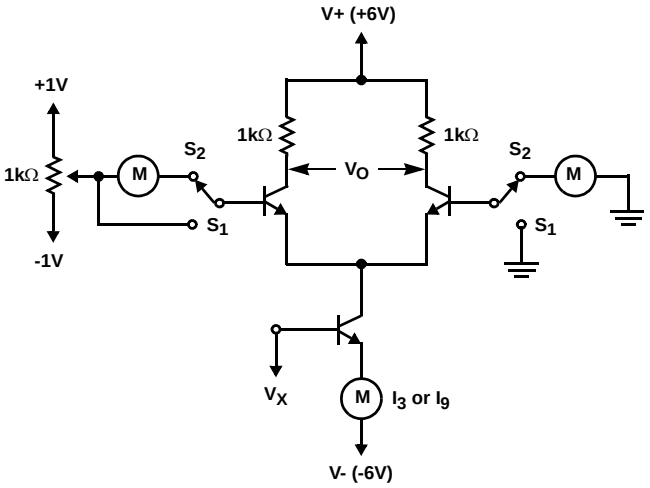


FIGURE 1. DC CHARACTERISTICS TEST CIRCUIT FOR CA3102

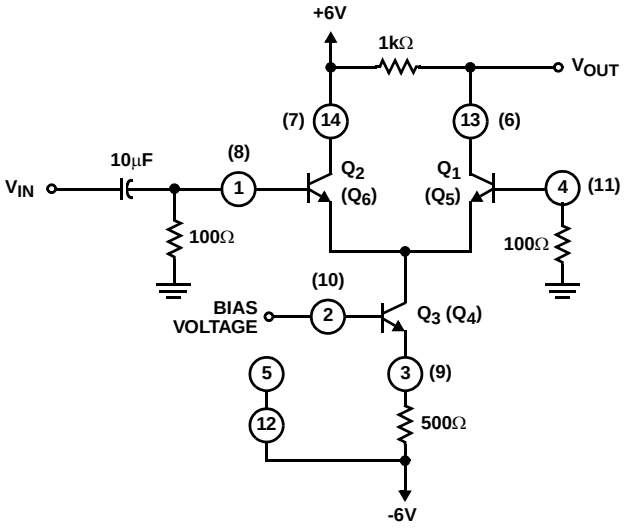
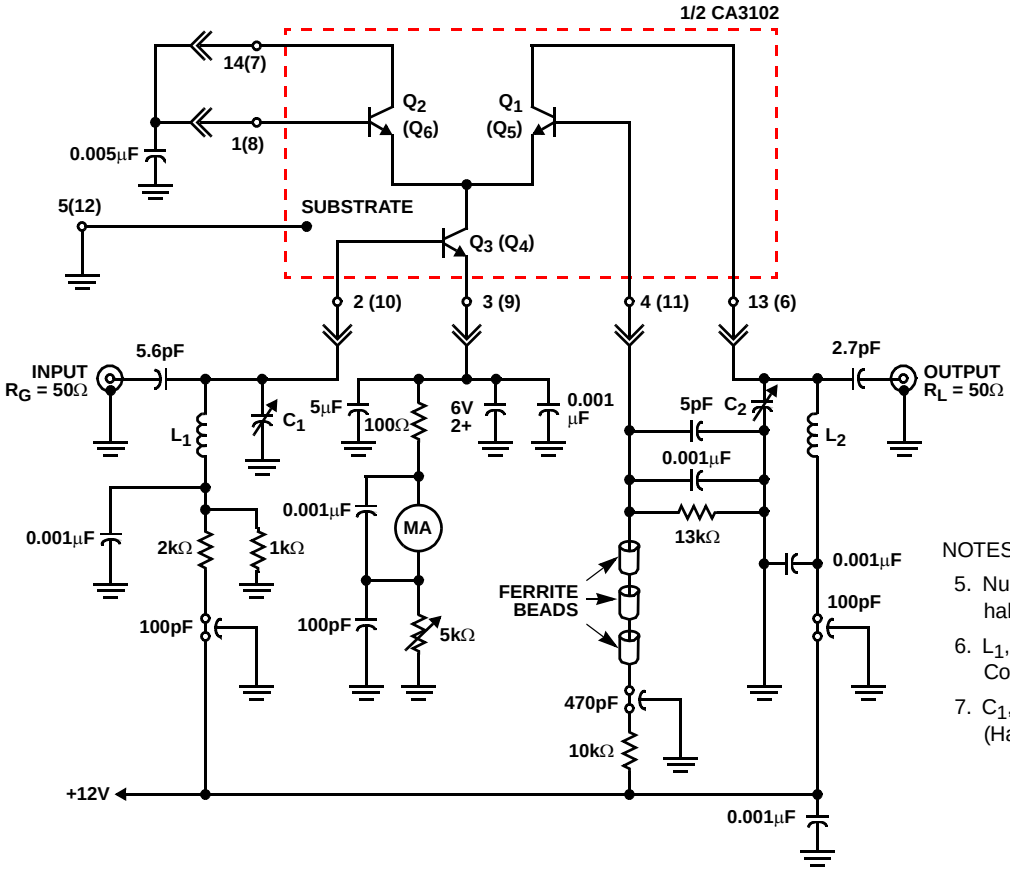


FIGURE 2. AGC RANGE AND VOLTAGE GAIN TEST CIRCUIT FOR CA3102



NOTES:

5. Numbers in parentheses refer to the other half of the CA3102.
6. L_1, L_2 - Approximately $^1/_2$ Turn #18 Tinned Copper Wire, 5/8" Diameter.
7. C_1, C_2 - 15pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent).

FIGURE 3. 200MHz CASCODE POWER GAIN AND NOISE FIGURE TEST CIRCUIT

Typical Performance Curves

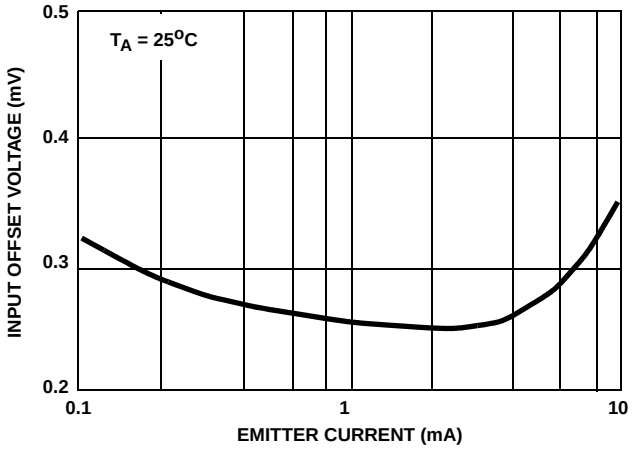


FIGURE 4. INPUT OFFSET VOLTAGE vs EMITTER CURRENT

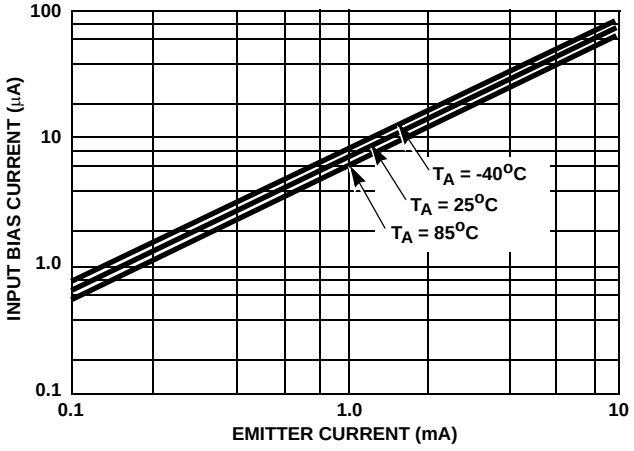


FIGURE 5. INPUT BIAS CURRENT vs EMITTER CURRENT

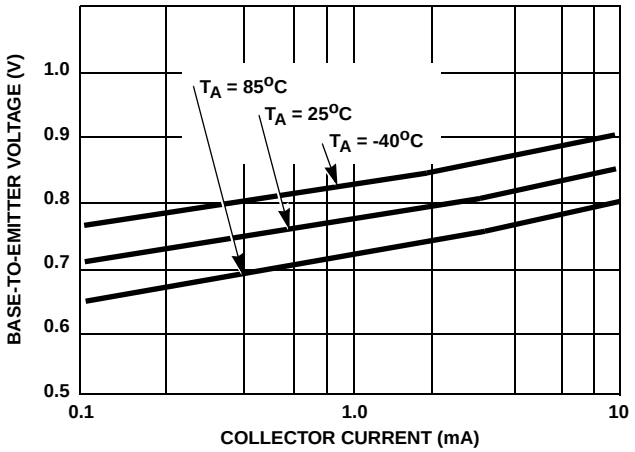


FIGURE 6. BASE-TO-EMITTER VOLTAGE vs COLLECTOR CURRENT

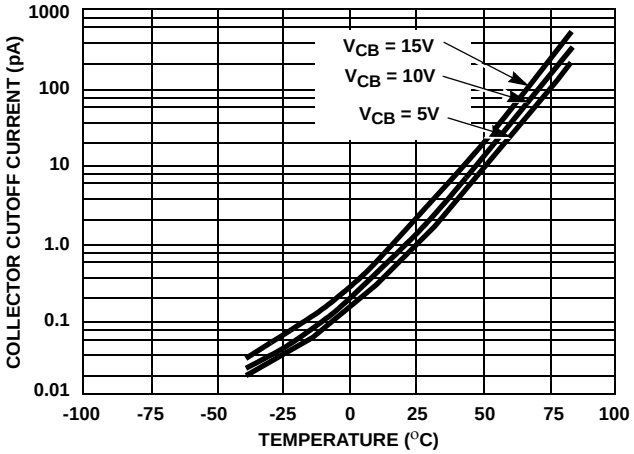


FIGURE 7. COLLECTOR CUTOFF CURRENT vs TEMPERATURE

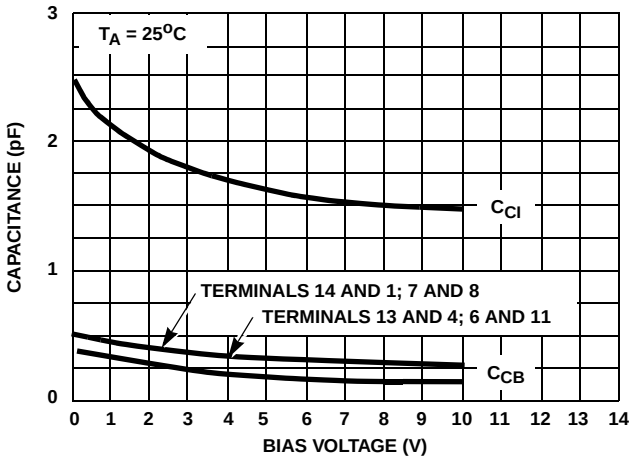


FIGURE 8. CAPACITANCE vs DC BIAS VOLTAGE

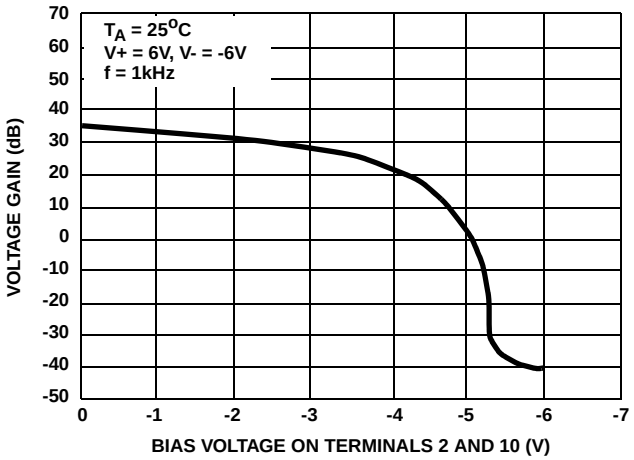


FIGURE 9. VOLTAGE GAIN vs DC BIAS VOLTAGE

Typical Performance Curves (Continued)

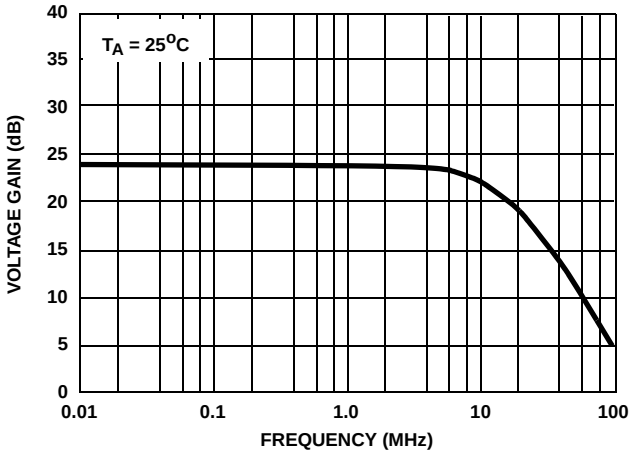


FIGURE 10. VOLTAGE GAIN vs FREQUENCY

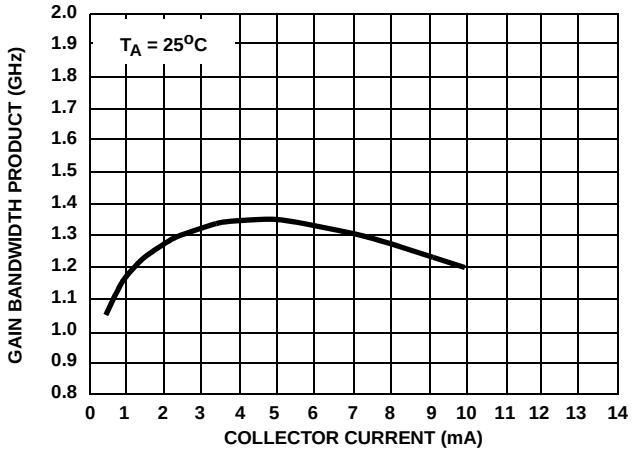


FIGURE 11. GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

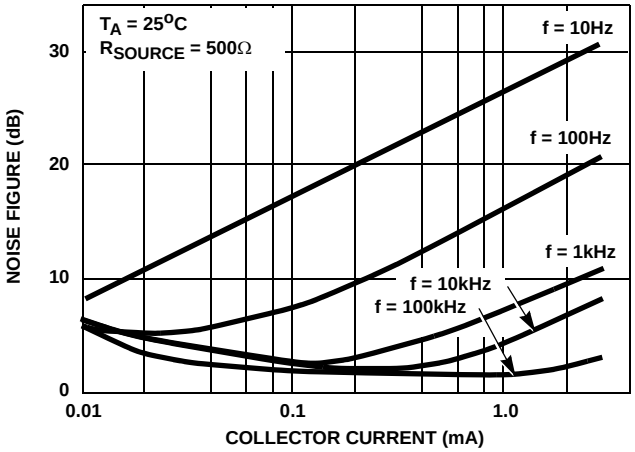


FIGURE 12. 1/f NOISE FIGURE vs COLLECTOR CURRENT

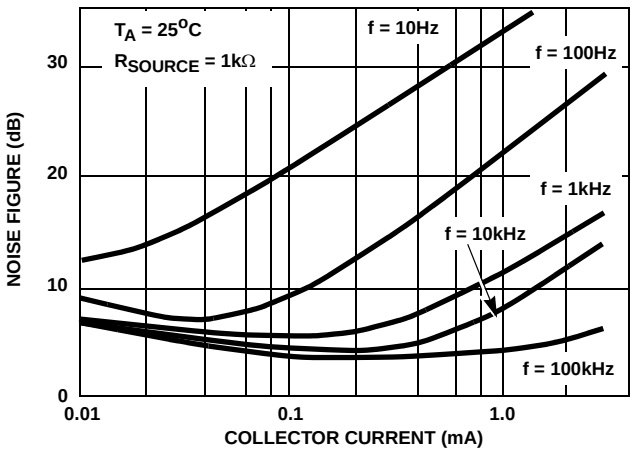


FIGURE 13. 1/f NOISE FIGURE vs COLLECTOR CURRENT

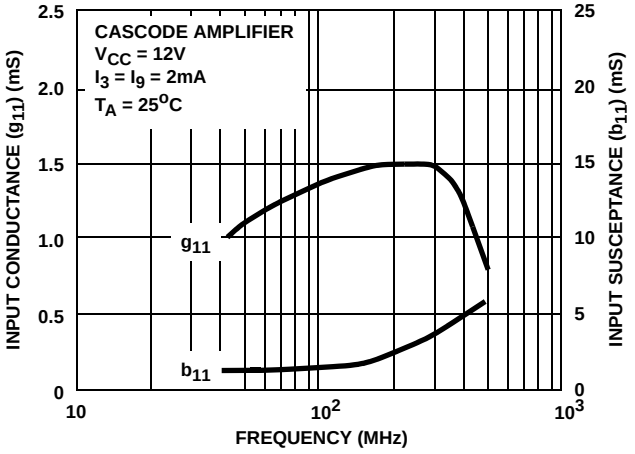


FIGURE 14. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

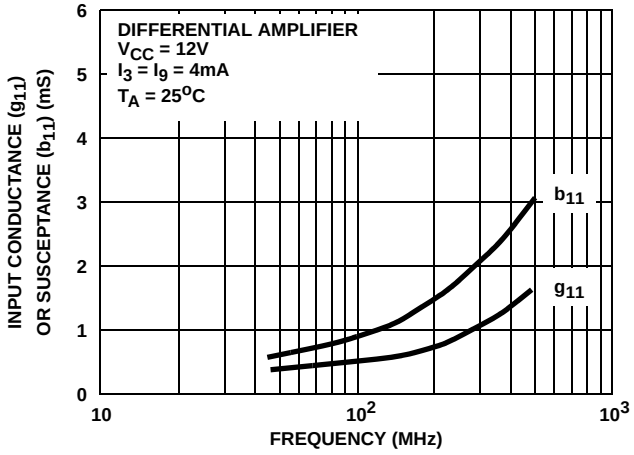


FIGURE 15. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

Typical Performance Curves (Continued)

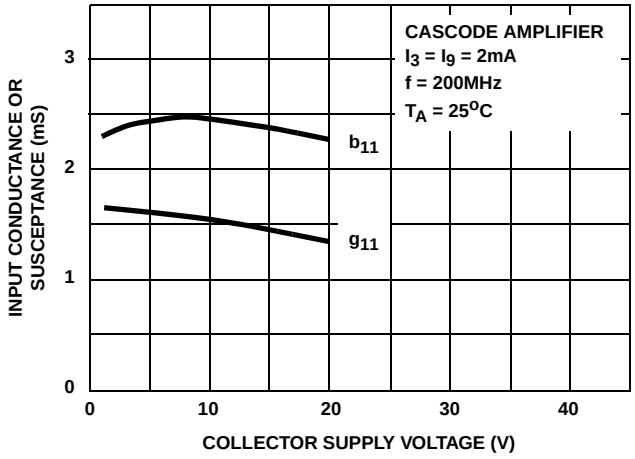


FIGURE 16. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR SUPPLY VOLTAGE

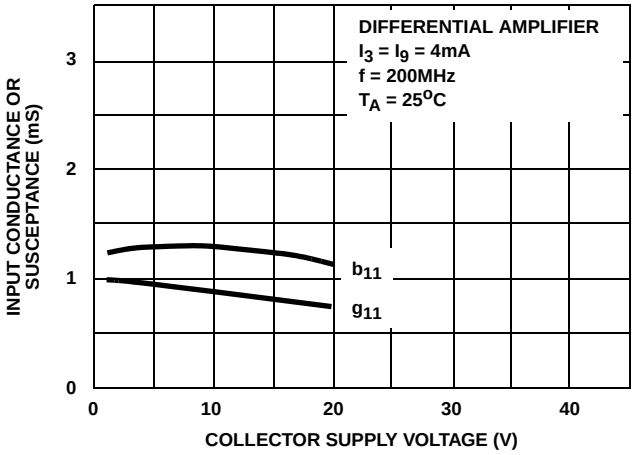


FIGURE 17. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR SUPPLY VOLTAGE

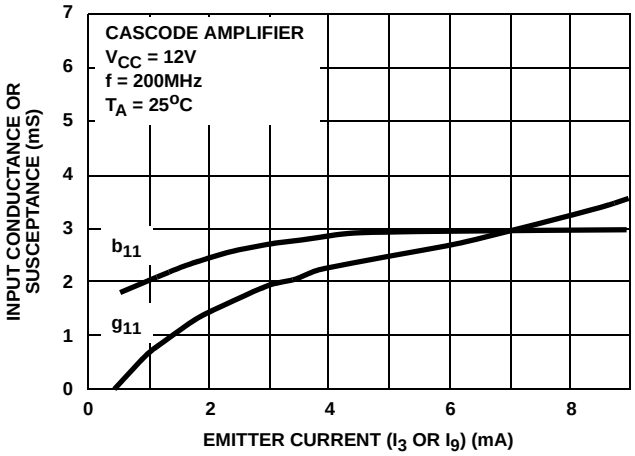


FIGURE 18. INPUT ADMITTANCE (Y_{11}) vs EMITTER CURRENT

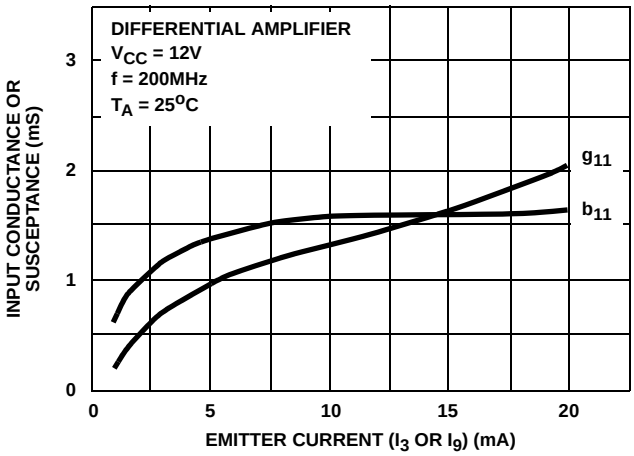


FIGURE 19. INPUT ADMITTANCE (Y_{11}) vs EMITTER CURRENT

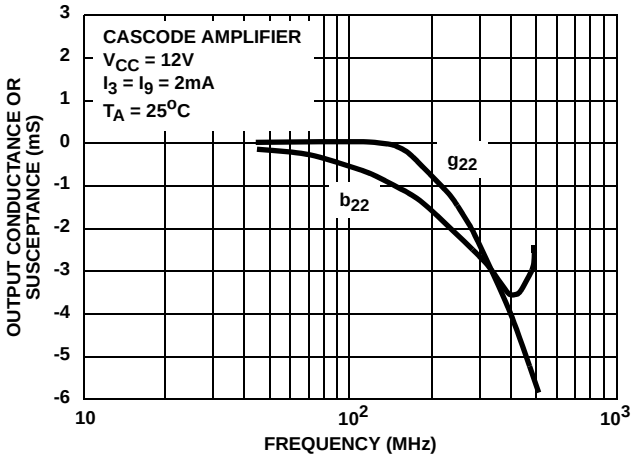


FIGURE 20. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

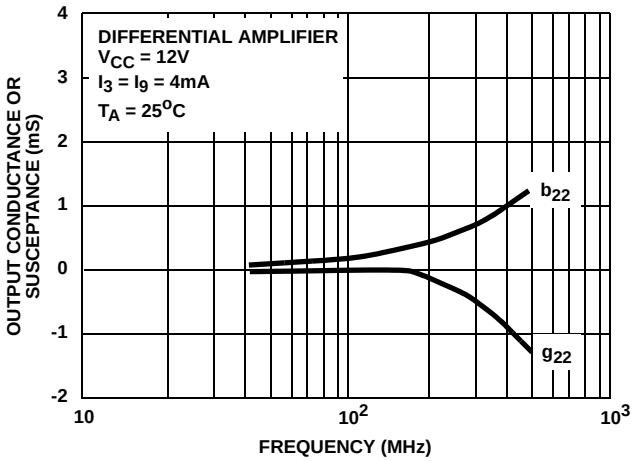


FIGURE 21. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

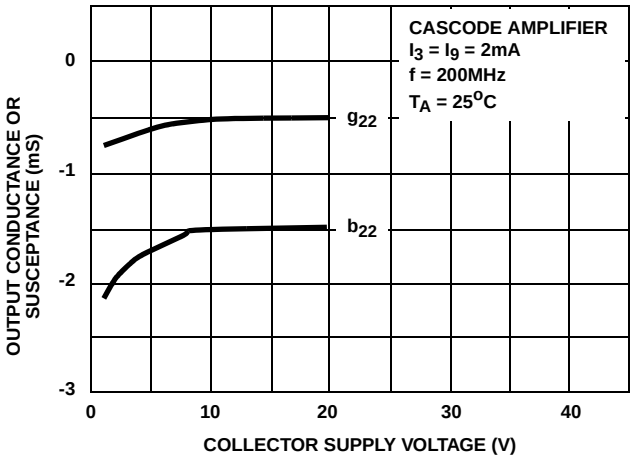


FIGURE 22. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR SUPPLY VOLTAGE

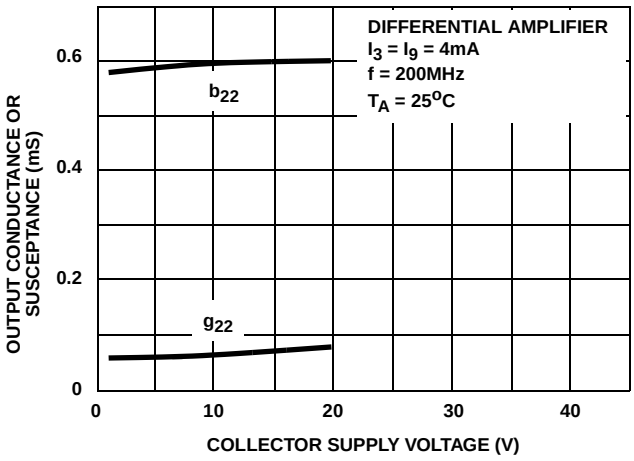


FIGURE 23. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR SUPPLY VOLTAGE

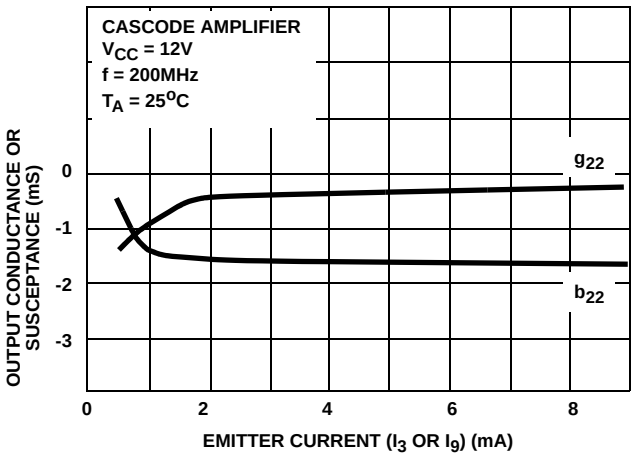


FIGURE 24. OUTPUT ADMITTANCE (Y_{22}) vs EMITTER CURRENT

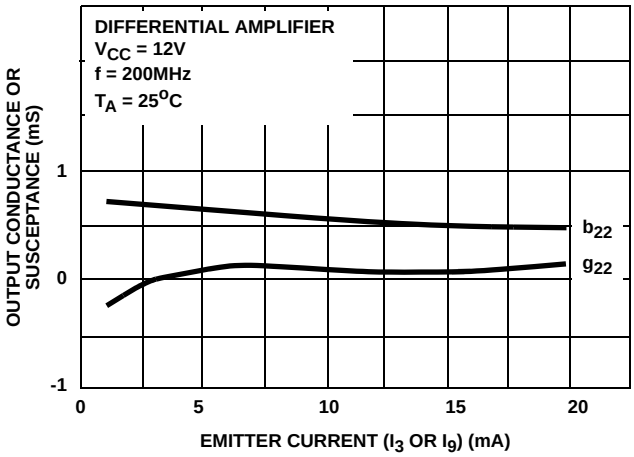


FIGURE 25. OUTPUT ADMITTANCE (Y_{22}) vs EMITTER CURRENT

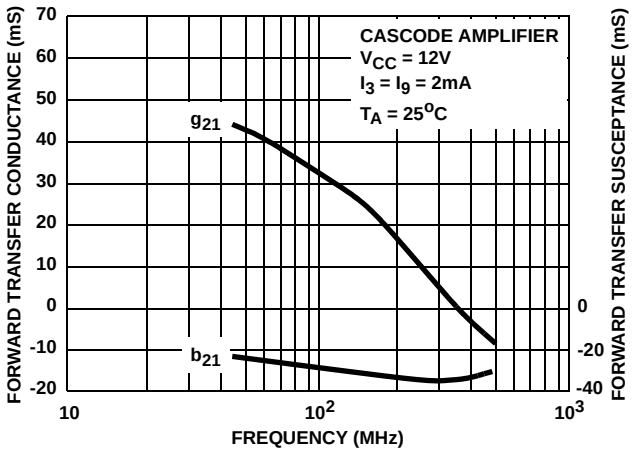


FIGURE 26. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

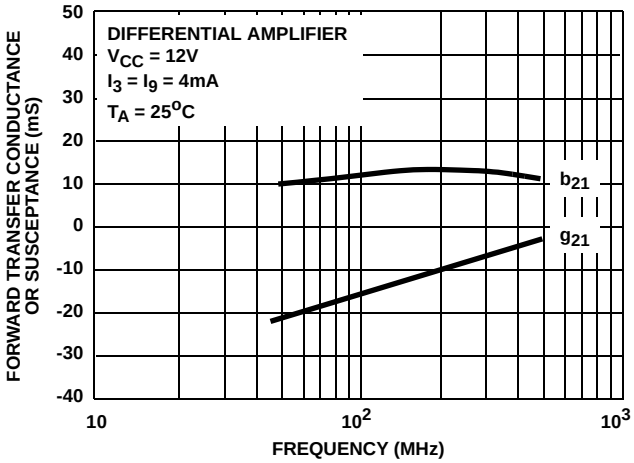


FIGURE 27. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

Typical Performance Curves (Continued)

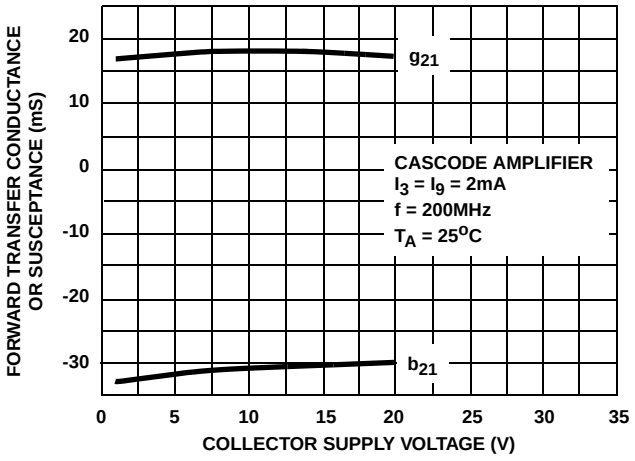


FIGURE 28. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs COLLECTOR SUPPLY VOLTAGE

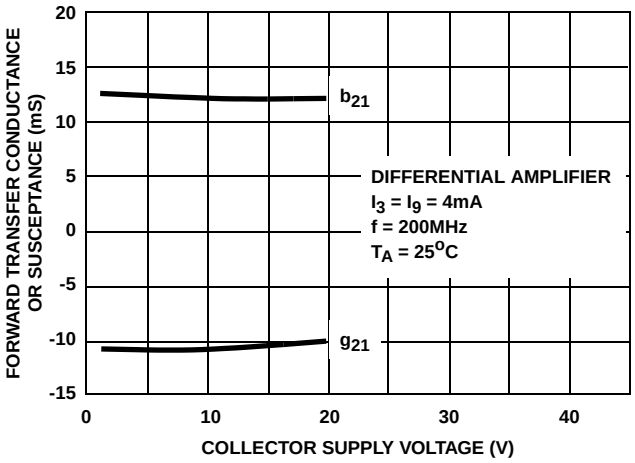


FIGURE 29. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs COLLECTOR SUPPLY VOLTAGE

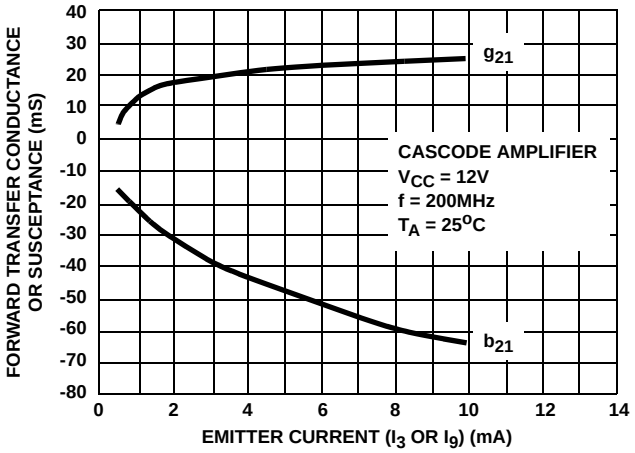


FIGURE 30. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs EMITTER CURRENT

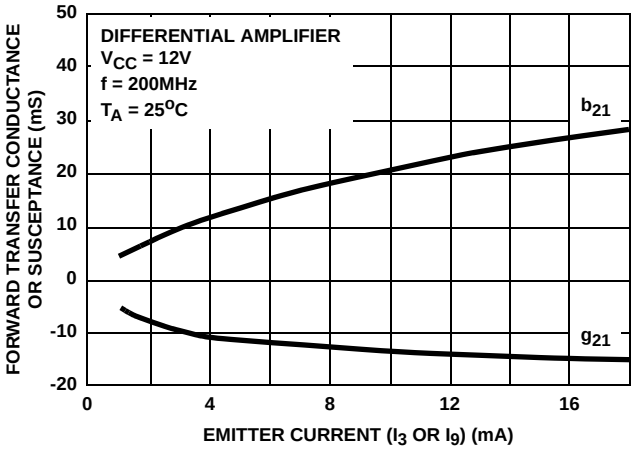
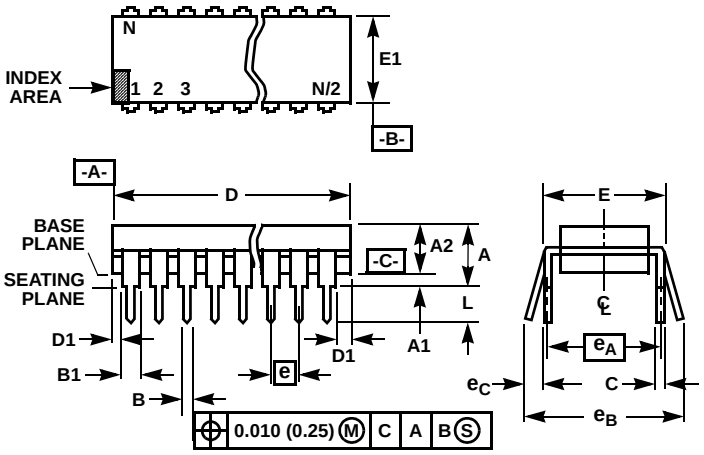


FIGURE 31. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs EMITTER CURRENT

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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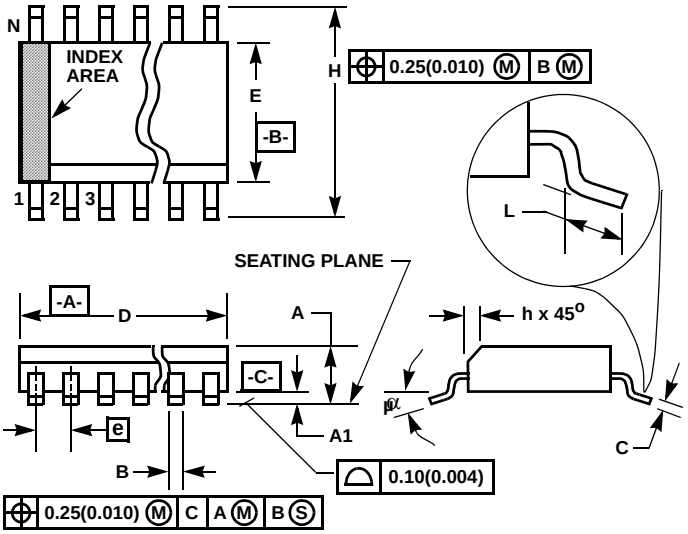
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

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