REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. - ro	02-09-19	R. MONNIN
B	Drawing updated as part of 5 year review. -rrp	07-08-13	ROBERT M. HEBER

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
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REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B			
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY
RICK C. OFFICER

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
CHARLES E. BESORE

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
91-11-22

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, LINEAR, OPERATIONAL AMPLIFIER, WIDEBAND, HIGH SLEW RATE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87787**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87787	01	C	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HA-2539	High slew rate wideband operational amplifier
02	EL-2039	High slew rate wideband operational amplifier

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage between $+V_S$ and $-V_S$ terminals ..... 35 V dc
Differential input voltage (V_{ID}) ..... 6.0 V dc
Voltage at either input terminal ..... $+V_S$ to $-V_S$
Peak output current (< 10 % duty cycle) ..... 50 mA
Power dissipation (P_D):
Case C ..... 1.03 W 1/
Case 2 ..... 1.06 W 2/
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +275°C
Junction temperature (T_J) ..... +175°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):
Case C ..... 98°C/W
Case 2 ..... 95°C/W

1/ Derate linearly above T_A = +75°C at 10.2 mW/°C.
2/ Derate linearly above T_A = +75°C at 10.6 mW/°C.

1.4 Recommended operating conditions.

Positive supply voltage range ($+V_S$) ..... +12 V dc to +15 V dc
Negative supply voltage range ($-V_S$) ..... -12 V dc to -15 V dc
Common mode input voltage (V_{CM}) ..... $\leq |(+V_S - (-V_S)) / 2|$
Load resistance (R_L) ..... 1.0 kΩ
Ambient operating temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V_{IO}	V_{CM} = 0 V	1	01	-10	+10	mV
			2,3		-15	+15	
			1	02	-2	+2	
			2,3		-6	+6	
Input bias current	$+I_{IB}$	V_{CM} = 0 V	1	All	-20	+20	µA
			2,3		-25	+25	
	$-I_{IB}$		1		-20	+20	
			2,3		-25	+25	
Input offset current	I_{IO}	V_{CM} = 0 V	1	All	-6	+6	µA
			2,3		-8	+8	
Common mode input range	$+V_{CM}$	$+V_S$ = +5 V, $-V_S$ = -25 V	1,2,3	All	10		V
	$-V_{CM}$	$+V_S$ = +25 V, $-V_S$ = -5 V				-10	
Large signal voltage gain	$+A_{VOL}$	V_{OUT} = 0 V and +10 V,	1	All	10		kV/V
		R_L = 1 kΩ	2,3		5		
	$-A_{VOL}$	V_{OUT} = 0 V and -10 V,	1		10		
		R_L = 1 kΩ	2,3		5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Common mode rejection ratio	+CMRR	ΔV_{CM} = +10 V, $+V_S$ = +5 V, $-V_S$ = -25 V, V_{OUT} = -10 V	1,2,3	All	60		dB
	-CMRR	ΔV_{CM} = -10 V, $+V_S$ = +25 V, $-V_S$ = -5 V, V_{OUT} = +10 V			60		
Output current	$+I_{OUT}$	V_{OUT} = -10 V, T_A = +25°C	1	All	10		mA
	$-I_{OUT}$	V_{OUT} = +10 V, T_A = +25°C				-10	
Output voltage swing	$+V_{OUT}$	R_L = 1 kΩ	1,2,3	All	+10		V
	$-V_{OUT}$					-10	
Quiescent power supply current	$+I_{CC}$	I_{OUT} = 0 mA, V_{OUT} = 0 V	1,2,3	01		25	mA
				02		17	
	$-I_{CC}$			01	-25		
				02	-17		
Power supply rejection ratio	+PSRR	$+V_S$ = +5.0 V and +15 V, $-V_S$ = -15 V	1,2,3	All	60		dB
	-PSRR	$-V_S$ = -5.0 V and -15 V, $+V_S$ = +15 V			60		
Quiescent power consumption 2/ 3/	P_C	V_{OUT} = 0 V, I_{OUT} = 0 mA	1,2,3	01		720	mW
				02		510	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain bandwidth product 2/	GBWP	V_{OUT} = 100 mV, f_O = 1 MHz, T_A = +25°C	4	01	370		MHz
				02	550		
		V_{OUT} = 100 mV, f_O = 60 MHz, T_A = +25°C		01	400		
				02	600		
Output resistance 2/	R_{OUT}	T_A = +25°C	4	All		60	Ω
Full power bandwidth 2/ 4/	FPBW	V_{PEAK} = 10 V, T_A = +25°C	4	All	8.4		MHz
Closed loop stable gain 2/	CLSG	R_L = 1 kΩ, C_L ≤ 10 pF	4,5,6	All	10		V/V
Slew rate 2/	+SR	V_{OUT} = -5.0 V to +5.0 V, R_L = 1 kΩ, A_V = 10 V/V, measured at –4.0 V to +4.0 V	7	01	530		V/µs
			8		425		
		V_{OUT} = -5.0 V to +5.0 V, R_L = 1 kΩ, A_V = 10 V/V, measured at –2.5 V to +2.5 V	7	02	530		
			8		425		
	-SR	V_{OUT} = +5.0 V to -5.0 V, R_L = 1 kΩ, A_V = 10 V/V, measured at –4.0 V to +4.0 V	7	01	530		
			8		425		
		V_{OUT} = +5.0 V to -5.0 V, R_L = 1 kΩ, A_V = 10 V/V, measured at –2.5 V to +2.5 V	7	02	530		
			8		425		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Rise time 2/ 5/	t_R	V_{OUT} = 0 V to +200 mV, T_A = +25°C	9	All		10	ns
Fall time 2/ 5/	t_F	V_{OUT} = 0 V to -200 mV, T_A = +25°C	9	All		10	ns
Overshoot 2/	+OS	V_{OUT} = 0 V to +200 mV, T_A = +25°C	9	All		50	%
	-OS	V_{OUT} = 0 V to -200 mV, T_A = +25°C				50	

1/ For all tests, unless otherwise specified, $+V_S$ = +15 V, $-V_S$ = -15 V, and $C_L \le 10$ pF. Unless otherwise specified, for dc tests, R_S = 100 Ω, R_L = 100 kΩ, V_{OUT} = 0 V, and for ac tests, A_V = +10 V/V.

2/ If not tested, shall be guaranteed to the limits specified in table I herein.

3/ Quiescent power consumption based on quiescent supply current test maximum (no load on outputs).

4/ Full power bandwidth = SR / (2 x π x V_{PEAK}).

5/ Rise and fall times measured between 10 percent and 90 percent point.

Device types	01 and 02	
Case outlines	C	2
Terminal number	Terminal symbol	
1	+INPUT	NC
2	NC	+INPUT
3	$-V_S$	NC
4	NC	$-V_S$
5	NC	NC
6	NC	NC
7	NC	NC
8	OUTPUT	NC
9	NC	NC
10	$+V_S$	NC
11	NC	NC
12	NC	OUTPUT
13	NC	NC
14	-INPUT	$+V_S$
15	---	NC
16	---	NC
17	---	NC
18	---	NC
19	---	NC
20	---	-INPUT

NC = No connection

FIGURE 1. Terminal connections.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 10 and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*,2,3,4,5,6
Group A test requirements (method 5005)	1,2,3,4,5,6,7**,8**,9
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 7 and 8 shall be guaranteed, if not tested, to the limits specified in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-08-13

Approved sources of supply for SMD 5962-87787 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/ .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8778701CA	34371	HA1-2539/883
	3/	EHA1-2539/883B
5962-87787012A	3/	HA4-2539/883
	3/	EHA4-2539/883B
5962-8778702CA	3/	EL2039J/883B
5962-87787022A	3/	EL2039L/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803 Point of contact: 1650 Robert J. Conlan Blvd Palm Bay, FL 32905