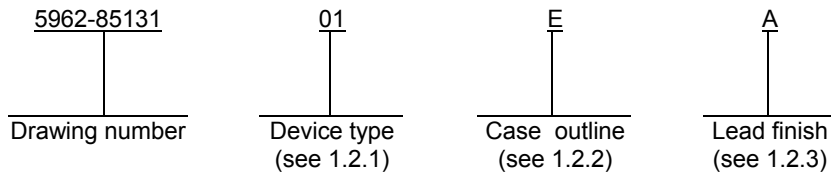


REVISIONS																				
LTR	DESCRIPTION										DATE (YR-MO-DA)					APPROVED				
A	Add case outlines, terminal connections and thermal resistance values for case outlines 2 and 3. For device type 01, 02, and 03, add subgroup 3 to I_{IH} and I_{IL} test, add R_{DS1} test, add V_{ISO} test, delete V_{CT} test, change R_L and C_L test conditions for $t_{ON(A)}$ and $t_{OFF(A)}$ tests, change C_L test condition for $t_{ON(EN)}$ and $t_{OFF(EN)}$ tests, change value of I_D for R_{DS1} test, change value of I_D and V_S for R_{DS2} test, add test condition circuits. Editorial changes throughout.										88-08-26					D. A. DiCENZO				
B	Add device types 07, 08, and 09. Table I changes. Editorial changes throughout.										93-06-28					M. A. FRYE				
C	Changes in accordance with NOR 5962-R061-95.										95-01-25					M. A. FRYE				
D	Changes in accordance with NOR 5962-R032-96.										96-01-09					M. A. FRYE				
E	Incorporate NOR's and current requirements. Editorial changes throughout. - drw										02-12-30					R. MONNIN				
F	Make change to the $t_{ON(A)}$ and $t_{OFF(A)}$ subgroup 9 test limit for devices 01, 02, and 03 as specified under Table I. - ro										07-09-13					R. HEBER				
REV	F	F	F																	
SHEET	35	36	37																	
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS				REV		F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14	
PMIC N/A				PREPARED BY MARCIA B. KELLEHER						DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dscc.dla.mil										
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY RAY MONNIN																
				APPROVED BY D. A. DiCENZO						MICROCIRCUIT, LINEAR, CMOS, MULTIPLEXER / DEMULTIPLEXER, MONOLITHIC SILICON										
				DRAWING APPROVAL DATE 86-06-30																
				REVISION LEVEL F						SIZE A	CAGE CODE 67268			5962-85131						
						SHEET 1 OF 37														

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	HI546	Single 16-channel MUX/DEMUX with overvoltage protection
02	HI547	Differential 8-channel MUX/DEMUX with overvoltage protection
03	HI549	Differential 4-channel MUX/DEMUX with overvoltage protection
04	HI5116	Single 16-channel MUX/DEMUX with overvoltage protection
05	HI5216	Differential 8-channel MUX/DEMUX with overvoltage protection
06	HI5208	Differential 4-channel MUX/DEMUX with overvoltage protection
07	HI506	Single 16-channel MUX/DEMUX
08	HI507	Differential 8-channel MUX/DEMUX
09	HI509	Differential 4-channel MUX/DEMUX

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP-T16 or CDIP-T16	16	Dual-in-line
X	GDIP-T28 or CDIP-T28	28	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

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1.3 Absolute maximum ratings.

Supply voltage between +V and -V	+44 V
Supply voltage between +V and ground:	
Device types 01-03, 07-09	+22 V
Device types 04-06	+20 V
Supply voltage between -V and ground:	
Device types 01-03, 07-09	-25 V
Device types 04-06	-20 V
Digital input voltage range (V_A , V_{EN}):	
Device types 01-03, 07-09	[(-V) -4 V] to (+V) +4 V] or 20 mA whichever comes first
Device types 04-06	-V to +V or 20 mA whichever comes first
Analog input voltage range (V_S):	
Device types 01-03	[(-V) -20 V] to (+V) +20 V]
Device types 04-06	[(-V) -25 V] to (+V) +25 V]
Device types 07-09	[(-V) -2 V] to (+V) +2 V]
Continuous current, source or drain	20 mA
Peak current, source or drain, pulsed, 1 ms, 10 percent duty cycle max	40 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D):	
Case E	1.25 W
Case X	2 W
Case 2	1.32 W
Case 3	1.23 W
Derating factor:	
Case E	12.5 mW/°C above $T_A = +75^\circ\text{C}$
Case X	20 mW/°C above $T_A = +75^\circ\text{C}$
Case 2	13.2 mW/°C above $T_A = +75^\circ\text{C}$
Case 3	12.3 mW/°C above $T_A = +75^\circ\text{C}$
Thermal resistance, junction-to-case (θ_{JC}):	
Cases E, X, 2, and 3.....	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E	80°C/W
Case X	50°C/W
Case 2	76°C/W
Case 3	81°C/W
Lead temperature (soldering, 10 seconds)	+275°C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage between +V and ground	+15 V
Supply voltage between -V and ground	-15 V
V_{REF} (device types 01 and 02 only)	open
$V_{AL}(\text{max})$	0.8 V
$V_{AH}(\text{min})$:	
Device types 01-03	4.0 V
Device types 04-09	2.4 V
V_{EN} :	
Device types 01-03	4.0 V
Device types 04-09	2.4 V
Ambient operating temperature range (T_A)	-55°C to +125°C

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current <u>2/</u>	I _{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3	01, 02, 03, 04, 05, 07, 08, 09		1.0	μA
			1, 3	06	-1.0	1.0	
			2		-10.0	10.0	
	I _{IL}		1, 2, 3	01, 02, 03, 04, 05, 07, 08, 09		1.0	
			1, 3	06	-1.0	1.0	
			2		-10.0	10.0	
Leakage current into the source terminal of an “OFF” switch	+I _{S(OFF)}	V _S = +10 V, V _{EN} = 0.8 V, all unused inputs = -10 V, V _D = -10 V	1	01, 02, 03, 07, 08, 09	-10	+10	nA
				04, 05, 06	-1	+1	
			2, 3	All	-50	+50	
	-I _{S(OFF)}	V _S = -10 V, V _{EN} = 0.8 V, all unused inputs = +10 V, V _D = +10 V	1	01, 02, 03, 07, 08, 09	-10	+10	
				04, 05, 06	-1	+1	
			2, 3	All	-50	+50	
Leakage current into the drain terminal of an “OFF” switch	+I _{D(OFF)}	V _D = +10 V, V _{EN} = 0.8 V, all unused inputs = -10 V	1	01, 02, 03, 07, 08, 09	-10	+10	nA
				04, 05	-2	+2	
				06	-1	+1	
			2, 3	01, 04, 07	-300	+300	
				02, 08	-200	+200	
				03, 06, 09	-100	+100	
				05	-150	+150	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1</u> / -55°C ≤ T _A ≤ +125°C -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit			
					Min	Max				
Leakage current into the drain terminal of an “OFF” switch	-I _D (OFF)	V _D = -10 V, V _{EN} = 0.8 V, all unused inputs = +10 V	1	01, 02, 03, 07, 08, 09	-10	+10	nA			
				04, 05	-2	+2				
				06	-1	+1				
			2, 3	01, 04, 07	-300	+300				
				02, 08	-200	+200				
				03, 06, 09	-100	+100				
				05	-150	+150				
			Leakage current from an “ON” driver into the switch (drain)	+I _D (ON)	V _D = +10 V, V _S = +10 V, all unused inputs = -10 V	1		01, 02, 03, 07, 08, 09	-10	+10
04, 05, 06	-2	+2								
2, 3	01, 04, 07	-300				+300				
	02, 08	-200				+200				
	03, 06, 09	-100				+100				
	05	-150				+150				
	-I _D (ON)	V _D = -10 V, V _S = -10 V, all unused inputs = +10 V				1	01, 02, 03, 07, 08, 09	-10	+10	
							04, 05, 06	-2	+2	
2, 3				01, 04, 07	-300	+300				
				02, 08	-200	+200				
				03, 06, 09	-100	+100				
				05	-150	+150				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Overvoltage protected, leakage current into the drain terminal of an "OFF" switch	+I _{D(OFF)} overvoltage	V _S = +33 V, V _D = 0 V, V _{EN} = 0.8 V, V _S applied at ≤ 25% duty cycle	1, 2, 3	01, 02, 03,	-2.0	+2.0	μA
		V _S = +25 V, V _D = 0 V, V _{EN} = 0.8 V	1, 3	04, 05, 06	-2.0	+2.0	
			2		-5	+5	
	-I _{D(OFF)} overvoltage	V _S = -33 V, V _D = 0 V, V _{EN} = 0.8 V, V _S applied at ≤ 25% duty cycle	1, 2, 3	01, 02, 03,	-2.0	+2.0	
		V _S = -25 V, V _D = 0 V, V _{EN} = 0.8 V	1, 3	04, 05, 06	-2.0	+2.0	
			2		-5	+5	
Positive supply current	+I	V _A = 0 V, V _{EN} = 4.0 V	1, 2, 3	01, 02, 03		2.0	mA
		V _A = 0 V, V _{EN} = 2.4 V		04, 05		2.0	
				07, 08		3.0	
				09		2.4	
		V _A = 5 V, V _{EN} = 2.4 V		06		2.0	
Negative supply current	-I	V _A = 0 V, V _{EN} = 4.0 V	1, 2, 3	01, 02, 03	-1.0		mA
		V _A = 0 V, V _{EN} = 2.4 V		04, 05, 07, 08, 09	-1.0		
		V _A = 5 V, V _{EN} = 2.4 V		06	-1.0		
Standby positive supply current	+I _{SBY}	V _A = 0 V, V _{EN} = 0 V	1, 2, 3	01, 02, 03, 04, 05, 06		2.0	mA
				07, 08		3.0	
				09		2.4	
Standby negative supply current	-I _{SBY}	V _A = 0 V, V _{EN} = 0 V	1, 2, 3	All	-1.0		mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Switch "ON" resistance	+R _{DS1}	V _S = +10 V, I _D = -100 μA	1	01, 02, 03		1.5	kΩ
			2, 3			1.8	
		V _S = +10 V, I _D = +100 μA	1	04, 05, 06		1.5	
			2, 3			2.0	
		V _S = +10 V, I _D = -1 mA	1	07, 08, 09		300	Ω
			2, 3			400	
	-R _{DS1}	V _S = -10 V, I _D = +100 μA	1	01, 02, 03		1.5	kΩ
			2, 3			1.8	
		V _S = -10 V, I _D = -100 μA	1	04, 05, 06		1.5	
			2, 3			2.0	
		V _S = -10 V, I _D = +1 mA	1	07, 08, 09		300	Ω
			2, 3			400	
	+R _{DS2} <u>3/</u>	+V = +10 V, -V = -10 V, V _S = +5.0 V, I _D = +100 μA	1, 3	04, 05, 06		2.2	kΩ
			2			2.4	
		+V = +10 V, -V = -10 V, V _S = -5.0 V, I _D = -100 μA	1, 3	04, 05, 06		2.2	
			2			2.4	
Difference in switch "ON" resistance between channels	ΔR _{DS1}	(+R _{DS1} max) – (+R _{DS1} min) x 100 +R _{DS1} Ave, T _A = +25°C	1	01, 02, 03		7	%
		(-R _{DS1} max) – (-R _{DS1} min) x 100 -R _{DS1} Ave, T _A = +25°C				7	
Capacitance: Address	C _A	+V = -V = 0 V, f = 1 MHz, T _A = +25°C, see 4.3.1c	4	01, 02, 03		15	pF
				04, 05, 06 <u>3/</u>		10	
				07, 08		12	
				09		10	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Capacitance: Output switch	C _{OS}	+V = -V = 0 V, f = 1 MHz, T _A = +25°C, see 4.3.1c	4	01		85	pF
				02, 08		50	
				03, 09		25	
				04, 05, 06 ^{3/}		85	
				07		90	
Capacitance: Input switch	C _{IS}	+V = -V = 0 V, f = 1 MHz, T _A = +25°C, see 4.3.1c	4	01, 02, 03		15	pF
				04, 05, 06 ^{3/}		10	
				07, 08, 09		12	
Charge transfer error	V _{CTE}	V _S = GND, T _A = +25°C, ^{3/} V _{GEN} = 0 V to 5 V	7	All		10	mV
Off isolation	V _{ISO}	V _{EN} = 0.8 V, V _S = 7 V _{rms} , R _L = 1 kΩ, C _L = 15 pF, f = 100 kHz, T _A = +25°C ^{3/}	7	01, 02, 03, 07, 08, 09		-50	dB
Single channel isolation	V _{ISO}	V _{EN} = 0 V, V _{GEN} = 1 V _{p-p} , R _L = 200 Ω, f = 200 kHz, T _A = +25°C ^{3/}	7	04, 05, 06		-50	dB
Crosstalk between channels	V _{CT}	V _{GEN} = 1 V _{p-p} , f = 200 kHz, T _A = +25°C ^{3/}	7	04, 05, 06		-50	dB
Break-before-make time delay	t _D	T _A = +25°C, see figure 3	9	01, 02, 03,	5		ns
				04, 05, 06 ^{3/}	5		
		R _L = 1 kΩ, C _L = 50 pF, T _A = +25°C, see figure 3		07, 08, 09	25		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C -V = -15 V, +V = +15 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay times: Address inputs to I/O channels times:	t _{ON(A)}	R _L = 10 kΩ, C _L = 50 pF, see figure 4	9	01, 02, 03		750	ns
	t _{OFF(A)}			07, 08, 09		500	
		R _L = 1 kΩ, C _L = 100 pF, see figure 4	10, 11	01, 02, 03, 07, 08, 09		1,000	
			9	04, 05, 06		1,000	
			10, 11			1,500	
Enable to I/O	t _{ON(EN)}	R _L = 1 kΩ, C _L = 50 pF, see figure 4	9	01, 02, 03, 07, 08, 09		500	ns
	t _{OFF(EN)}		10, 11			1,000	
		R _L = 1 kΩ, C _L = 100 pF, See figure 4	9	04, 05, 06		700	
			10, 11			1,000	

^{1/} For device types 01 and 02, V_{REF} = open. For device types 01, 02, and 03, V_{EN} = 4.0 V unless otherwise specified. For device types 04, 05, 06, 07, 08 and 09, V_{EN} = 2.4 V unless otherwise specified. For device types 04, 05, and 06, current flowing in either direction between any associated input and output terminals of the switch shall be 30 mA.

^{2/} Input current of one input mode.

^{3/} Guaranteed, if not tested, to the limits specified.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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Case outlines	E	X	X	X	X	2	3	3	3	3
Device types	03, 06, 09	01	02	04, 07	05, 08	03, 06, 09	01	02	07	08
Terminal number	Terminal symbol									
1	A0	V+	V+	V+	V+	NC	V+	V+	V+	V+
2	Enable	NC	OUT B	NC	OUT B	A0	NC	OUT B	NC	OUT B
3	V-	NC	NC	NC	NC	Enable	NC	NC	NC	NC
4	IN 1A	IN 16	IN 8B	IN 16	IN 8B	V-	IN 16	IN 8B	IN 16	IN 8B
5	IN 2A	IN 15	IN 7B	IN 15	IN 7B	IN 1A	IN 15	IN 7B	IN 15	IN 7B
6	IN 3A	IN 14	IN 6B	IN 14	IN 6B	NC	IN 14	IN 6B	IN 14	IN 6B
7	IN 4A	IN 13	IN 5B	IN 13	IN 5B	IN 2A	IN 13	IN 5B	IN 13	IN 5B
8	OUT A	IN 12	IN 4B	IN 12	IN 4B	IN 3A	IN 12	IN 4B	IN 12	IN 4B
9	OUT B	IN 11	IN 3B	IN 11	IN 3B	IN 4A	IN 11	IN 3B	IN 11	IN 3B
10	IN 4B	IN 10	IN 2B	IN 10	IN 2B	OUT A	IN 10	IN 2B	IN 10	IN 2B
11	IN 3B	IN 9	IN 1B	IN 9	IN 1B	NC	IN 9	IN 1B	IN 9	IN 1B
12	IN 2B	GND	GND	GND	GND	OUT B	GND	GND	GND	GND
13	IN 1B	VREF	VREF	NC	NC	IN 4B	VREF	VREF	NC	NC
14	V+	A3	NC	A3	NC	IN 3B	A3	NC	A3	NC
15	GND	A2	A2	A2	A2	IN 2B	A2	A2	A2	A2
16	A1	A1	A1	A1	A1	NC	A1	A1	A1	A1
17	---	A0	A0	A0	A0	IN 1B	A0	A0	A0	A0
18	---	Enable	Enable	Enable	Enable	V+	Enable	Enable	Enable	Enable
19	---	IN 1	IN 1A	IN 1	IN 1A	GND	IN 1	IN 1A	IN 1	IN 1A
20	---	IN 2	IN 2A	IN 2	IN 2A	A1	IN 2	IN 2A	IN 2	IN 2A
21	---	IN 3	IN 3A	IN 3	IN 3A	---	IN 3	IN 3A	IN 3	IN 3A
22	---	IN 4	IN 4A	IN 4	IN 4A	---	IN 4	IN 4A	IN 4	IN 4A
23	---	IN 5	IN 5A	IN 5	IN 5A	---	IN 5	IN 5A	IN 5	IN 5A
24	---	IN 6	IN 6A	IN 6	IN 6A	---	IN 6	IN 6A	IN 6	IN 6A
25	---	IN 7	IN 7A	IN 7	IN 7A	---	IN 7	IN 7A	IN 7	IN 7A
26	---	IN 8	IN 8A	IN 8	IN 8A	---	IN 8	IN 8A	IN 8	IN 8A
27	---	V-	V-	V-	V-	---	V-	V-	V-	V-
28	---	OUT	OUT A	OUT	OUT A	---	OUT	OUT A	OUT	OUT A

FIGURE 1. Terminal connections.

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Device types 01, 04, and 07

A3	A2	A1	A0	EN	CHANNEL SELECTED
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

Device types 02, 05, and 08

A2	A1	A0	EN	CHANNEL SELECTED
X	X	X	L	NONE
L	L	L	H	1A, 1B
L	L	H	H	2A, 2B
L	H	L	H	3A, 3B
L	H	H	H	4A, 4B
H	L	L	H	5A, 5B
H	L	H	H	6A, 6B
H	H	L	H	7A, 7B
H	H	H	H	8A, 8B

Device types 03, 06, and 09

A1	A0	EN	CHANNEL SELECTED
X	X	L	NONE
L	L	H	1A, 1B
L	H	H	2A, 2B
H	L	H	3A, 3B
H	H	H	4A, 4B

FIGURE 2. Truth tables.

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Device type 01

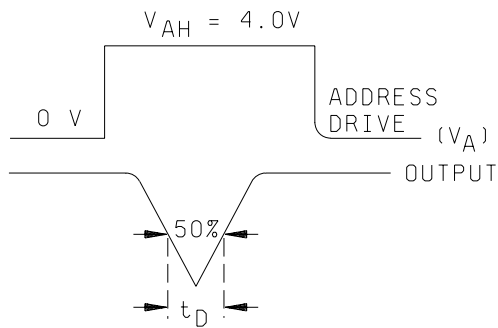
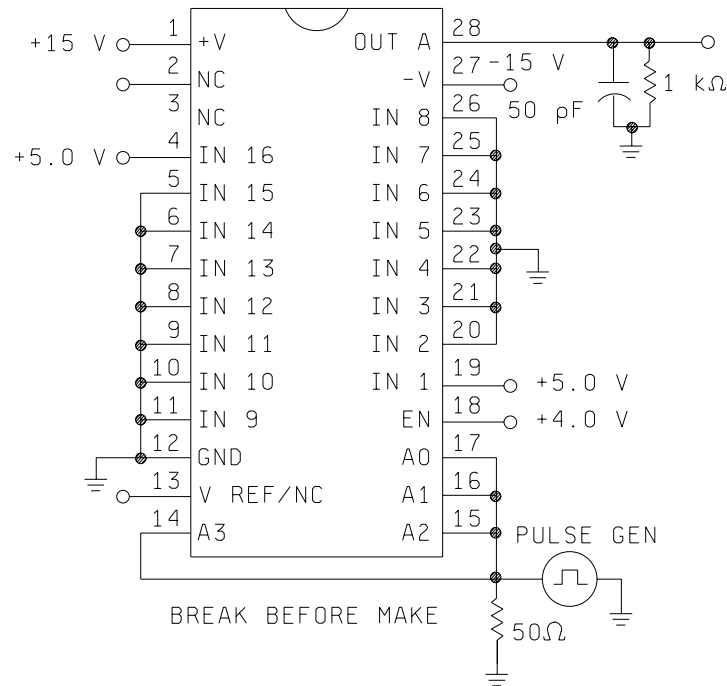


FIGURE 3. Break-before-make test circuit and waveforms.

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Device type 02

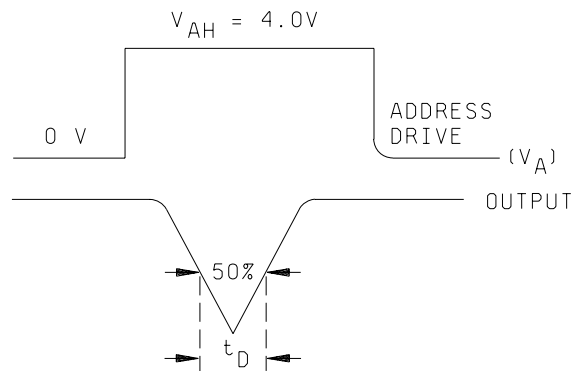
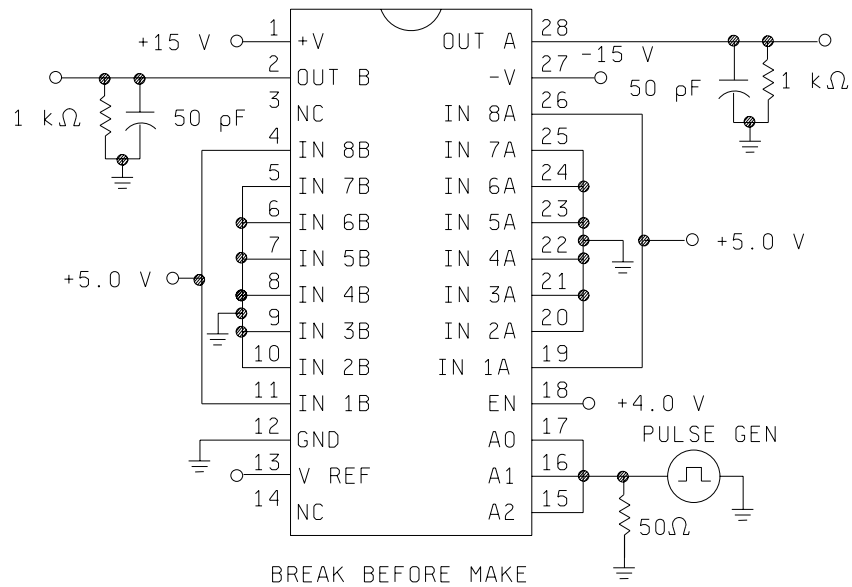


FIGURE 3. Break-before-make test circuit and waveforms – continued.

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DEFENSE SUPPLY CENTER COLUMBUS
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Device type 03

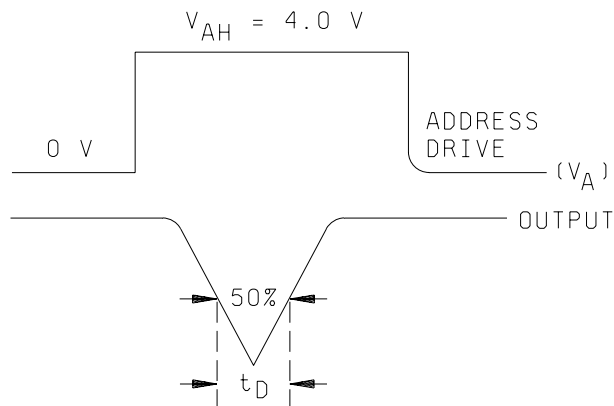
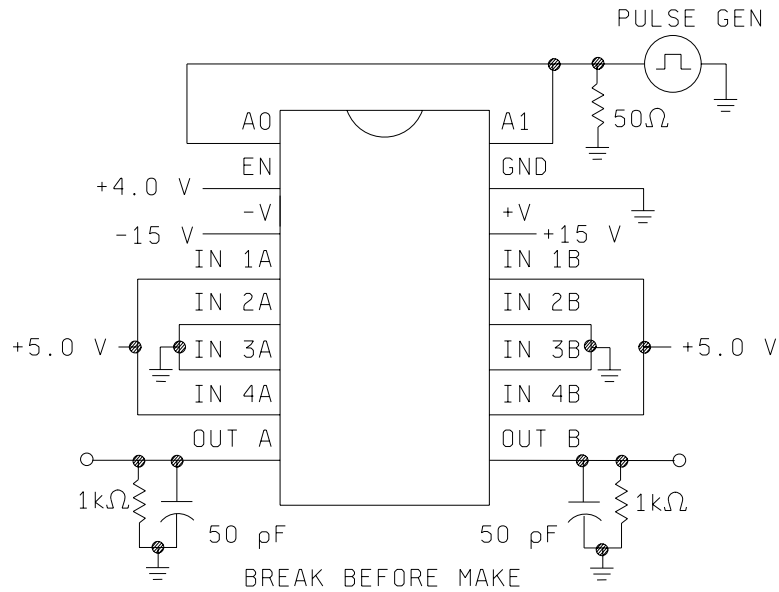


FIGURE 3. Break-before-make test circuit and waveforms – continued.

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Device types 04, 05, and 06

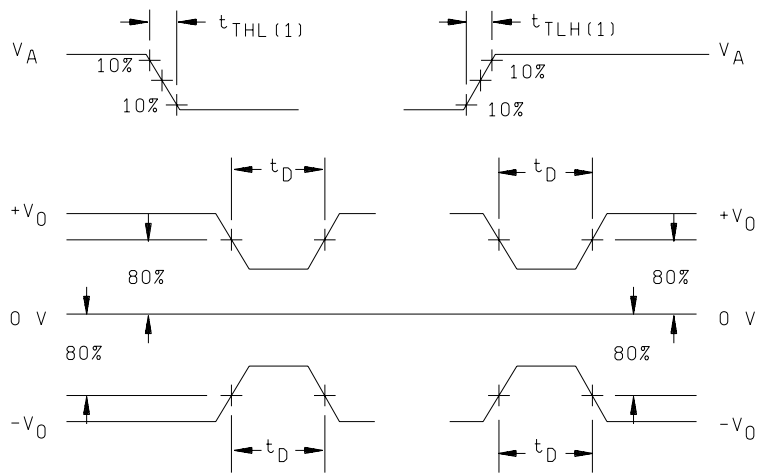
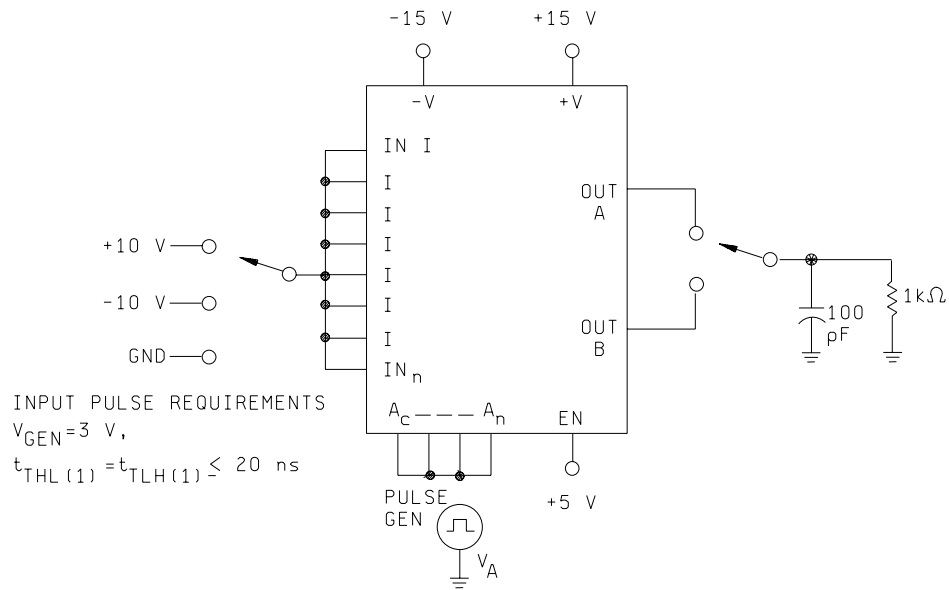


FIGURE 3. Break-before-make test circuit and waveforms – continued.

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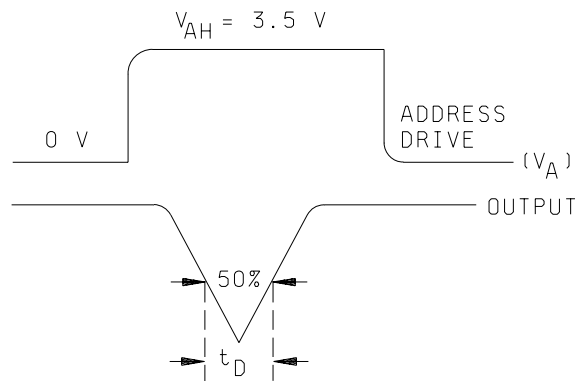
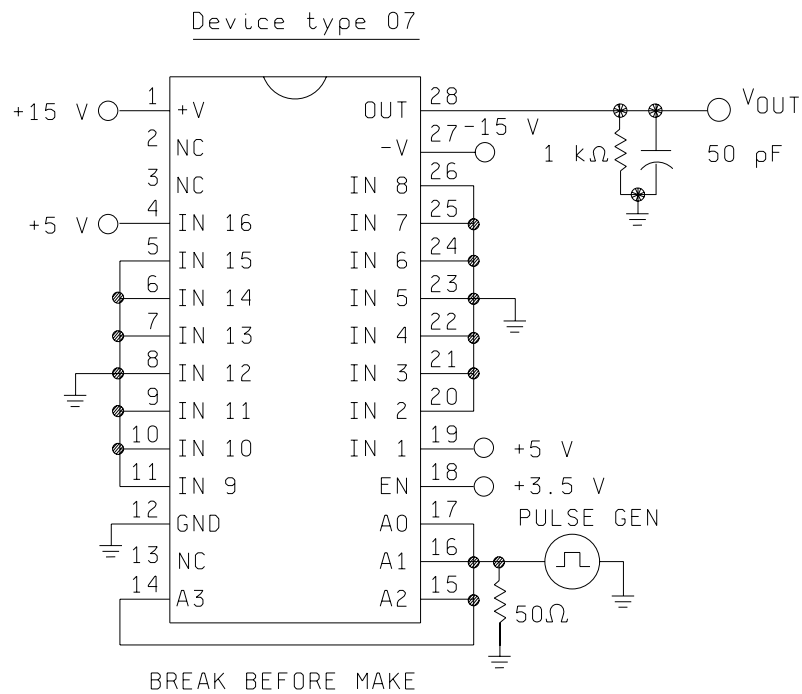


FIGURE 3. Break-before-make test circuit and waveforms – continued.

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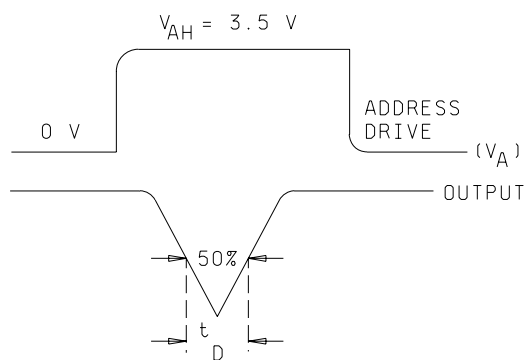
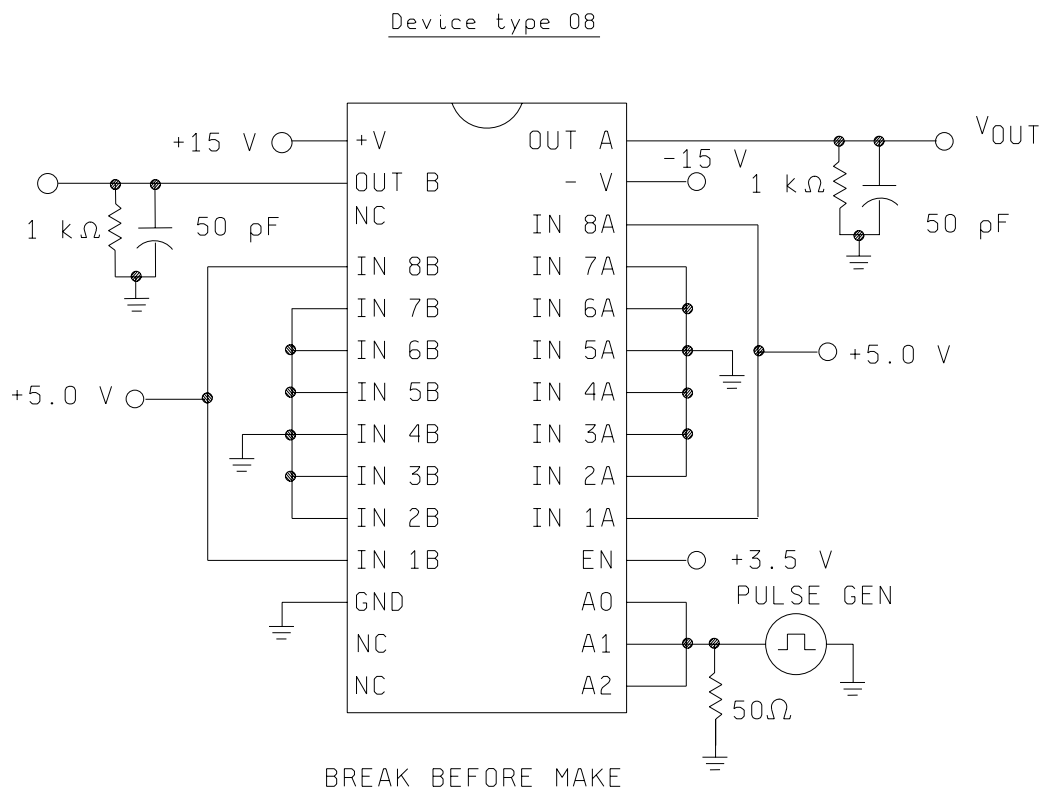


FIGURE 3. Break-before-make test circuit and waveforms – continued.

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Device type 09

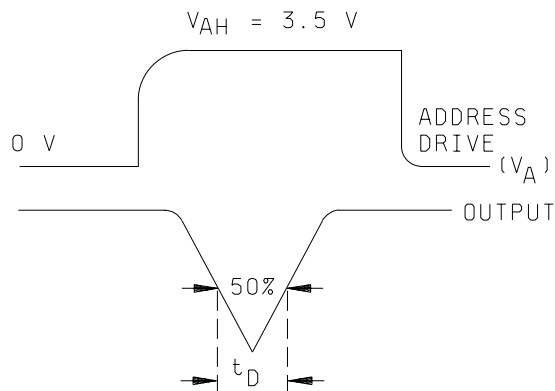
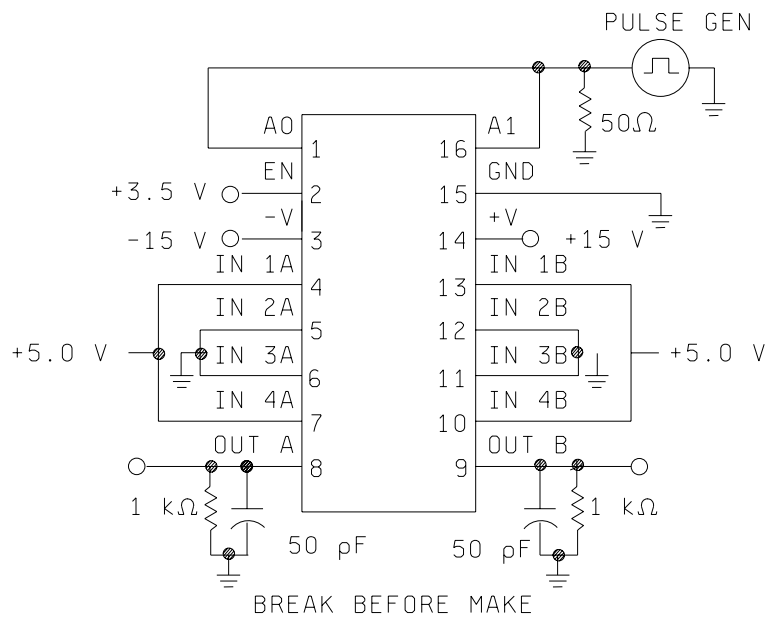


FIGURE 3. Break-before-make test circuit and waveforms – continued.

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Device type 01

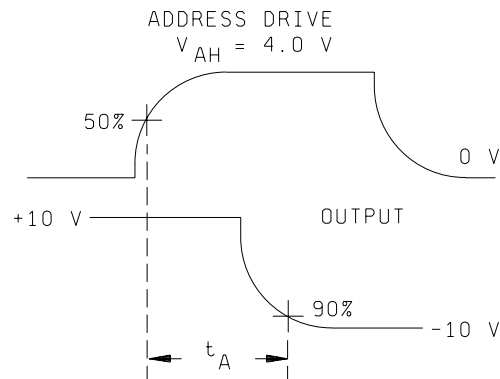
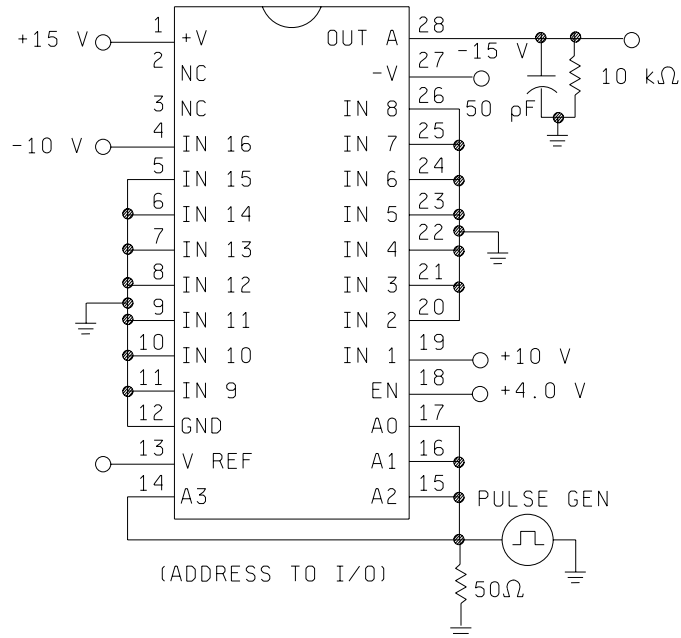


FIGURE 4. Switching times test circuits.

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DEFENSE SUPPLY CENTER COLUMBUS
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SHEET
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Device type 01

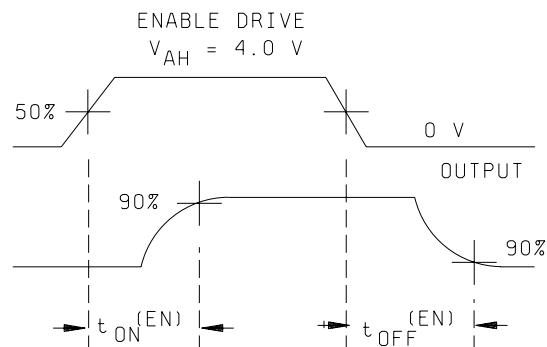
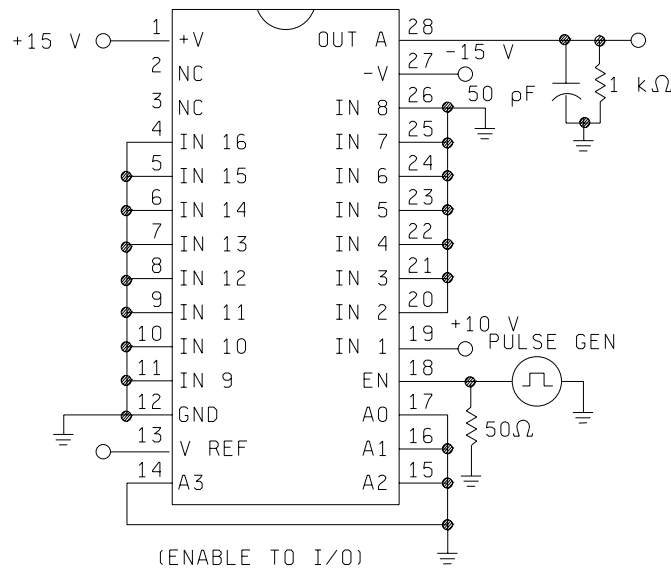


FIGURE 4. Switching times test circuits – continued.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
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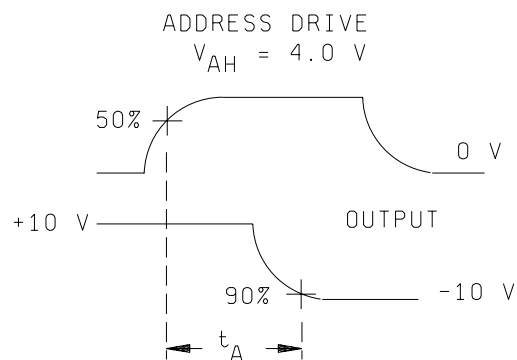
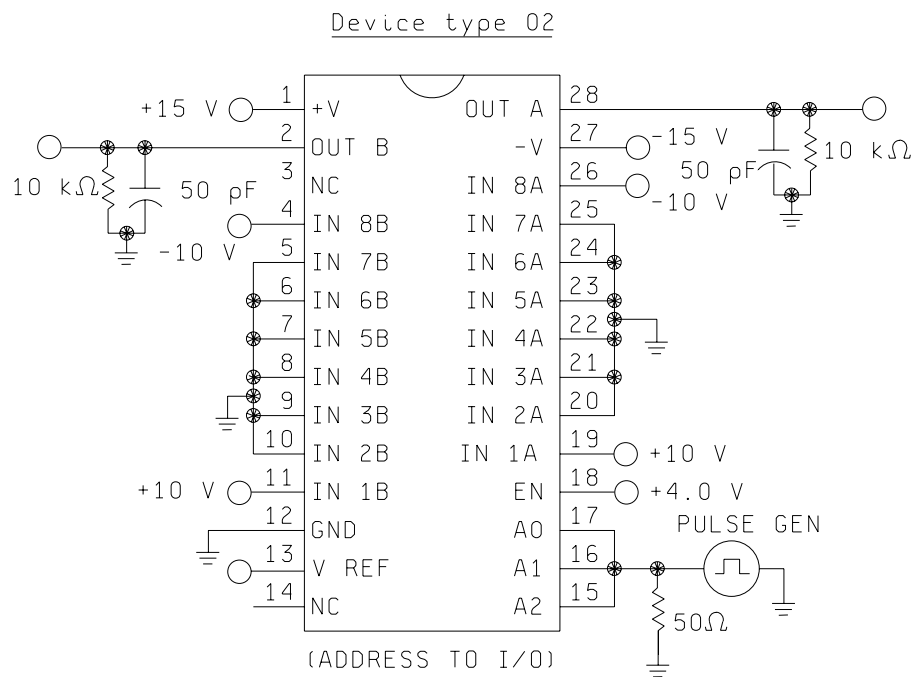


FIGURE 4. Switching times test circuits – continued.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
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SIZE
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REVISION LEVEL
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SHEET
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Device type 02

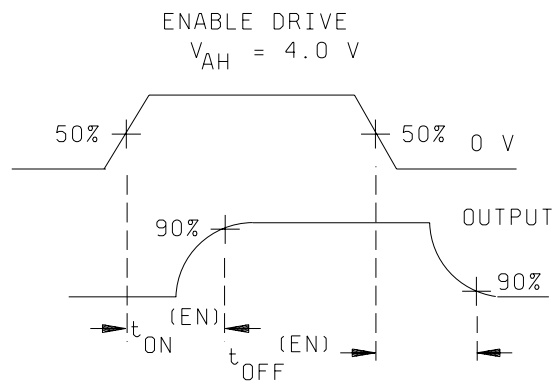
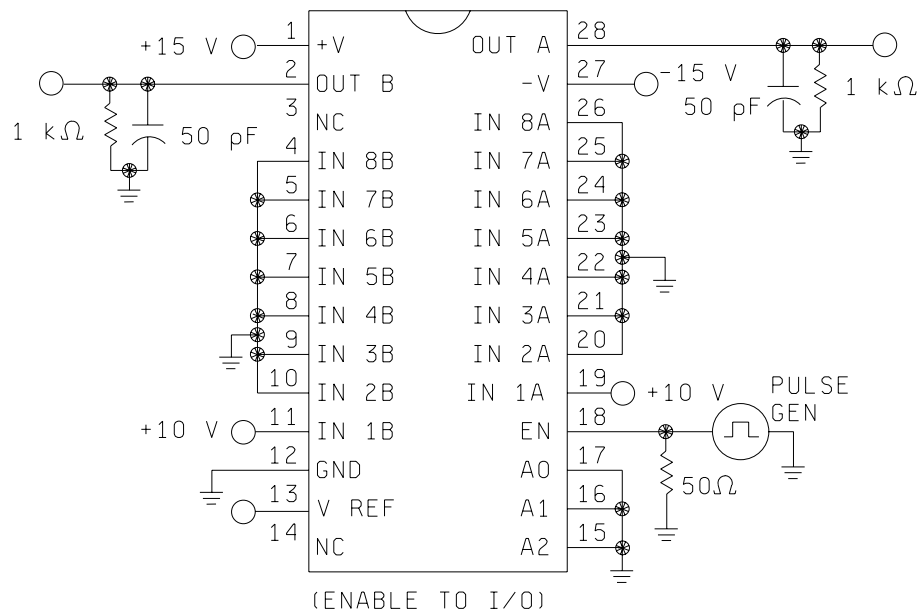


FIGURE 4. Switching times test circuits – continued.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
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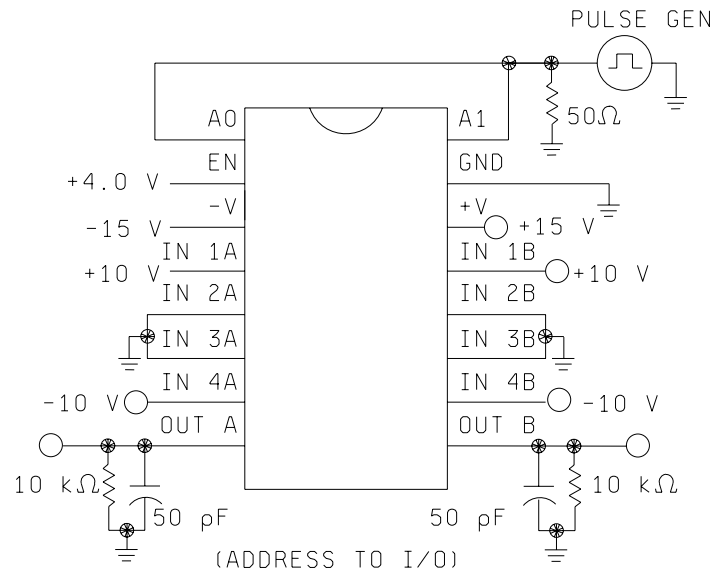
SIZE
A

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Device type 03



ADDRESS DRIVE

$V_{AH} = 4.0 \text{ V}$ for device type 03

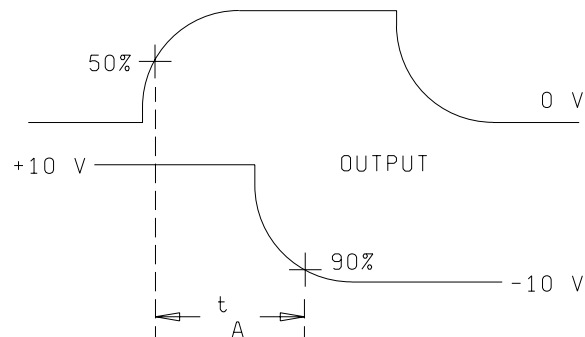


FIGURE 4. Switching times test circuits – continued.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
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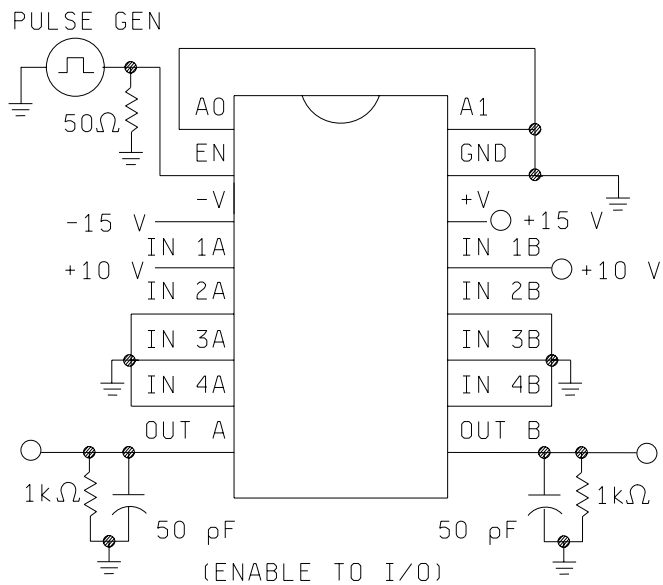
SIZE
A

REVISION LEVEL
F

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SHEET
24

Device type 03



ENABLE DRIVE

$V_{AH} = 4.0 \text{ V}$ for device type 03

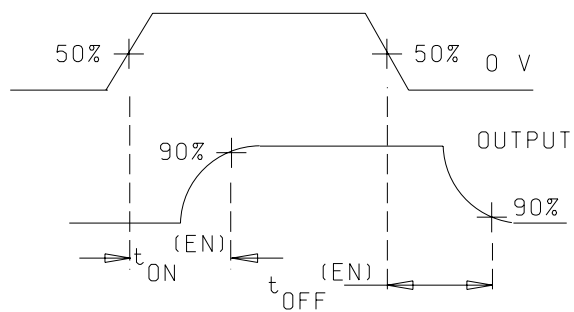


FIGURE 4. Switching times test circuits – continued.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
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Device type 04

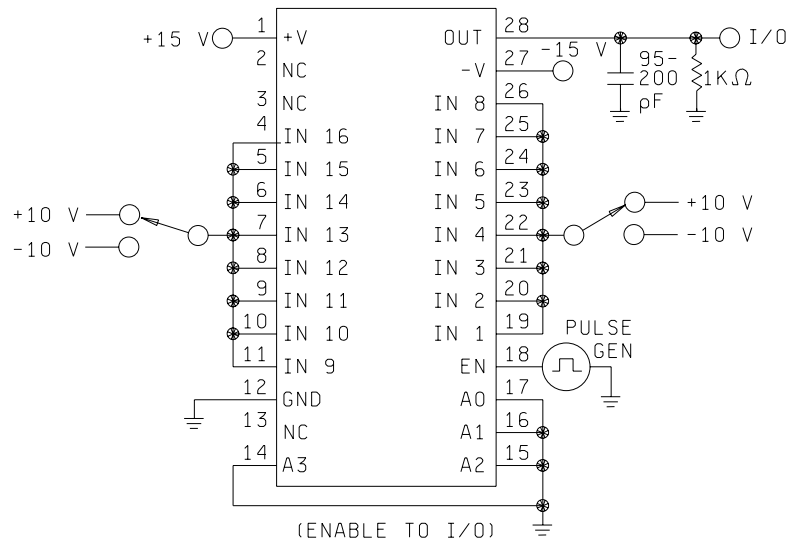
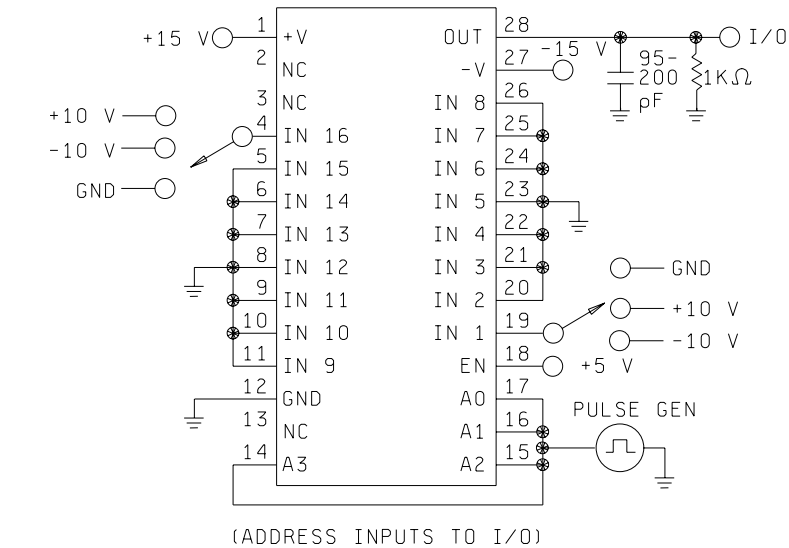


FIGURE 4. Switching times test circuits – continued.

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MICROCIRCUIT DRAWING**
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Device type 05



FIGURE 4. Switching times test circuits – continued.

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MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
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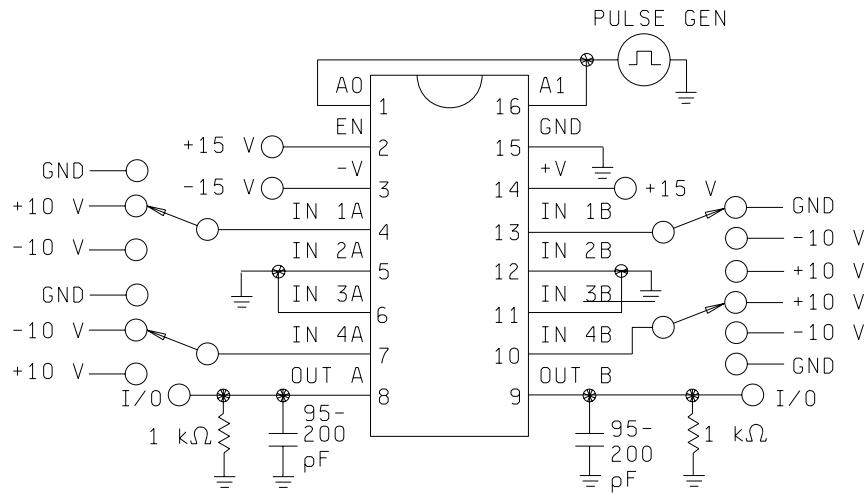
SIZE
A

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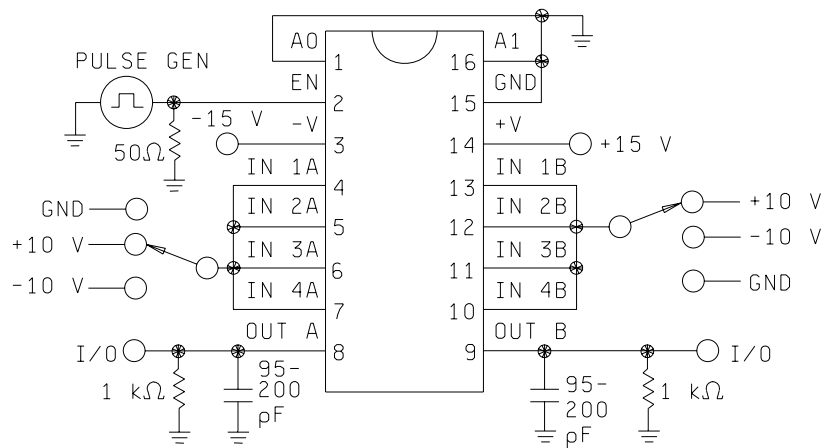
REVISION LEVEL
F

SHEET **27**

Device type 06



(ADDRESS INPUTS TO I/O)



(ENABLE TO I/O)

FIGURE 4. Switching times test circuits – continued.

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Device type 07

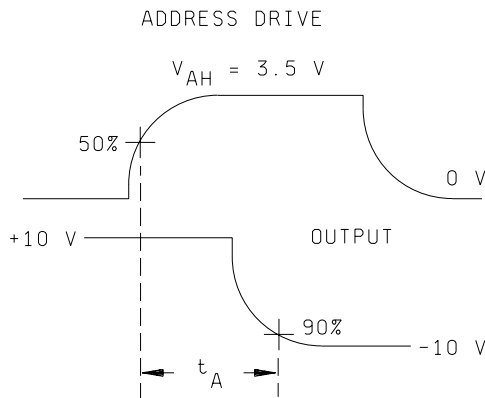
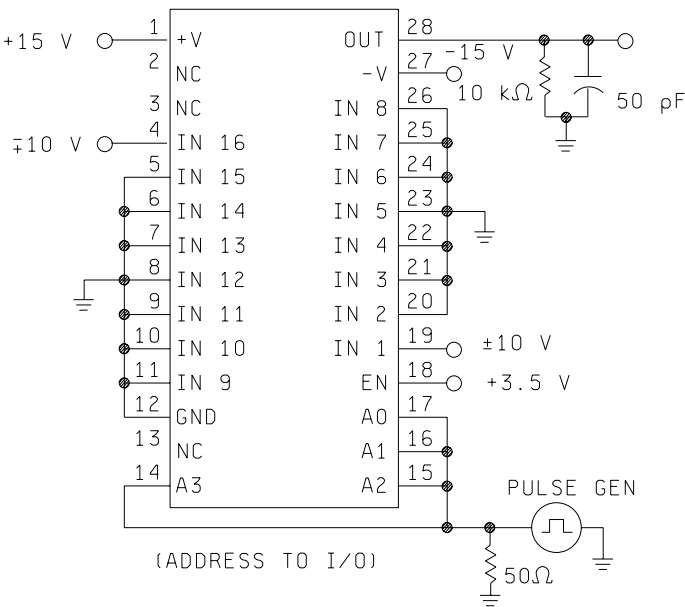


FIGURE 4. Switching times test circuits – continued.

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Device type 07

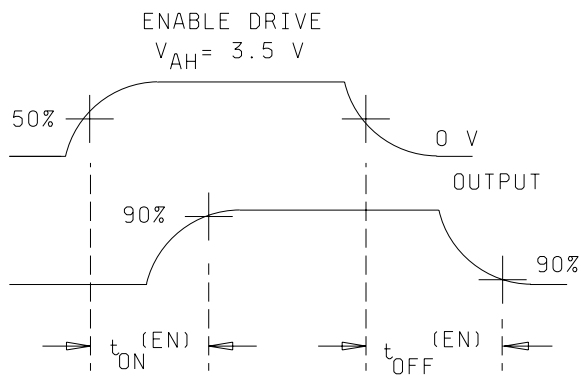
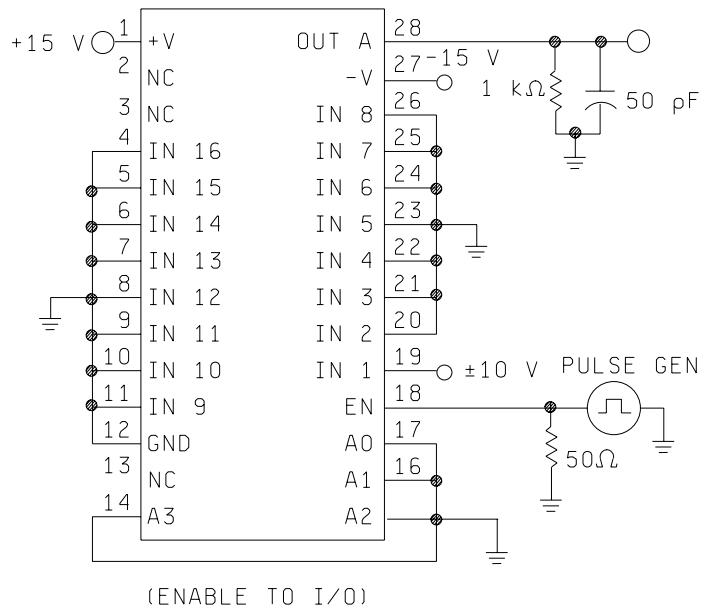


FIGURE 4. Switching times test circuits – continued.

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MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
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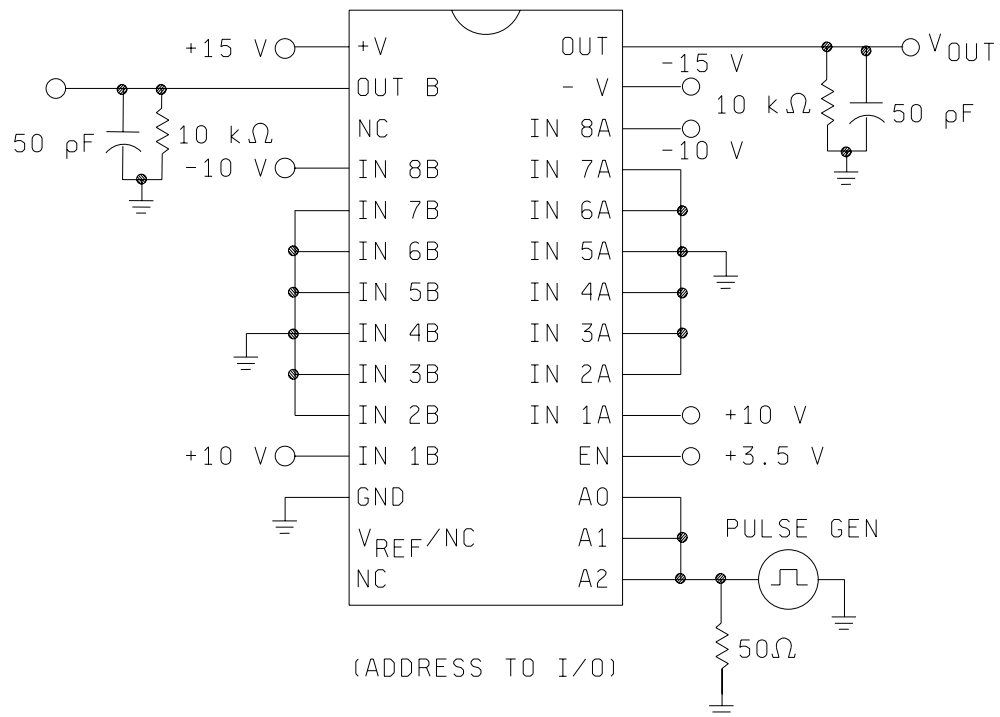
SIZE
A

REVISION LEVEL
F

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SHEET
30

Device type 08



(ADDRESS TO I/O)

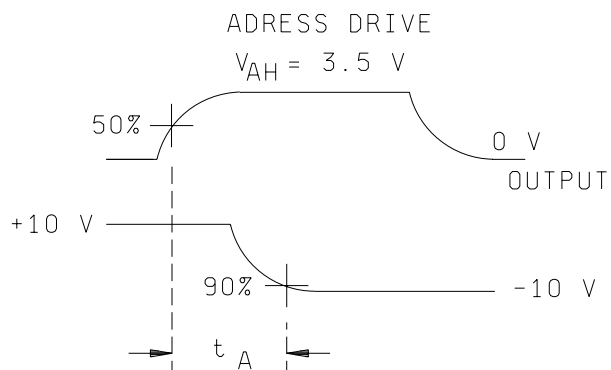


FIGURE 4. Switching times test circuits – continued.

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MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
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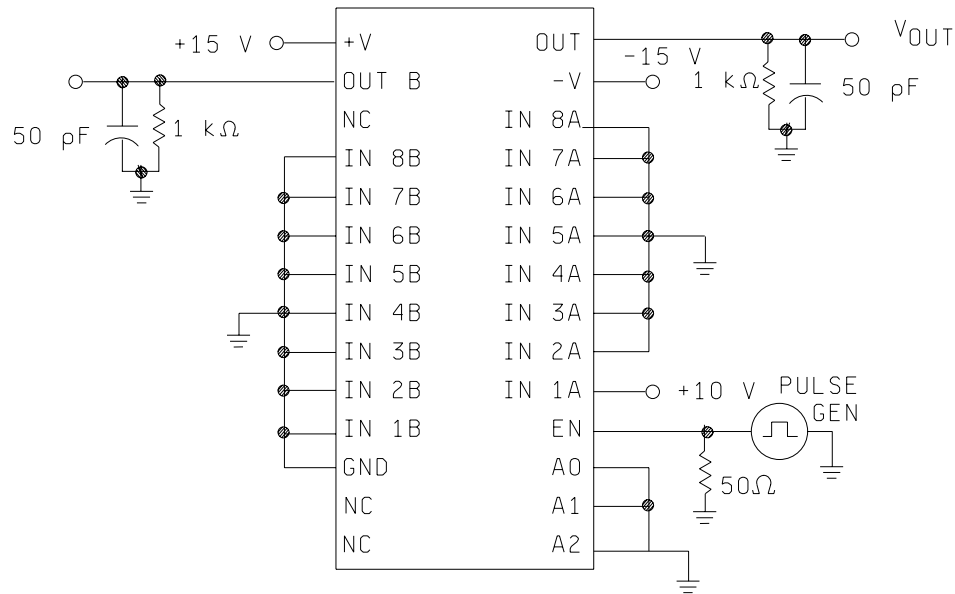
SIZE
A

REVISION LEVEL
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SHEET
31

Device type 08



(ENABLE TO I/O)

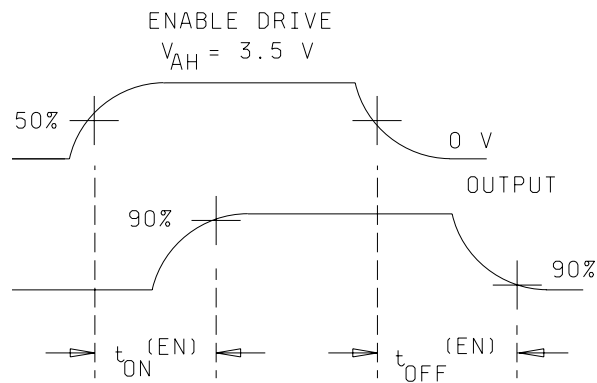


FIGURE 4. Switching times test circuits – continued.

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Device type 09

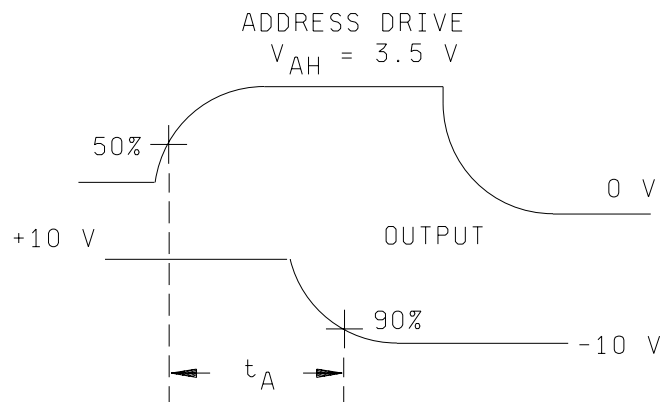
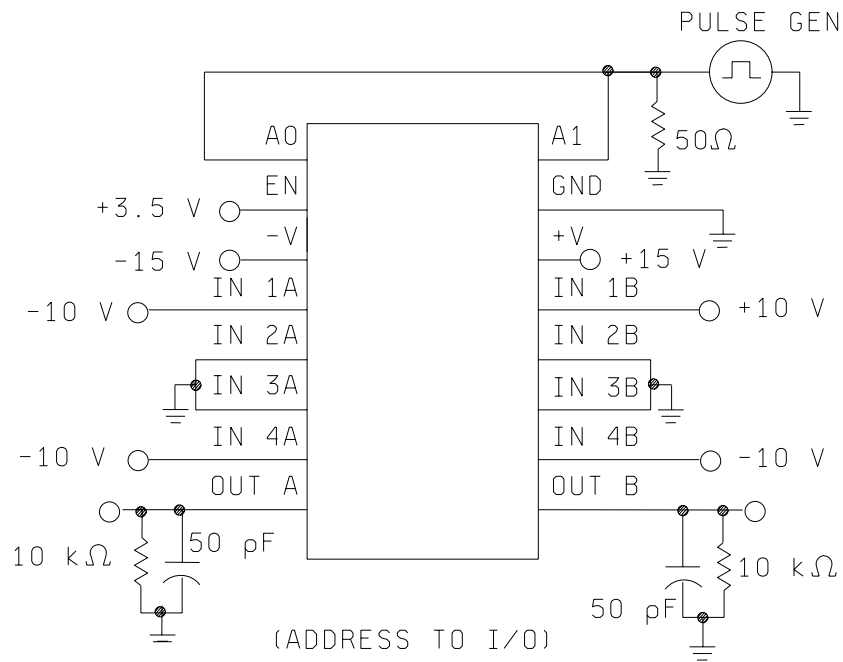


FIGURE 4. Switching times test circuits – continued.

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Device type 09

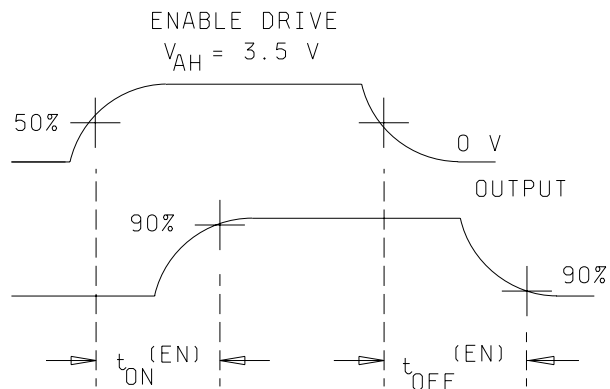
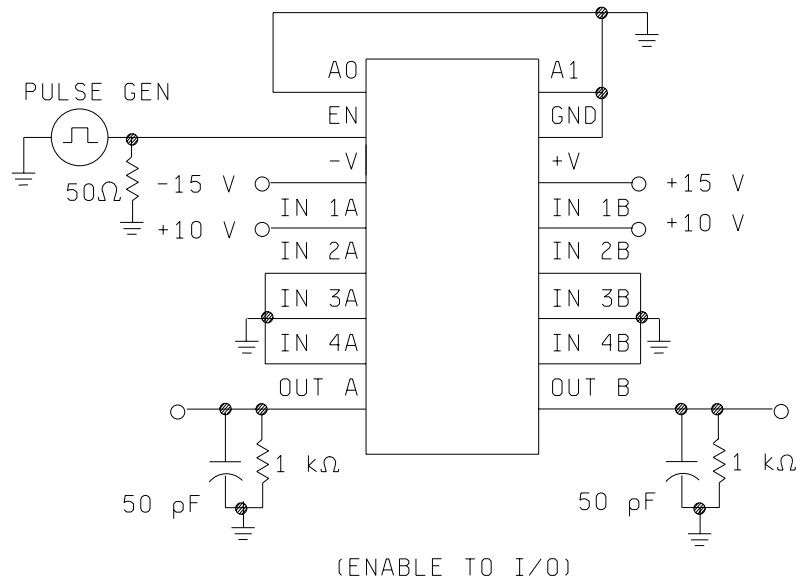


FIGURE 4. Switching times test circuits – continued.

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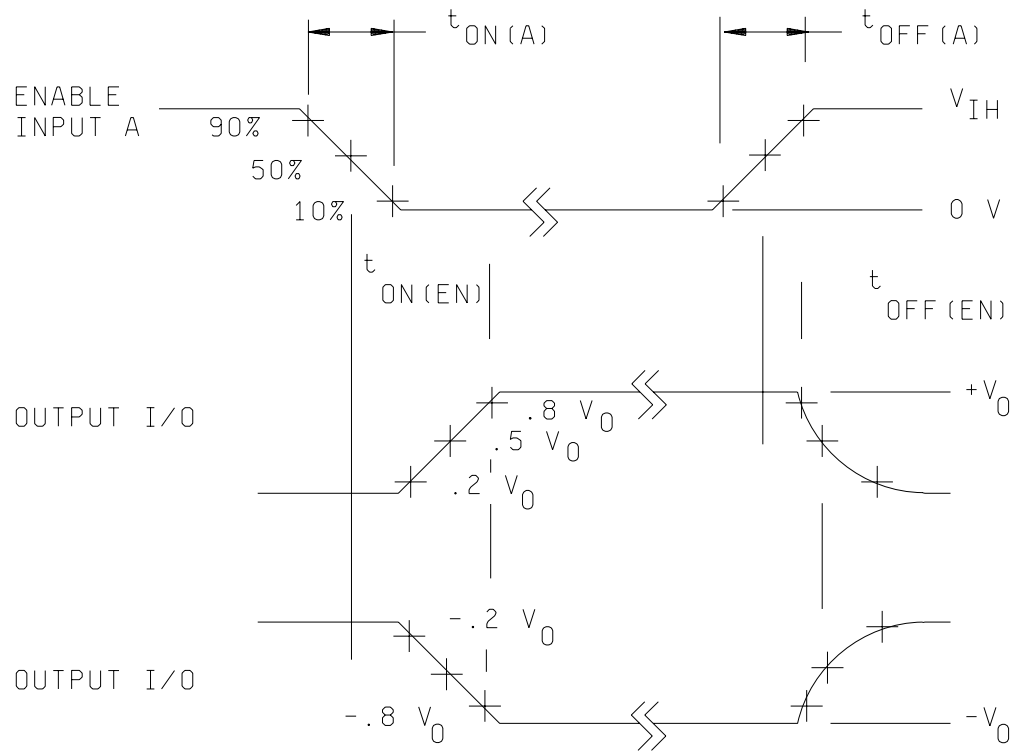
SIZE
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Device types 04, 05, and 06



INPUT PULSE REQUIREMENTS

$V_{GEN} = 3 V$

$t_{THL(1)} = t_{TLH(1)} \leq 20 ns$

FIGURE 4. Switching times test circuits – continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 capacitance measurements shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,9
Group A test requirements (method 5005)	1,2,3,4,7,9,10**,11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-09-13

Approved sources of supply for SMD 5962-85131 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /	Reference military specification
5962-85131013A	34371	HI4-546/883	
5962-8513101XA	34371	HI1-546/883	M38510/19002BXA
5962-85131023A	34371	HI4-547/883	
5962-8513102XA	34371	HI1-547/883	M38510/19004BXA
5962-85131032A	<u>3</u> /	HI4-549/883	
5962-8513103EA	34371	HI1-549/883	M38510/19006BEA
5962-8513104XA	<u>3</u> /	IH5116MJI	M38510/19002BXA
5962-8513105XA	<u>3</u> /	IH5216MJI	M38510/19004BXA
5962-85131062C	1ES66	MAX359MLP/883B	
5962-8513106EA	1ES66	MAX359MJE/883B	M38510/19006BEA
	<u>3</u> /	IH5208MJE	
5962-85131073A	34371	HI4-506/883	
5962-85131073C	1ES66	DG506AAZ/883B	
5962-8513107XA	34371	HI1-506/883	M38510/19001BXA
5962-85131083A	<u>3</u> /	HI4-507/883	
5962-85131083C	1ES66	DG507AAZ/883B	
5962-8513108XA	<u>3</u> /	HI1-507/883	M38510/19003BXA
5962-85131092A	34371	HI4-509/883	
5962-85131092C	1ES66	DG509AAZ/883B	
5962-8513109EA	<u>3</u> /	HI1-509/883	M38510/19008BEA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

STANDARD MICROCIRCUIT DRAWING BULLETIN - CONTINUED

Vendor CAGE
number

Vendor name
and address

34371

Intersil Corporation
1001 Murphy Ranch Road
Milpitas, CA 95035-6803
Point of contact: 1650 Robert J. Conlan Blvd.
Palm Bay, FL 32905

1ES66

Maxim Integrated Products
120 San Gabriel Drive
Sunnyvale, CA 94086-5125

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.