Data Sheet | July 18, 2007 | FN9143.5

ACPI Regulator/Controller for Dual Channel DDR Memory Systems

The ISL6537A provides a complete ACPI compliant power solution for up to 4 DIMM dual channel DDR/DDR2 Memory systems. Included are both a synchronous buck controller to supply V_{DDQ} during S0/S1 and S3 states. During S0/S1 state, a fully integrated sink-source regulator generates an accurate (V_{DDQ}/2) high current V_{TT} voltage without the need for a negative supply. A buffered version of the V_{DDQ}/2 reference is provided as V_{REF}. A second PWM controller, which requires external MOSFET drivers, is available for regulation of the GMCH Core voltage. An LDO controller is also integrated for the CPU V_{TT} termination voltage regulation and the DAC.

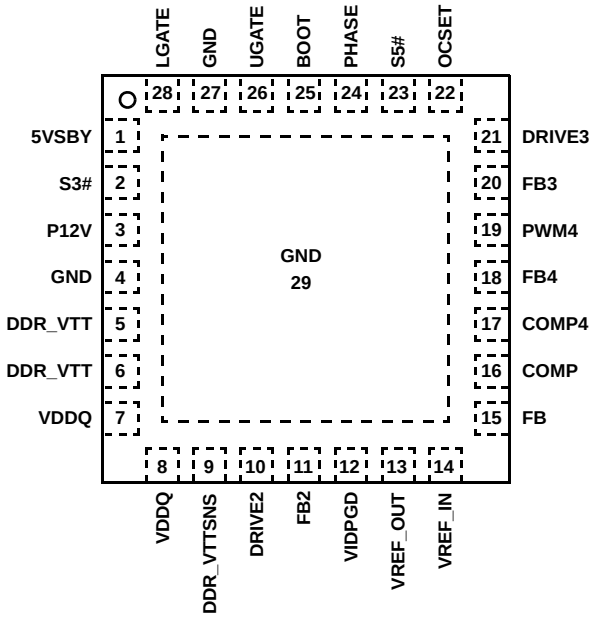
The switching PWM controller drives two N-Channel MOSFETs in a synchronous-rectified buck converter topology. The synchronous buck converter uses voltage-mode control with fast transient response. The switching regulator provides a maximum static regulation tolerance of ±2% over line, load, and temperature ranges. The output is user-adjustable by means of external resistors down to 0.8V.

An integrated soft-start feature brings all outputs into regulation in a controlled manner when returning to S0/S1 state from any sleep state. During S0 the VIDPGD signal indicates that the GMCH and CPU V_{TT} termination voltage is within spec and operational.

All outputs, except VDAC, have undervoltage protection. The switching regulator also has overvoltage and overcurrent protection. Thermal shutdown is integrated.

Pinout

ISL6537A (6X6 QFN)
TOP VIEW



Features

- Generates 5 Regulated Voltages
  - Synchronous Buck PWM Controller for DDR V_{DDQ}
  - 3A Integrated Sink/Source Linear Regulator with Accurate VDDQ/2 Divider Reference for DDR V_{TT}
  - PWM Regulator for GMCH Core
  - LDO Regulator for CPU/GMCH V_{TT} Termination
  - LDO Regulator for DAC
- ACPI Compliant Sleep State Control
- Glitch-Free Transitions During State Changes
- Integrated V_{REF} Buffer
- V_{DDQ} PWM Controller Drives Low Cost N-Channel MOSFETs
- 250kHz Constant Frequency Operation
  - Both PWM Controllers are Phase Shifted 180°
- Tight Output Voltage Regulation
  - All Outputs: ±2% Over Temperature
- Fully-Adjustable Outputs with Wide Voltage Range: Down to 0.8V Supports DDR and DDR2 Specifications
- Simple Single-Loop Voltage-Mode PWM Control Design
- Fast PWM Converter Transient Response
- Under and Overvoltage Monitoring
- OCP on the V_{DDQ} Switching Regulator
- Integrated Thermal Shutdown Protection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Single and Dual Channel DDR Memory Power Systems in ACPI Compliant PCs
- Graphics Cards - GPU and Memory Supplies
- ASIC Power Supplies
- Embedded Processor and I/O Supplies
- DSP Supplies

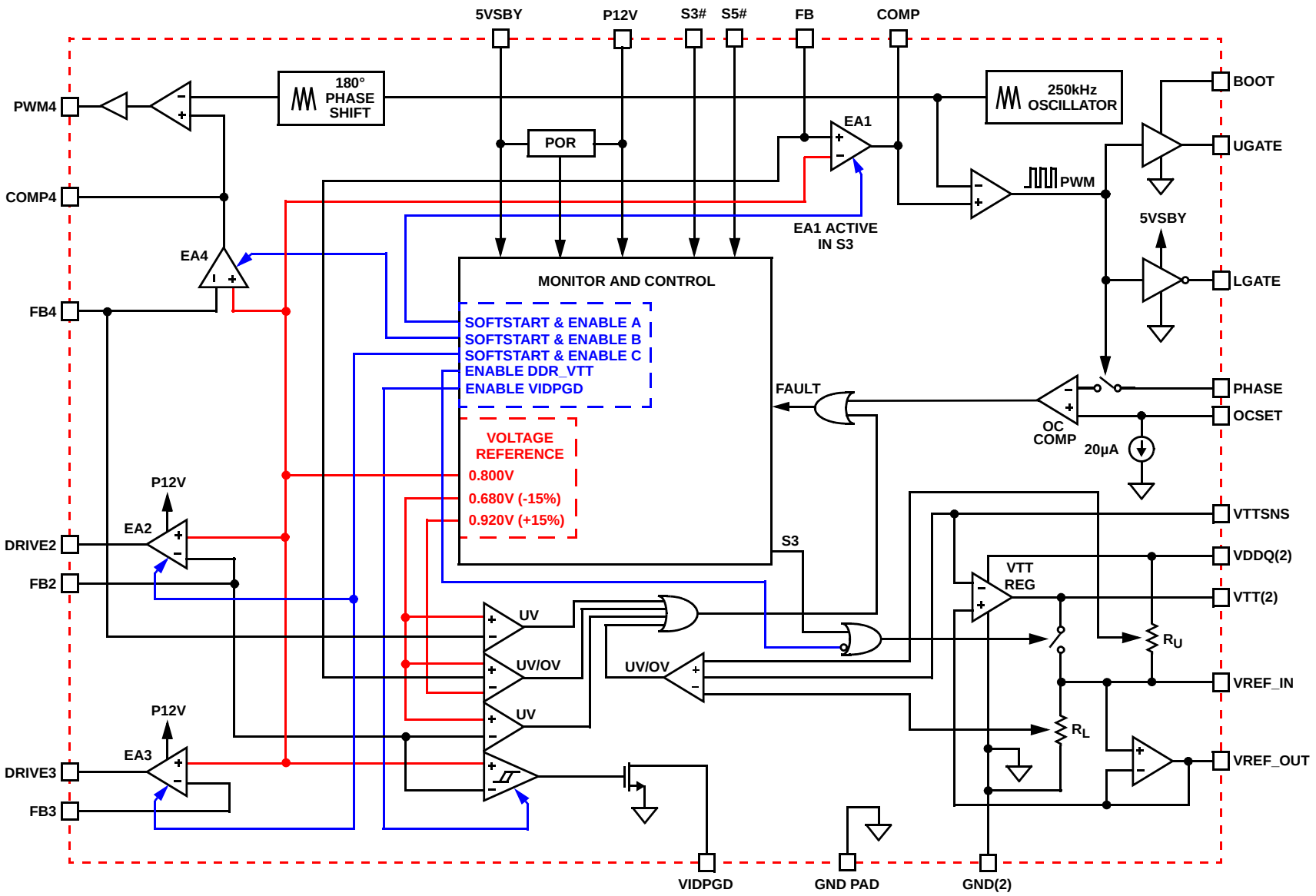
Ordering Information

PART NUMBER	PART MARKING	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6537ACR	ISL6537ACR	0 to +70	28 Ld 6x6 QFN	L28.6x6
ISL6537ACRZ (Note)	ISL6537ACRZ	0 to +70	28 Ld 6x6 QFN (Pb-free)	L28.6x6
ISL6537ACRZA (Note)	ISL6537ACRZ	0 to +70	28 Ld 6x6 QFN (Pb-free)	L28.6x6

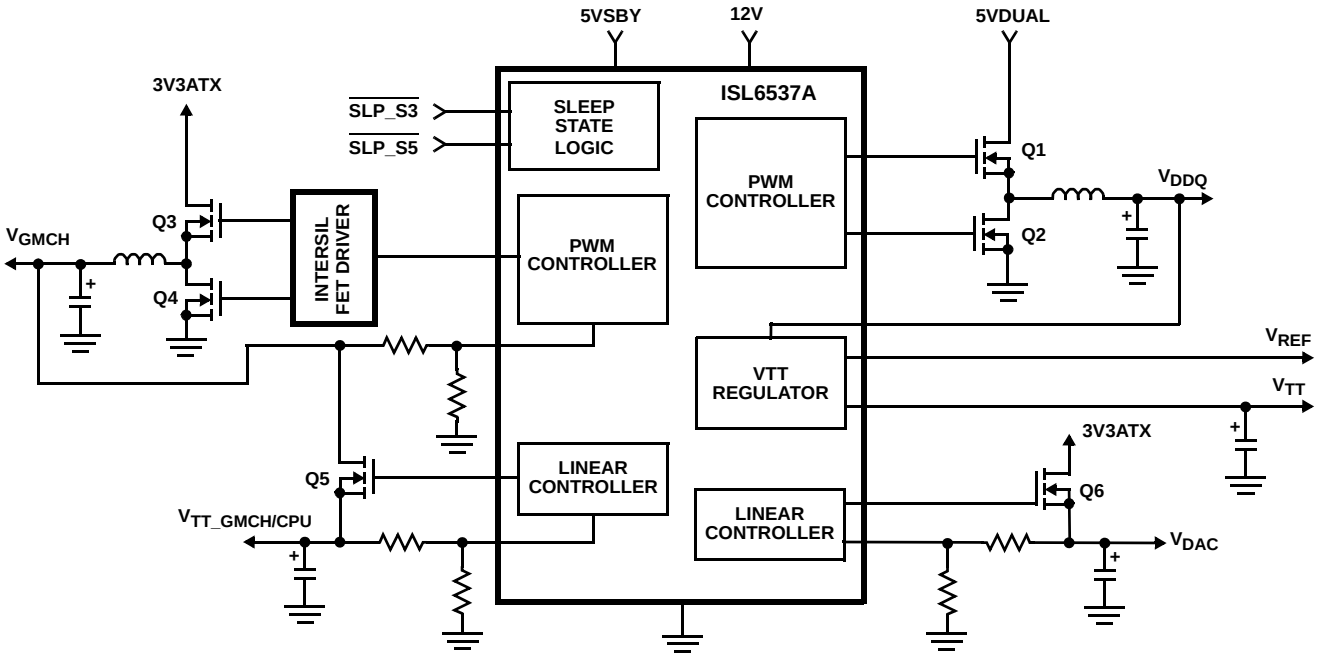
*Add “-T” suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

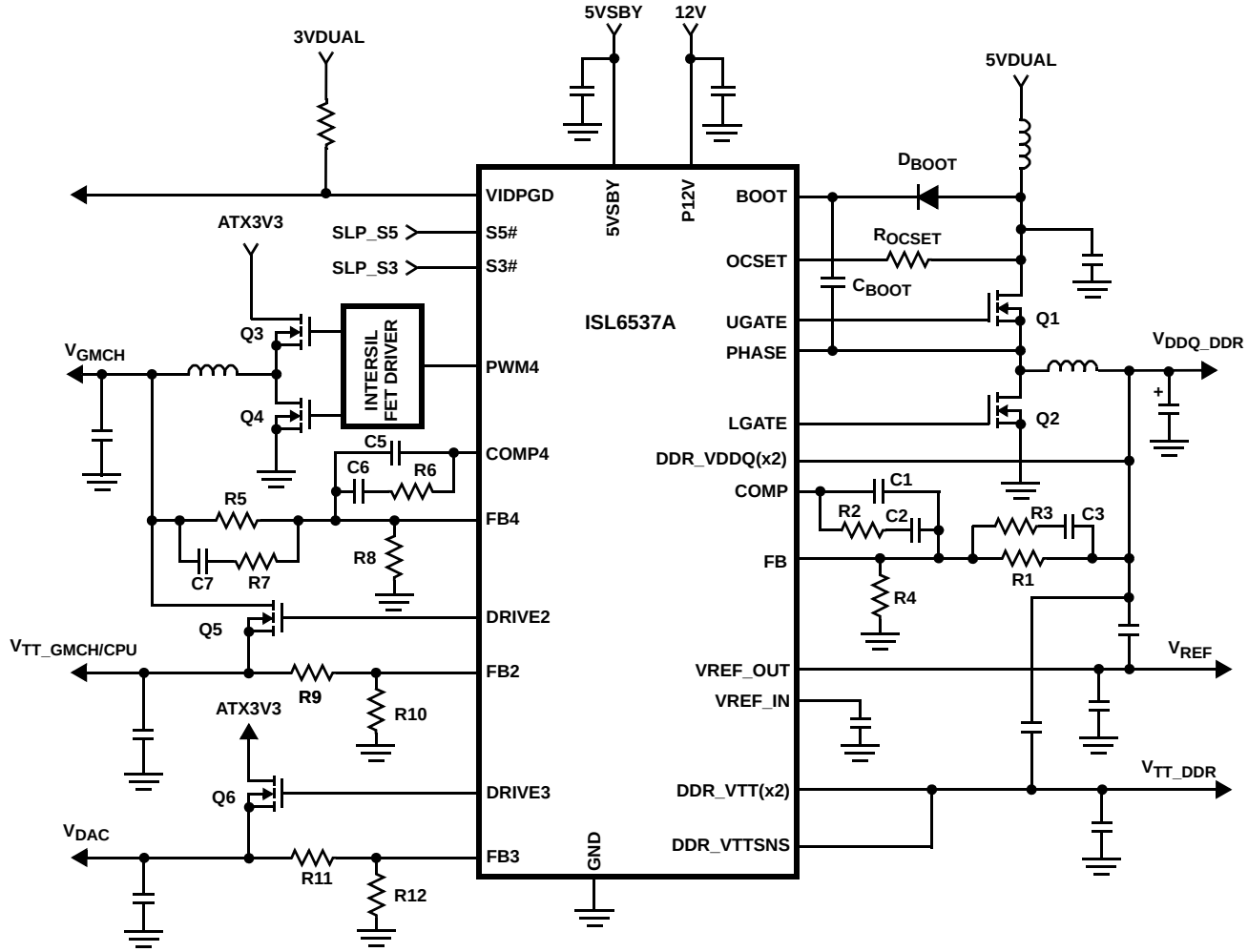
Block Diagram



Simplified Power System Diagram



Typical Application



Absolute Maximum Ratings

5VSBY . . . . . GND - 0.3V to +7V
P12V . . . . . GND - 0.3V to +14V
Absolute Boot Voltage, V_{BOOT} . . . . . +15.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE} . . . . . 7.0V (DC)
8.0V (<10ns Pulse Width, 10µJ)
All other Pins . . . . . GND - 0.3V to 5VCC + 0.3V
ESD Classification . . . . . Class 2

Recommended Operating Conditions

Supply Voltage on 5VSBY . . . . . +5V ±10%
Supply Voltage on P12V . . . . . +12V ±10%
Ambient Temperature Range . . . . . 0°C to +70°C
Junction Temperature Range . . . . . 0°C to +125°C

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package	32	5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams and Typical Application Schematics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5VSBY SUPPLY CURRENT						
Nominal Supply Current	I_{CC_S0}	S3# and S5# HIGH, UGATE/LGATE Open	5.5	7.0	8.0	mA
	I_{CC_S5}	S5# LOW, S3# Don’t Care, UGATE/LGATE Open	-	700	850	µA
POWER-ON RESET						
Rising 5VSBY POR Threshold			4.10	-	4.45	V
Falling 5VSBY POR Threshold			3.60	-	3.95	V
Rising P12V POR Threshold			10.0	-	10.5	V
Falling P12V POR Threshold			8.80	-	9.75	V
OSCILLATOR AND SOFT-START						
PWM Frequency	f_{OSC}		220	250	280	kHz
Ramp Amplitude	ΔV_{OSC}		-	1.5	-	V
Soft-Start Interval	t_{SS}		6.5	8.2	9.5	ms
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}		-	0.800	-	V
System Accuracy			-2.0	-	+2.0	%
V_{DDQ} AND V_{GMCH} PWM CONTROLLER ERROR AMPLIFIERS						
DC Gain		(Note 3)	-	80	-	dB
Gain-Bandwidth Product	GBWP	(Note 3)	15	-	-	MHz
Slew Rate	SR	(Note 3)	-	6	-	V/µs
CONTROL I/O (S3#, S5#)						
LOW Level Input Threshold			0.75	-	-	V
HIGH Level Input Threshold			-	-	2.2	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams and Typical Application Schematics **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM CONTROLLER GATE DRIVERS						
UGATE and LGATE Source	I_{GATE}		-	-0.8	-	A
UGATE and LGATE Sink	I_{GATE}		-	0.8	-	A
VTT REGULATOR						
Upper Divider Impedance	R_U		-	2.5	-	kΩ
Lower Divider Impedance	R_L		-	2.5	-	kΩ
VREF_OUT Buffer Source Current	I_{VREF_OUT}		-	-	2	mA
Maximum V_{TT} Load Current	I_{VTT_MAX}	Periodic load applied with 30% duty cycle and 10ms period using ISL6537A_6506EVAL1 evaluation board (see Application Note AN1124)	-3	-	3	A
LINEAR REGULATORS						
DC Gain		(Note 3)	-	80	-	dB
Gain Bandwidth Product	GBWP	(Note 3)	15	-	-	MHz
Slew Rate	SR	(Note 3)	-	6	-	V/µs
DRIVEn High Output Voltage		DRIVEn Unloaded	9.75	10.0	-	V
DRIVEn Low Output Voltage			-	0.16	0.50	V
DRIVEn High Output Source Current		V_{FB} = 770mV, V_{DRIVEn} = 0V	-	1.7	-	mA
DRIVEn Low Output Sink Current		V_{FB} = 830mV, V_{DRIVEn} = 10V	-	1.20	-	mA
VIDPGD						
$V_{TT\_GMCH/CPU}$ Rising Threshold		S0	.725	.740	-	V
$V_{TT\_GMCH/CPU}$ Falling Threshold		S0	-	0.700	0.715	V
PROTECTION						
OCSET Current Source	I_{OCSET}		18	20	22	µA
V_{TT_DDR} Current Limit		(Note 3)	-3.3	-	3.3	A
V_{DDQ} OV Level	V_{FB}/V_{REF}	S0/S3	-	115	-	%
V_{DDQ} UV Level	V_{FB}/V_{REF}	S0/S3	-	75	-	%
V_{TT_DDR} OV Level	V_{TT}/V_{VREF_IN}	S0	-	115	-	%
V_{TT_DDR} UV Level	V_{TT}/V_{VREF_IN}	S0	-	85	-	%
V_{GMCH} UV Level	V_{FB4}/V_{REF}	S0	-	75	-	%
$V_{TT\_GMCH/CPU}$ UV Level	V_{FB2}/V_{REF}	S0	-	75	-	%
Thermal Shutdown Limit	T_{SD}	(Note 3)	-	140	-	°C

NOTE:

3. Limits should be considered typical and are not production tested

Functional Pin Description

5VSBY (Pin 1)

5VSBY is the bias supply of the ISL6537A. It is typically connected to the 5V standby rail of an ATX power supply. During S4/S5 sleep states the ISL6537A enters a reduced power mode and draws less than 1mA (I_{CC_S5}) from the 5VSBY supply. The supply to 5VSBY should be locally bypassed using a 0.1µF capacitor.

P12V (Pin 3)

The V_{TT} regulation circuit and the Linear Drivers are powered by P12V. P12V is not required during S3/S4/S5 operation. P12V is typically connected to the +12V rail of an ATX power supply.

GND (Pins 4, 27, 29)

The GND terminals of the ISL6537A provide the return path for the V_{TT} LDO, and switching MOSFET gate drivers. High

ground currents are conducted directly through the exposed paddle of the QFN package which must be electrically connected to the ground plane through a path as low in inductance as possible.

UGATE (Pin 26)

Connect this pin to the upper MOSFET's gate. This pin provides the PWM-controlled gate drive for the upper MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. Do not insert any circuitry between this pin and the gate of the upper MOSFET, as it may interfere with the internal adaptive shoot-through protection circuitry and render it ineffective.

LGATE (Pin 28)

Connect this pin to the lower MOSFET's gate. This pin provides the PWM-controlled gate drive for the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off. Do not insert any circuitry between this pin and the gate of the lower MOSFET, as it may interfere with the internal adaptive shoot-through protection circuitry and render it ineffective.

FB (Pin 15) and COMP (Pin 16)

The V_{DDQ} switching regulator employs a single voltage control loop. FB is the negative input to the voltage loop error amplifier. The V_{DDQ} output voltage is set by an external resistor divider connected to FB. With a properly selected divider, V_{DDQ} can be set to any voltage between the power rail (reduced by converter losses) and the 0.8V reference. Loop compensation is achieved by connecting an AC network across COMP and FB.

The FB pin is also monitored for under and overvoltage events.

PHASE (Pin 24)

Connect this pin to the upper MOSFET's source. This pin is used to monitor the voltage drop across the upper MOSFET for overcurrent protection.

OCSET (Pin 22)

Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 20µA current source (I_{OCSET}), and the upper MOSFET on-resistance ($r_{DS(ON)}$) set the converter overcurrent (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} x R_{OCSET}}{r_{DS(ON)}} \quad \text{(EQ. 1)}$$

An overcurrent trip cycles the soft-start function.

VDDQ (Pins 7, 8)

The VDDQ pins should be connected externally together to the regulated V_{DDQ} output. During S0/S1 states, the VDDQ pins serve as inputs to the V_{TT} regulator and to the V_{TT} Reference precision divider.

DDR_VTT (Pins 5, 6)

The DDR_VTT pins should be connected externally together. During S0/S1 states, the DDR_VTT pins serve as the outputs of the V_{TT} linear regulator. During S3 state, the V_{TT} regulator is disabled.

DDR_VTTSNS (Pin 9)

VTTSNS is used as the feedback for control of the V_{TT} linear regulator. Connect this pin to the V_{TT} output at the physical point of desired regulation.

VREF_OUT (Pin 13)

VREF_OUT is a buffered version of V_{TT} and also acts as the reference voltage for the V_{TT} linear regulator. It is recommended that a minimum capacitance of 0.1µF is connected between V_{DDQ} and VREF_OUT and also between VREF_OUT and ground for proper operation.

VREF_IN (Pin 14)

A capacitor, C_{SS}, connected between VREF_IN and ground is required. This capacitor and the parallel combination of the Upper and Lower Divider Impedance ($R_U||R_L$), sets the time constant for the start up ramp when transitioning from S3/S4/S5 to S0/S1/S2.

The minimum value for C_{SS} can be found through the following equation:

$$C_{SS} > \frac{C_{VTTOUT} \cdot V_{DDQ}}{10 \cdot 2A \cdot R_U \| R_L} \quad \text{(EQ. 2)}$$

The calculated capacitance, C_{SS}, will charge the output capacitor bank on the V_{TT} rail in a controlled manner without reaching the current limit of the V_{TT} LDO.

BOOT (Pin 25)

This pin provides ground referenced bias voltage to the upper MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive a logic-level N-channel MOSFET.

PWM4 (Pin 19)

This pin provides the PWM output for the GMCH core switching regulator. Connect this pin to the PWM input of an Intersil MOSFET driver.

FB4 (Pin 19) and COMP4 (Pin 17)

The GMCH core switching regulator employs a single voltage control loop. FB4 is the negative input to the voltage loop error amplifier. The GMCH core output voltage is set by an external resistor divider connected to FB4. With a properly selected divider, V_{GMCH} can be set to any voltage between the power rail (reduced by converter losses) and the 0.8V reference. Loop compensation is achieved by connecting an AC network across COMP4 and FB4.

The FB4 pin is also monitored for undervoltage events.

FB2 (Pin 18)

Connect the output of the $V_{TT\_GMCH/CPU}$ linear regulator to this pin through a properly sized resistor divider. The voltage at this pin is regulated to 0.8V. This pin is monitored for undervoltage events.

DRIVE2 (Pin 10)

This pin provides the gate voltage for the $V_{TT\_GMCH/CPU}$ linear regulator pass transistor. Connect this pin to the gate terminal of an external N-Channel MOSFET transistor.

FB3 (Pin 18)

Connect the output of the DAC linear regulator to this pin through a properly sized resistor divider. The voltage at this pin is regulated to 0.8V.

DRIVE3 (Pin 10)

This pin provides the gate voltage for the DAC linear regulator pass transistor. Connect this pin to the gate terminal of an external N-Channel MOSFET transistor.

VIDPGD (Pin 12)

The VIDPGD pin is an open-drain logic output that changes to a logic low if the $V_{TT\_GMCH/CPU}$ linear regulator is out of regulation in S0/S1/S2 state. VIDPGD will always be low in any state other than S0/S1/S2.

SLP_S5# (Pin 23)

This pin accepts the SLP_S5# sleep state signal.

SLP_S3# (Pin 2)

This pin accepts the SLP_S3# sleep state signal.

Functional Description

Overview

The ISL6537A provides complete control, drive, protection and ACPI compliance for regulator powering DDR memory systems and the GMCH core and GMCH/CPU termination rails. It is primarily designed for computer applications powered from an ATX power supply.

A 250kHz Synchronous Buck Regulator with a precision 0.8V reference provides the proper Core voltage to the system memory of the computer. An internal LDO regulator with the ability to both sink and source current and an externally available buffered reference that tracks the V_{DDQ} output by 50% provides the V_{TT} termination voltage.

A second 250kHz PWM Buck regulator, which requires an external MOSFET driver, provides the GMCH core voltage. This PWM regulator is +180° out of phase with the PWM regulator used for the Memory core. Two additional LDO controllers are included, one for the regulation of the GMCH/CPU termination rail and the second for the DAC.

ACPI compliance is realized through the SLP_S3 and SLP_S5 sleep signals and through monitoring of the 12V ATX bus.

Initialization

The ISL6537A automatically initializes upon receipt of input power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input bias supply voltages. The POR monitors the bias voltage at the 5VSBY and P12V pins. The POR function initiates soft-start operation after the bias supply voltages exceed their POR thresholds.

ACPI State Transitions

Figure 1 shows how the individual regulators are controlled during all state transitions. All references to timing in this section are in reference to Figure 1.

Cold Start (S4/S5 to S0 Transition)

At the onset of a mechanical start, time t_0 in Figure 1, the ISL6537A receives its bias voltage from the 5V Standby bus (5VSBY). Once the 5VSBY rail has exceeded the POR threshold, the ISL6537A will remain in an internal S5 state until both the SLP_S3 and SLP_S5 signal have transitioned high and the 12V POR threshold has been exceeded by the +12V rail from the ATX, which occurs at time t_1.

Once all of these conditions are met, the PWM error amplifiers will first be reset by internally shorting the COMP pins to the respective FB pins. This reset lasts for three soft-start cycles, which is typically 24ms (one soft-start cycle is typically 8.2ms). The digital soft-start sequence will then begin. Each regulator is enabled and soft-started according to a preset sequence.

At time t_2, the 3 soft-start cycle reset has ended and the V_{DDQ_DDR} rail is digitally soft-started.

The digital soft-start for both PWM regulators is accomplished by clamping the error amplifier reference input to a level proportional to the internal digital soft-start voltage. As the soft-start voltage slews up, the PWM comparator generates PHASE pulses of increasing width that charge the output capacitor(s). This method provides a rapid and controlled output voltage rise.

The linear regulators, with the exception of the internal V_{TT_DDR} LDO, are soft-started in a similar manner. The error amplifier reference is clamped to the internal digital soft-start voltage. As the soft-start voltage ramps up, the respective DRIVE pin voltages increase, thus enhancing the N-MOSFETs and charging the output capacitors in a controlled manner.

At time t_3, the V_{DDQ_DDR} rail is in regulation and the V_{GMCH} rail is soft-started. At time t_4, the V_{GMCH} rail is in regulation and the $V_{TT\_GMCH/CPU}$ and the DAC linear regulators are soft-started. At time t_5, the $V_{TT\_GMCH/CPU}$ rail and DAC rails are in regulation and the V_{TT_DDR} internal regulator is soft-started.

The V_{TT_DDR} LDO soft-starts in a manner unlike the other regulators. When the V_{TT_DDR} regulator is disabled, the reference is internally shorted to the V_{TT_DDR} output. This

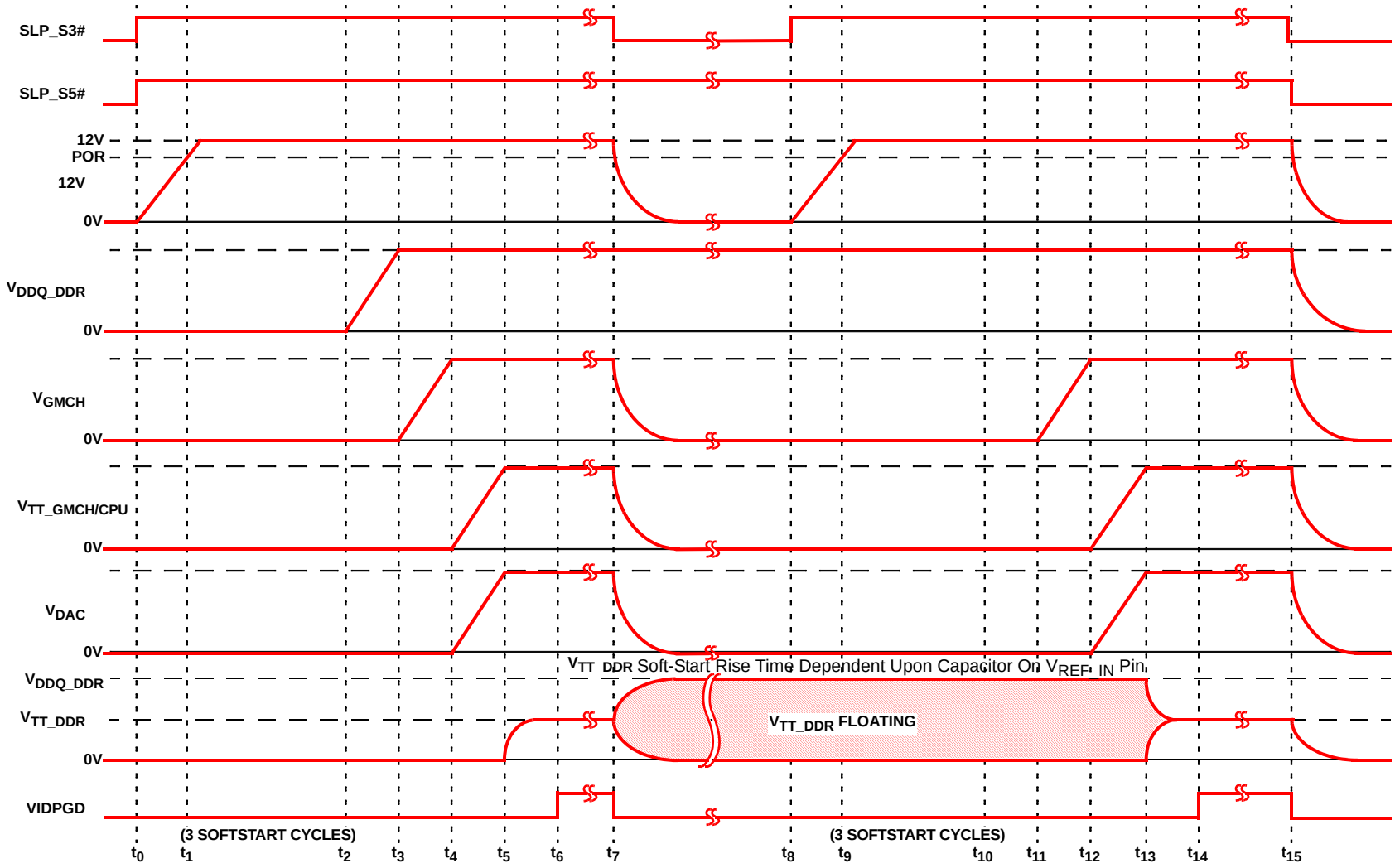


FIGURE 1. ISL6537A TIMING DIAGRAM

allows the termination voltage to float during the S3 sleep state. When the ISL6537A enables the V_{TT_DDR} regulator or enters S0 state from a sleep state, this short is released and the internal divide down resistors which set the V_{TT_DDR} voltage to 50% of V_{DDQ_DDR} will provide a controlled voltage rise on the capacitor that is tied to the VREF_IN pin. The voltage on this capacitor is the reference for the V_{TT_DDR} regulator and the output will track it as it settles to 50% of the V_{DDQ} voltage. The combination of the internal resistors and the V_{REF_IN} capacitor will determine the rise time of the V_{TT_DDR} regulator (see the Functional Pin Description section for proper sizing of the VREF_IN capacitor).

At time t_6, a full soft-start cycle has passed from the time that the V_{TT_DDR} regulator was enabled. At this time the VIDPGD comparator is enabled. Once enabled if the $V_{TT\_GMCH/CPU}$ output is within regulation, the VIDPGD pin will be forced to a high impedance state.

Active to Sleep (S0 to S3 Transition)

When SLP_S3 goes LOW with SLP_S5 still HIGH, the ISL6537A will disable all the regulators except for the V_{DDQ} regulator, which is continually supplied by the 5VDUAL rail. VIDPGD will also transition LOW. When V_{TT} is disabled, the internal reference for the V_{TT} regulator is internally shorted to the V_{TT} rail. This allows the V_{TT} rail to float. When floating, the voltage on the V_{TT} rail will depend on the leakage characteristics of the memory and MCH I/O pins. It is important to note that the V_{TT} rail may not bleed down to 0V. Figure 1 shows how the individual regulators are affected by the S3 state at time t_7.

Sleep to Active (S3 to S0 Transition)

When SLP_S3 transitions from LOW to HIGH with SLP_S5 held HIGH and after the 12V rail exceeds POR, the ISL6537A will initiate the soft-start sequence. This sequence is very similar to the mechanical start soft-start sequencing. The transition from S3 to S0 is represented in Figure 1 between times t_8 and t_{14}.

At time t_8, the SLP_S3 signal transitions HIGH. This enables the ATX, which brings up the 12V rail. At time t_9, the 12V rail has exceeded the POR threshold and the ISL6537A enters a reset mode that lasts for 3 soft-start cycles. At time t_{10}, the 3 soft-start cycle reset is ended and the individual regulators are enabled and soft-started in the same sequence as the mechanical cold start sequence, with the exception that the V_{DDQ} regulator is already enabled and in regulation.

Active to Shutdown (S0 to S5 Transition)

When the system transitions from active, S0, state to shutdown, S4/S5, state, the ISL6537A IC disables all regulators and forces the VIDPGD pin LOW. This transition is represented on Figure 1 at time t_{15}.

Fault Protection

The ISL6537A monitors the V_{DDQ} regulator for under and overvoltage events. The V_{DDQ} regulator also has overcurrent protection. The internal V_{TT_DDR} LDO regulator is monitored for under and overvoltage events. All other regulators, with the exception of the DAC LDO, are monitored for undervoltage events.

An overvoltage event on either the V_{DDQ} or V_{TT_DDR} regulator will cause an immediate shutdown of all regulators. This can only be cleared by toggling the SLP_S5 signal such that the system enters the S5 sleep state and then transitions back to the active, S0, state.

If a regulator experiences any other fault condition (an undervoltage or an overcurrent on V_{DDQ}), then that regulator, and only that regulator, will be disabled and an internal fault counter will be incremented by 1. If the disabled regulator is used as the input for another regulator, then that cascoded regulator will also experience a fault condition due to a loss of input. The cascoded regulator will be disabled and the fault counter incremented by 1.

At every fault occurrence, the internal fault counter is incremented by 1 and an internal Fault Reset Counter is cleared to zero. The Fault Reset Counter will increment once for every clock cycle (1 clock cycle is typically 1/250kHz, or 4µs). If the Fault Reset Counter reaches a count of 16384 before another fault occurs, then the Fault Counter is cleared to 0. If a fault occurs prior to the Fault Reset Counter reaching a count of 16384, then the Fault Reset Counter is set back to zero.

The ISL6537A will immediately shut down when the Fault Counter reaches a count of 4 when the system is restarting from an S5 state into the active, or S0, state. The ISL6537A will immediately shut down when the Fault Counter reaches a count of 5 at any other time.

The 16384 counts that are required to reset the Fault Reset Counter represent 8 soft-start cycles, as one soft-start cycle is 2048 clock cycles. This allows the ISL6537A to attempt at least one full soft-start sequence to restart the faulted regulators.

When attempting to restart a faulted regulator, the ISL6537A will follow the preset start up sequencing. If a regulator is already in regulation, then it will not be affected by the start up sequencing.

V_{DDQ} Overcurrent Protection

The overcurrent function protects the switching converter from a shorted output by using the upper MOSFET on-resistance, $r_{DS(ON)}$, to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The overcurrent function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the overcurrent trip level (see Typical Application

diagrams on page 4). An internal 20µA (typical) current sink develops a voltage across R_{OCSET} that is referenced to the converter input voltage. When the voltage across the upper MOSFET (also referenced to the converter input voltage) exceeds the voltage across R_{OCSET}, the overcurrent function initiates a soft-start sequence. The initiation of soft-start may affect other regulators. The V_{TT_DDR} regulator is directly affected as it receives its reference and input from V_{DDQ}.

The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}} \quad \text{(EQ. 3)}$$

where I_{OCSET} is the internal OCSET current source (20µA typical). The OC trip point varies mainly due to the MOSFET $r_{DS(ON)}$ variations. To avoid overcurrent tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + \frac{(\Delta I)}{2}$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled ‘Output Inductor Selection’.

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Thermal Protection (S0/S3 State)

If the ISL6537A IC junction temperature reaches a nominal temperature of +140°C, all regulators will be disabled. The ISL6537A will not re-enable the outputs until the junction temperature drops below +110°C and either the bias voltage is toggled in order to initiate a POR or the SLP_S5 signal is forced LOW and then back to HIGH.

Shoot-Through Protection

A shoot-through condition occurs when both the upper and lower MOSFETs are turned on simultaneously, effectively shorting the input voltage to ground. To protect from a shoot-through condition, the ISL6537A incorporates specialized circuitry on the V_{DDQ} regulator which insures that complementary MOSFETs are not ON simultaneously.

The adaptive shoot-through protection utilized by the V_{DDQ} regulator looks at the lower gate drive pin, LGATE, and the upper gate drive pin, UGATE, to determine whether a MOSFET is ON or OFF. If the voltage from UGATE or from LGATE to GND is less than 0.8V, then the respective MOSFET is defined as being OFF and the other MOSFET is allowed to turned ON. This method allows the V_{DDQ} regulator to both source and sink current.

Since the voltage of the MOSFET gates are being measured to determine the state of the MOSFET, the designer is encouraged to consider the repercussions of introducing external components between the gate drivers and their respective MOSFET gates before actually implementing such measures. Doing so may interfere with the shoot-through protection.

Application Guidelines

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently at 250kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes.

As an example, consider the turn-off transition of the control MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the lower MOSFET. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimizes the magnitude of voltage spikes.

There are two sets of critical components in the ISL6537A switching converter. The switching components are the most critical because they switch large amounts of energy, and therefore tend to generate large amounts of noise. Next are the small signal components which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 2 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the GATE pins to the MOSFET gates should be kept short and wide enough to easily handle the 1A of drive current.

In order to dissipate heat generated by the internal V_{TT} LDO, the ground pad, pin 29, should be connected to the internal ground plane through at least four vias. This allows

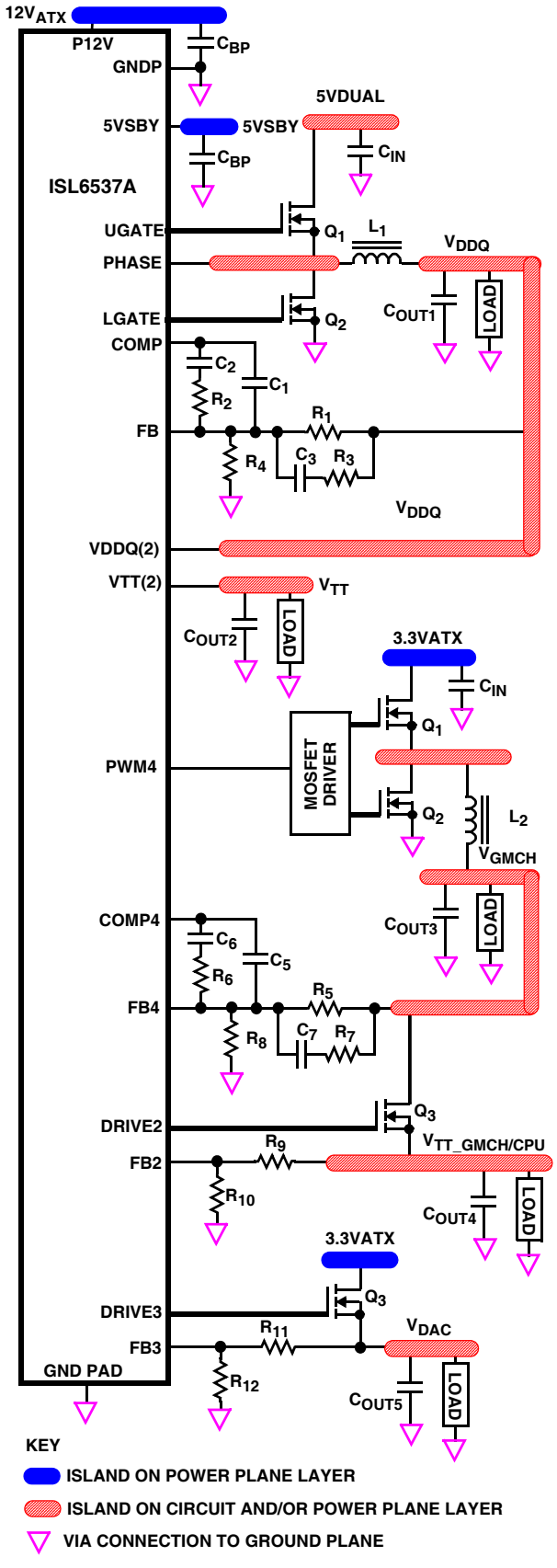


FIGURE 2. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

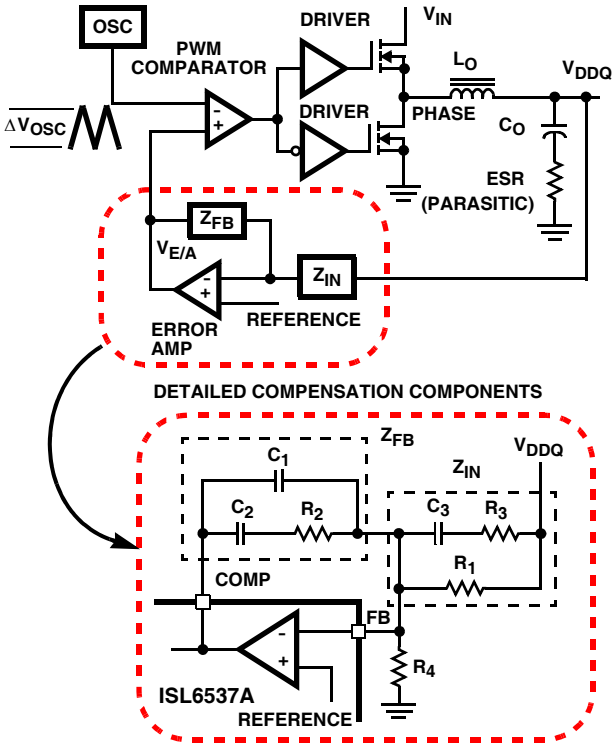
the heat to move away from the IC and also ties the pad to the ground plane through a low impedance path.

The switching components should be placed close to the ISL6537A first. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper and lower MOSFETs and the load.

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors should be located as close as possible to the FB pin with vias tied straight to the ground plane as required.

Feedback Compensation - PWM Buck Converters

Figure 3 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).



$$V_{DDQ} = 0.8 \times \left(1 + \frac{R_1}{R_4}\right)$$

FIGURE 3. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN AND OUTPUT VOLTAGE SELECTION

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(EQ. 4)}$$

The compensation network consists of the error amplifier (internal to the ISL6537A) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 3. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R_2/R_1) for desired converter bandwidth.
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC}).
3. Place 2ND Zero at Filter's Double Pole.
4. Place 1ST Pole at the ESR Zero.
5. Place 2ND Pole at Half the Switching Frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3} \quad \text{(EQ. 5)}$$

Figure 4 shows an asymptotic plot of the DC/DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 4. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the graph of Figure 4 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

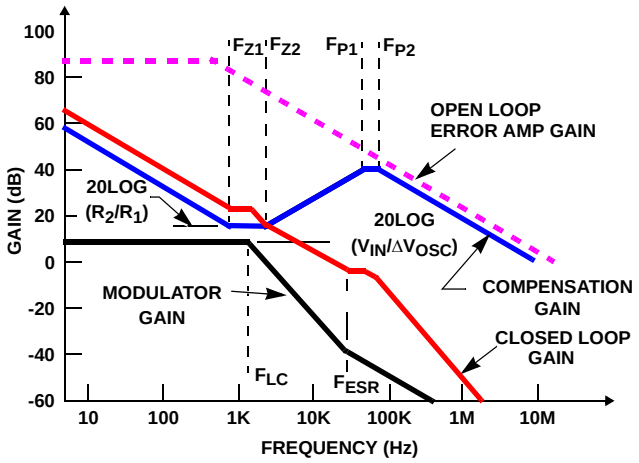


FIGURE 4. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Output Voltage Selection

The output voltage of all the external voltage regulators can be programmed to any level between their individual input voltage and the internal reference, 0.8V. An external resistor divider is used to scale the output voltage relative to the reference voltage and feed it back to the inverting input of the error amplifier, refer to the Typical Application on page 4.

The output voltage programming resistor will depend on the value chosen for the feedback resistor and the desired output voltage of the particular regulator.

$$R4 = \frac{R1 \times 0.8V}{V_{DDQ} - 0.8V}$$

$$R8 = \frac{R5 \times 0.8V}{V_{GMCH} - 0.8V} \quad \text{(EQ. 6)}$$

$$R10 = \frac{R9 \times 0.8V}{V_{TT\_GMCH/CPU} - 0.8V}$$

$$R12 = \frac{R11 \times 0.8V}{V_{DAC} - 0.8V}$$

If the output voltage desired is 0.8V, simply route the output voltage back to the respective FB pin through the feedback resistor and do not populate the output voltage programming resistor.

The output voltage for the internal V_{TT_DDR} linear regulator is set internal to the ISL6537A to track the V_{DDQ} voltage by 50%. There is no need for external programming resistors.

Component Selection Guidelines

Output Capacitor Selection - PWM Buck Converter

An output capacitor is required to filter the inductor current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

DDR memory systems are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Capacitor Selection - LDO Regulators

The output capacitors used in LDO regulators are used to provide dynamic load current. The amount of capacitance and type of capacitor should be chosen with this criteria in mind.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 7)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6537A will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 8)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection - PWM Buck Converter

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of upper MOSFET and the source of lower MOSFET.

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a conservative guideline. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current required by the regulator may be closely approximated through the following equation:

$$I_{RMS_{MAX}} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left({I_{OUT_{MAX}}}^2 + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_s} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \right)}$$

(EQ. 9)

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

MOSFET Selection - PWM Buck Converter

The ISL6537A requires 2 N-Channel power MOSFETs for switching power and a third MOSFET to block backfeed from V_{DDQ} to the Input in S3 Mode. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor. The switching losses seen when sourcing current will be different from the switching losses seen when sinking current. When sourcing current, the upper MOSFET realizes most of the switching losses. The lower switch realizes most of the switching losses when the converter is sinking current (see the equations below). These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the upper and lower MOSFET's body diode. The gate-charge losses are dissipated in part by the ISL6537A and do not significantly heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Approximate Losses while Sourcing current

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_s$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

Approximate Losses while Sinking current (EQ. 10)

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D) + \frac{1}{2} \cdot Io \times V_{IN} \times t_{SW} \times f_s$$

Where: D is the duty cycle = V_{OUT}/V_{IN},
t_{SW} is the combined switch ON and OFF time, and
f_s is the switching frequency.

MOSFET Selection - LDO

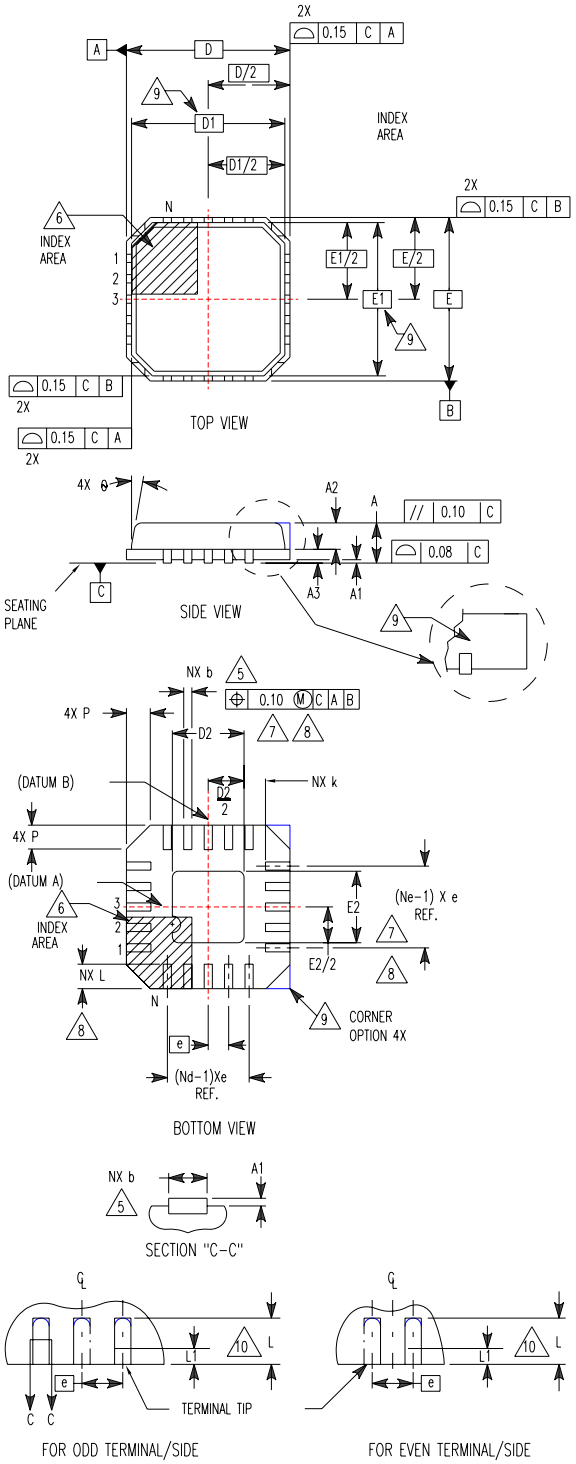
The main criteria for selection of the linear regulator pass transistor is package selection for efficient removal of heat. Select a package and heatsink that maintains the junction temperature below the rating with a maximum expected ambient temperature.

The power dissipated in the linear regulator is:

$$P_{LINEAR} \cong I_O \times (V_{IN} - V_{OUT}) \quad \text{(EQ. 11)}$$

where I_O is the maximum output current and V_{OUT} is the nominal output voltage of the linear regulator.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L28.6x6

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.95	4.10	4.25	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.95	4.10	4.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		28		2
Nd		7		3
Ne		7		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.