Data Sheet | September 2, 2008 | FN6762.0

ZVS Full Bridge PWM Controller

The ISL6551IREC is a zero voltage switching (ZVS) full bridge PWM controller designed for isolated power systems. This part implements a unique control algorithm for fixed frequency ZVS current mode control, yielding high efficiency with low EMI. The two lower drivers are PWM-controlled on the trailing edge and employ resonant delay while the two upper drivers are driven at a fixed 50% duty cycle.

This IC integrates many features in a 28 lead 6mmx6mm^2 QFN package to yield a complete and sophisticated power supply solution. Control features include programmable soft-start for controlled start-up, programmable resonant delay for zero voltage switching, programmable leading edge blanking to prevent false triggering of the PWM comparator due to the leading edge spike of the current ramp, adjustable ramp for slope compensation, drive signals for implementing synchronous rectification in high output current, ultra high efficiency applications, and current share support for paralleling up to 10 units, which helps achieve higher reliability and availability as well as better thermal management. Protective features include adjustable cycle-by-cycle peak current limiting for overcurrent protection, fast short-circuit protection (in hiccup mode), a latching shutdown input to turn off the IC completely on output overvoltage conditions or other extreme and undesirable faults, a non-latching enable input to accept an enable command when monitoring the input voltage and thermal condition of a converter, and VDD undervoltage lockout with hysteresis. Additionally, the ISL6551IREC includes high current high-side and low-side totem-pole drivers to avoid additional external drivers for moderate gate capacitance (up to 1.6nF at 1MHz) applications, an uncommitted high bandwidth (10MHz) error amplifier for feedback loop compensation, a precision bandgap reference with ±1.5% or ±1% tolerance over recommended operating conditions, and a ±5% “in regulation” monitor.

In addition to the ISL6551IREC, other external elements such as transformers, pulse transformers, capacitors, inductors and Schottky or synchronous rectifiers are required for a complete power supply solution. A detailed 200W telecom power supply reference design using the ISL6551IREC with companion Intersil ICs, Supervisor and Monitor ISL6550 and Half-bridge Driver HIP2100, is presented in Application Note AN1002.

In addition, the ISL6551IREC can also be designed in push-pull converters using all of the features except the two upper drivers and adjustable resonant delay features.

Features

- Full Traceability Through Assembly and Test by Date/Trace Code Assignment
- Enhanced Process Change Notification per MIL-PRF-38535
- Enhanced Obsolescence Management
- High Speed PWM (up to 1MHz) for ZVS Full Bridge Control
- Current Mode Control Compatible
- High Current High-Side and Low-Side Totem-Pole Drivers
- Adjustable Resonant Delay for ZVS
- 10MHz Error Amplifier Bandwidth
- Programmable Soft-Start
- Precision Bandgap Reference
- Latching Shutdown Input
- Non-latching Enable Input
- Adjustable Leading Edge Blanking
- Adjustable Dead Time Control
- Adjustable Ramp for Slope Compensation
- Fast Short-Circuit Protection (Hiccup Mode)
- Adjustable Cycle-by-Cycle Peak Current Limiting
- Drive Signals to Implement Synchronous Rectification
- VDD Undervoltage Lockout
- Current Share Support
- ±5% “In Regulation” Indication
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package Footprint, which Improves PCB Efficiency and has a Thinner Profile

Applications

- Full-Bridge and Push-Pull Converters
- Power Supplies for Off-line and Telecom/Datacom
- Power Supplies for High End Microprocessors and Servers

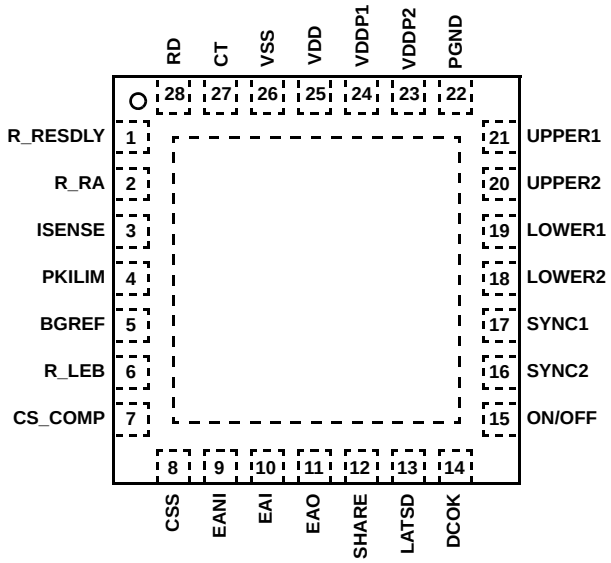
Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6551IREC	ISL 6551IR	0 to +85	28 Ld 6x6 QFN (Pb-free)	L28.6x6
ISL6551IR-TEC*	ISL 6551IR	0 to +85	28 Ld 6x6 QFN (Pb-free)	L28.6x6

*Please refer to TB347 for details on reel specifications.

Pinout

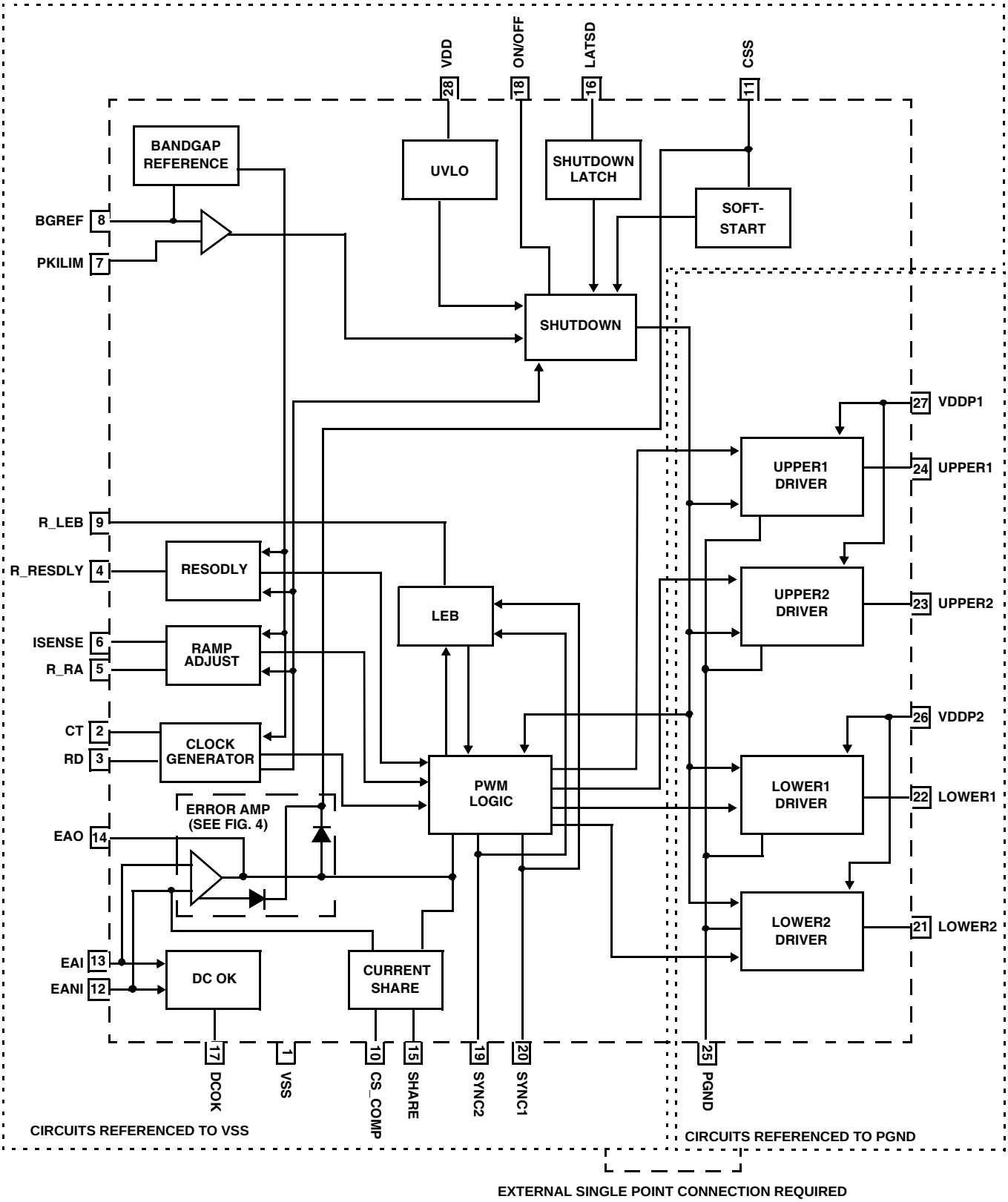
ISL6551IREC
(28 LD QFN)
TOP VIEW



Functional Pin Description

PIN #	PIN SYMBOL	FUNCTION
26	VSS	Reference ground. All control circuits are referenced to this pin.
27	CT	Set the oscillator frequency, up to 1MHz.
28	RD	Adjust the clock dead time from 50ns to 1000ns.
1	R_RESDLY	Program the resonant delay from 50ns to 500ns.
2	R_RA	Adjust the ramp for slope compensation (from 50mV to 250mV).
3	ISENSE	The pin receives the current information via a current sense transformer or a power resistor.
4	PKILIM	Set the overcurrent limit with the bandgap reference as the trip threshold.
5	BGREF	Precision bandgap reference, 1.263V ±2% overall recommended operating conditions.
6	R_LEB	Program the leading edge blanking from 50ns to 300ns.
7	CS_COMP	Set a low current sharing loop bandwidth with a capacitor.
8	CSS	Program the rise time and the clamping voltage with a capacitor and a resistor, respectively.
9	EANI	Non-inverting input of Error Amp. It is clamped by the voltage at the CSS pin (Vclamp).
10	EAI	Inverting input of Error Amp. It receives the feedback voltage.
11	EAO	Output of Error Amp. It is clamped by the voltage at the CSS pin (Vclamp).
12	SHARE	This pin is the SHARE BUS connecting with other unit(s) for current share operation.
13	LATSD	The IC is latched off with a voltage greater than 3V at this pin and is reset by recycling VDD.
14	DCOK	Power-Good indication with a ±5% window.
15	ON/OFF	This is an Enable pin that controls the states of all drive signals and the soft-start.
16, 17	SYNC2, SYNC1	These are the gate control signals for the output synchronous rectifiers.
18, 19	LOWER2, LOWER1	Both lower drivers are PWM-controlled on the trailing edge.
20, 21	UPPER2, UPPER1	Both upper drivers are driven at a fixed 50% duty cycle.
22	PGND	Power Ground. High current return paths for both the upper and the lower drivers.
23, 24	VDDP2, VDDP1	Power is delivered to both the upper and the lower drivers through these pins.
25	VDD	Power is delivered to all control circuits including SYNC1 and SYNC2 via this pin.

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage VDD, VDDP1, VDDP2 . . . . . -0.3 to 16V
Enable Inputs (ON/OFF, LATSD) . . . . . VDD
Power Good Sink Current (I_{DCOK}) 5mA

Recommended Operating Conditions

Ambient Temperature Range . . . . . 0°C to +85°C
Supply Voltage Range, VDD . . . . . 10.8V to 13.2V
Supply Voltage Range, VDDP1 and VDDP2 . . . . . <13.2V
Maximum Operating Junction Temperature . . . . . +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	30	2.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

These specifications apply for VDD = VDDP = 12V and T_A = 0°C to +85°C, Unless Otherwise Stated. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY (VDD, VDDP1, VDDP2)						
Supply Voltage	VDD		10.8	12.0	13.2	V
Bias Current from VDD	IDD	VDD = 12V (not including drivers current at VDDP)	5	13	18	mA
Total Current from VDD and VDDP	ICC	VDD = VDDP = 12V, F = 1MHz, 1.6nF Load		60		mA
UNDERVOLTAGE LOCKOUT (UVLO)						
Start Threshold	VDD_{ON}		9.2	9.6	9.9	V
Stop Threshold	VDD_{OFF}		8.03	8.6	8.87	V
Hysteresis	VDD_{HYS}		0.3	1	1.9	V
CLOCK GENERATOR (CT, RD)						
Frequency Range	F	VDD = 12V (Figure 1)	100		1000	kHz
Dead Time Pulse Width (Note 3)	DT	VDD = 12V (Figure 3)	50		1000	ns
BANDGAP REFERENCE (BGREF)						
Bandgap Reference Voltage	VREF	VDD = 12V, 399kΩ pull-up, 0.1µF, after trimming	1.250	1.263	1.280	V
Bandgap Reference Output Current	IREF	VDD = 12V, see “Block/Pin Functional Descriptions” on page 9 for details			100	µA
PWM DELAYS (Note 3)						
LOW1, 2 delay “Rising”	LOWR	With respect to RESDLY rising		5		ns
LOW1, 2 delay “Falling”	LOWF	Compare Delay @ Verror = Vramp		44		ns
SYNC1, 2 delay “Falling”	SYNCF	With respect to RESDLY falling and with 20pF load		18		ns
SYNC1, 2 delay “Rising”	SYNCR	With respect to CLK rising and with 20pF load		20		ns
ERROR AMPLIFIER (EANI, EAI, EAO) (Note 3)						
Unity Gain Bandwidth	UGBW			10		MHz
DC Gain	DCG			79		dB
Maximum Offset Error Voltage	Vos				3.1	mV
Input Common Mode Range	Vcm	VDD = 12V	0.4		9	V
Common Mode Rejection Ratio	CMMR			82		dB
Power Supply Rejection Ratio	PSSR	1mA load		95		dB
Maximum Output Source Current	ISRC		2			mA

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Lower Saturation Voltage	Vsatlow	Sinking 0.27mA			125	mV
RAMP ADJUST (R_RA) (Note 3)						
Ramp Frequency	F		100		1000	kHz
Linear Voltage Ramp, Minimum	LVR			50		mV
Linear Voltage Ramp, Maximum				250		mV
Overall Variation				25		%
PEAK CURRENT LIMIT (PKILIM)						
Peak Current Shutdown Threshold	IpkThr	BGREF = 0.1µF, 399kΩ pull-up	1.25	1.263	1.31	V
Peak Current Shutdown Delay (Note 3)	IpkDel			75		ns
SOFT-START (CSS)						
Charge Current	Iss	Vcss = 0.6V	8		12	µA
Discharge Current	Idis		1.6		5.2	mA
Cycle-by-Cycle Current Limit	Vclamp		2		8	V
DRIVERS (UPPER1, UPPER2, LOWER1, LOWER2)						
Maximum Capacitive Load (each)	CL	VDD = VDDP = 12V, F = 1MHz, Thermal Dependence	1600			pF
Turn-On Rise Time	t_r	1.0nF Capacitive load		8.9	16	ns
Turn-Off Fall Time	t_f	1.0nF Capacitive load		6.4	10	ns
Shutdown Delay (Note 3)	t_{SD}	1.0nF Capacitive load		14.5		ns
Rising Edge Delay (Note 3)	t_{RD}	1.0nF Capacitive load		16.4		ns
Falling Edge Delay (Note 3)	t_{FD}	1.0nF Capacitive load		13.7		ns
Vsat_sourcing	Vsat_high	Sourcing 20mA			1.00	V
		Sourcing 200mA			1.35	V
Vsat_sinking	Vsat_low	Sinking 20mA			0.035	V
		Sinking 200mA			0.31	V
SYNCHRONOUS SIGNALS (SYNC1, SYNC2)						
Maximum Capacitive Load		VDD = 12, F = 1MHz	20			pF
PROGRAMMABLE DELAYS (RESDLY, LEB) (Note 3)						
Resonant Delay Adjust Range		(Figure 7)	50		500	ns
Resonant Delay	t_{RESDLY}	R_RESDLY = 10k		55		ns
		R_RESDLY = 120k		488		ns
Leading Edge Blanking Adjust Range		(Figure 8)	50		300	ns
Leading Edge Blanking	t_{LEB}	R_LEB = 20k		64		ns
		R_LEB = 140k		302		ns
		R_LEB = 12V		0		ns
LATCHING SHUTDOWN (LATSD)						
Fault Threshold	VIN		3			V
Fault_NOT Threshold	VINN				1.9	V
Time to Set latch (Note 3)	t_{SET}			415		ns
ON/OFF (ONOFF)						
Turn-off Threshold	OFF				0.8	V
Turn-on Threshold	ON		2			V

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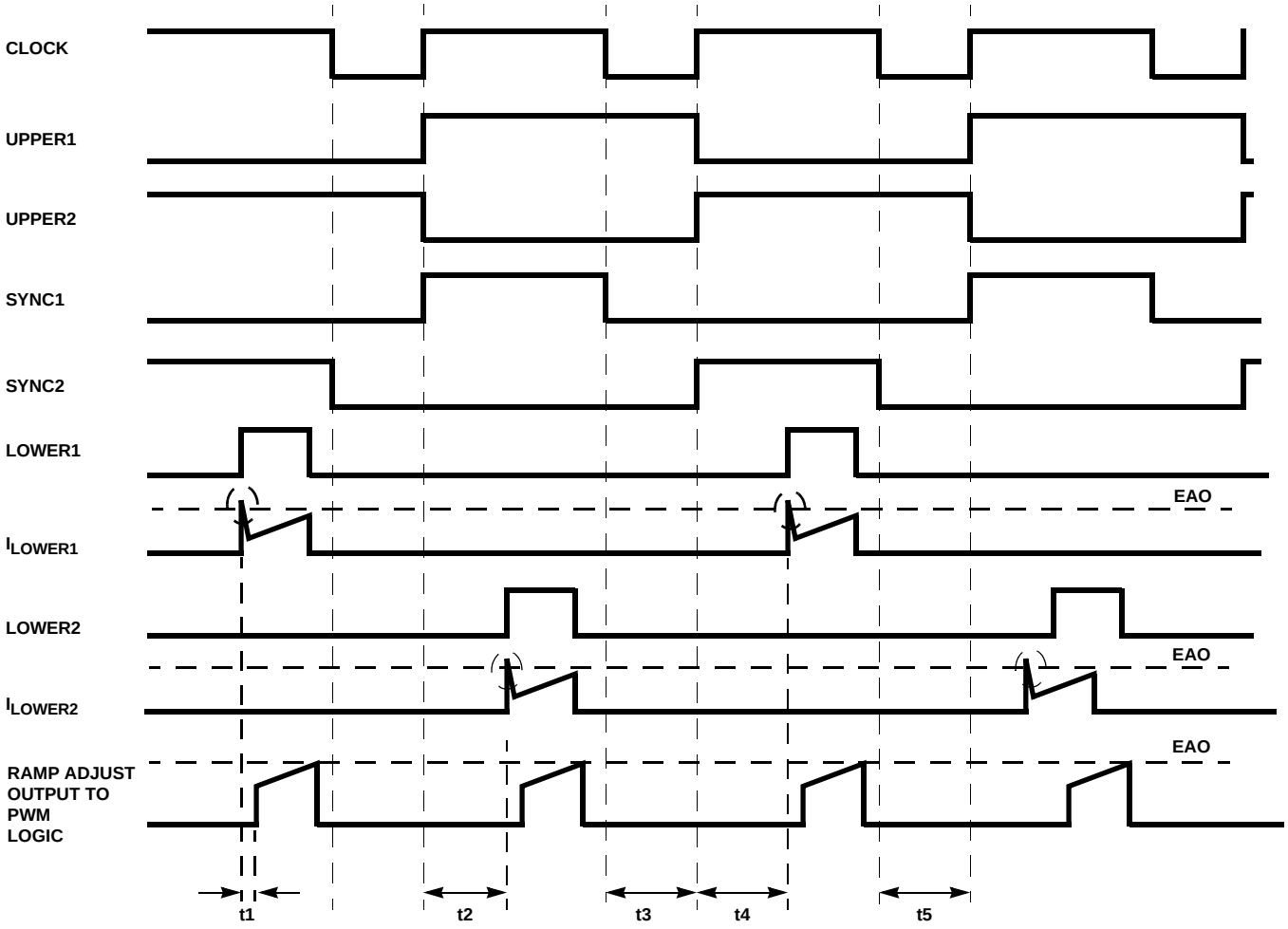
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT SHARE (SHARE, CS_COMP) (Note 3)						
Voltage Offset Between Error Amp Voltage of Master and Slave	Vcs_offset	SHARE = 30k		30		mV
Maximum Source Current to External Reference	Ics_source	SHARE = 30k		190		µA
Maximum Correctable Deviation In Reference Voltage Between Master and Slave		SHARE = 30K, Rsource = 1k, OUTPUT REFERENCE = 1 to 5V, (See Figure 10)		190		mV
Share/Adjust Loop Bandwidth	CS BW	CS_COMP = 0.1µF		500		Hz
DC OK (DCOK)						
Sink Current	I_{DCOK}				5	mA
Saturation Voltage	$V_{SATDCOK}$	I_{DCOK} = 5mA			0.4	V
Input Reference	Vref_in		1		5	V
Threshold (Relative to Vref_in)	OV	(Figure 11)		5		%
Recovery (Relative to Vref_in)	OV	(Figure 11)		3		%
Threshold (Relative to Vref_in)	UV	(Figure 11)		-5		%
Recovery (Relative to Vref_in)	UV	(Figure 11)		-3		%
Transient Rejection (Note 3)	TRej	100mV transient on Vout (system implicit rejection and feedback network dependence (Figure 12)		250		µs

NOTE:

3. Limits established by characterization and are not production tested.

Drive Signals Timing Diagrams

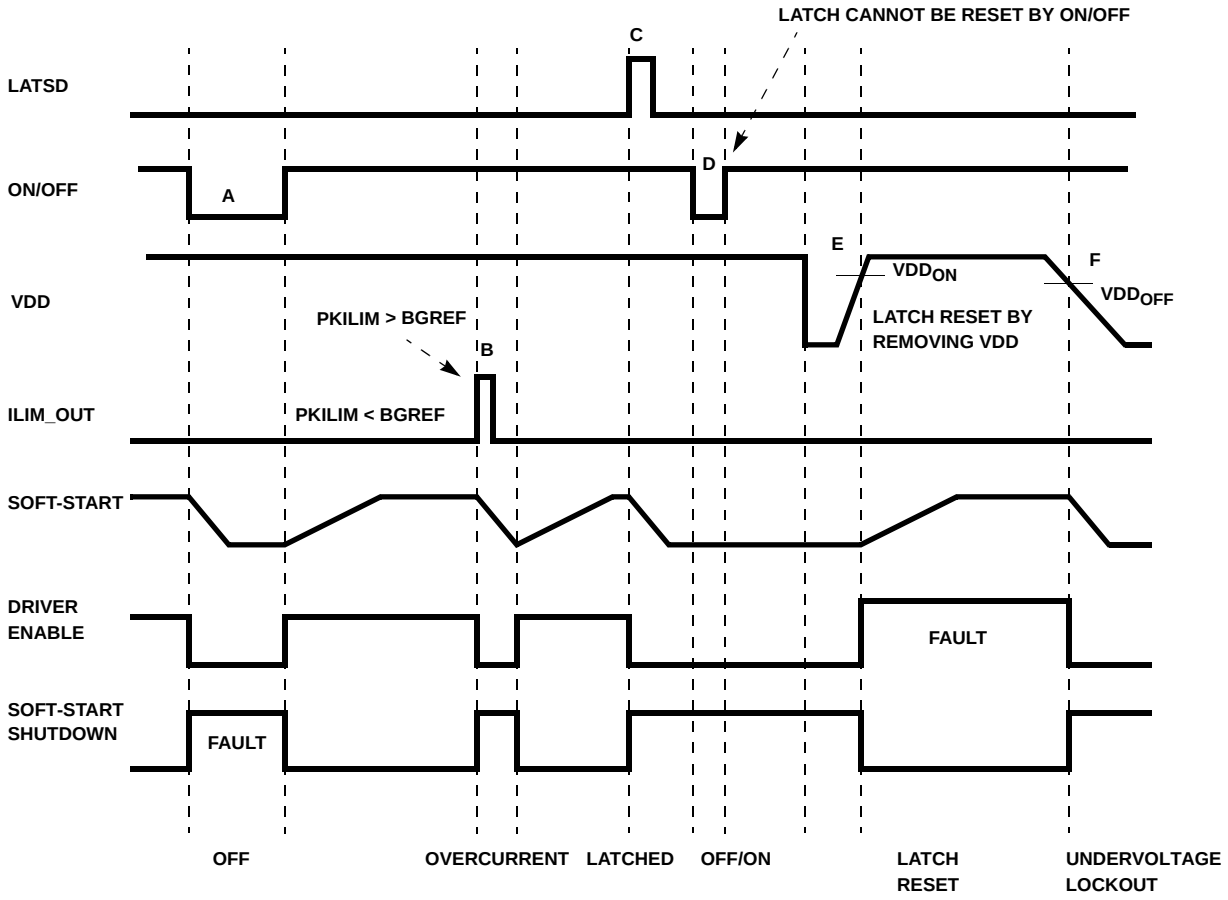


NOTES:
t1 = Leading edge blanking
t2 = t4 = Resonant delay
t3 = t5 = dead time
In the above figure, the values for t1 through t5 are exaggerated for demonstration purposes.

Timing Diagram Descriptions

The two upper drivers (UPPER1 and UPPER2) are driven at a fixed 50% duty cycle and the two lower drivers (LOWER1 and LOWER2) are PWM-controlled on the trailing edge, while the leading edge employs resonant delay (t2 and t4). In current mode control, the sensed switch (FET) current (I_{LOWER1} and I_{LOWER2}) is processed in the Ramp Adjust and Leading Edge Blanking (LEB) circuits and then compared to a control signal (EAO). Spikes, due to parasitic elements in the bridge circuit, would falsely trigger the comparator generating the PWM signal. To prevent false triggering, the leading edge of the sensed current signal is blanked out by t1, which can be programmed at the R_LEB pin with a resistor. Internal switches gate the analog input to the PWM comparator, implementing the blanking function that eliminates response degrading delays, which would be caused if filtering of the current feedback was incorporated. The dead time (t3 and t5) is the delay to turn on the upper FET (UPPER1/UPPER2) after its corresponding lower FET (LOWER1/LOWER2) is turned off when the bridge is operating at maximum duty cycle in normal conditions, or is responding to load transients or input line dipping conditions. Therefore, the upper and lower FETs that are located at the same side of the bridge can never be turned on together, which eliminates shoot-through currents. SYNC1 and SYNC2 are the gate control signals for the output synchronous rectifiers. They are biased by VDD and are capable of driving capacitive loads up to 20pF at 1MHz clock frequency (500kHz switching frequency). External drivers with high current capabilities are required to drive the synchronous rectifiers, cascading with both synchronous signals (SYNC1 and SYNC2).

Shutdown Timing Diagrams



Shutdown Timing Descriptions

A (ON/OFF)

When the ON/OFF is pulled low, the soft-start capacitor is discharged and all the drivers are disabled. When the ON/OFF is released without a fault condition, a soft-start is initiated.

B (OVERCURRENT)

If the output of the converter is over loaded, i.e., the PKILIM is above the bandgap reference voltage (BGREF), the soft-start capacitor is discharged very quickly and all the drivers are turned off. Thereafter, the soft-start capacitor is charged slowly, and discharged quickly if the output is overloaded again. The soft-start will remain in hiccup mode as long as the overload conditions persist. Once the overload is removed, the soft-start capacitor is charged up and the converter is then back to normal operation.

C (LATCHING SHUTDOWN)

The IC is latched off completely as the LATSD pin is pulled high, and the soft-start capacitor is reset.

D (ON/OFF)

The latch cannot be reset by the ON/OFF.

E (LATCH RESET)

The latch is reset by removing the VDD. The soft-start capacitor starts to be charged after VDD increases above the turn-on threshold VDD_{ON}.

F (VDD UVLO)

The IC is turned off when the VDD is below the turn-off threshold VDD_{OFF}. Hysteresis VDD_{HYS} is incorporated in the undervoltage lockout (UVLO) circuit.

Block/Pin Functional Descriptions

Detailed descriptions of each individual block in the functional block diagram on page 3 are included in this section. Application information and design considerations for each pin and/or each block are also included.

IC Bias Power (VDD, VDDP1, VDDP2)

- The IC is powered from a 12V ±10% supply.
- VDD supplies power to both the digital and analog circuits and should be bypassed directly to the VSS pin with an 0.1µF low ESR ceramic capacitor.

- VDDP1 and VDDP2 are the bias supplies for the upper drivers and the lower drivers, respectively. They should be decoupled with ceramic capacitors to the PGND pin.
- Heavy copper should be attached to these pins for a better heat spreading.

IC GNDs (VSS, PGND)

- VSS is the reference ground, the return of VDD, of all control circuits and must be kept away from nodes with switching noises. It should be connected to the PGND in only one location as close to the IC as practical. For a secondary side control system, it should be connected to the net after the output capacitors, i.e., the output return pinout(s). For a primary side control system, it should be connected to the net before the input capacitors, i.e., the input return pinout(s).
- PGND is the power return, the high-current return path of both VDDP1 and VDDP2. It should be connected to the SOURCE pins of two lower power switches or the RETURNs of external drivers as close as possible with heavy copper traces.
- Copper planes should be attached to both pins.

Undervoltage Lockout (UVLO)

- UVLO establishes an orderly start-up and verifies that VDD is above the turn-on threshold voltage (VDD_{ON}). All the drivers are held low during the lockout. UVLO incorporates hysteresis VDD_{HYS} to prevent multiple startup/shutdowns while powering up.
- UVLO limits are not applicable to VDDP1 and VDDP2.

Bandgap Reference (BGREF)

- The reference voltage VREF is generated by a precision bandgap circuit.
- This pin must be pulled up to VDD with a resistance of approximately 399kΩ for proper operation. For additional reference loads (no more than 1mA), this pull-up resistor should be scaled accordingly.
- This pin must also be decoupled with an 0.1µF low ESR ceramic capacitor.

Clock Generator (CT, RD)

- This free-running oscillator is set by two external components, as shown in Figure 2. A capacitor at CT is charged and discharged with two equal constant current sources and fed into a window comparator to set the clock frequency. A resistor at RD sets the clock dead time. RD and CT should be tied to the VSS pin on their other ends as close as possible. The corresponding CT for a particular frequency can be selected from Figure 1.
- The switching frequency (Fsw) of the power train is half of the clock frequency (Fclock), as shown in Equation 1.

$$Fsw = \frac{Fclock}{2} \quad \text{(EQ. 1)}$$

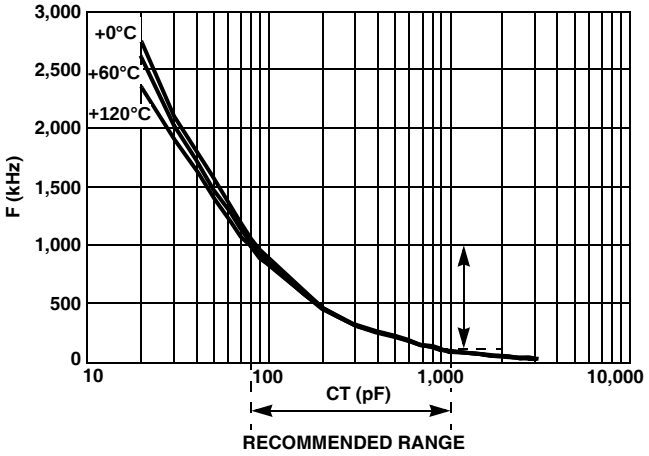


FIGURE 1. CT vs FREQUENCY

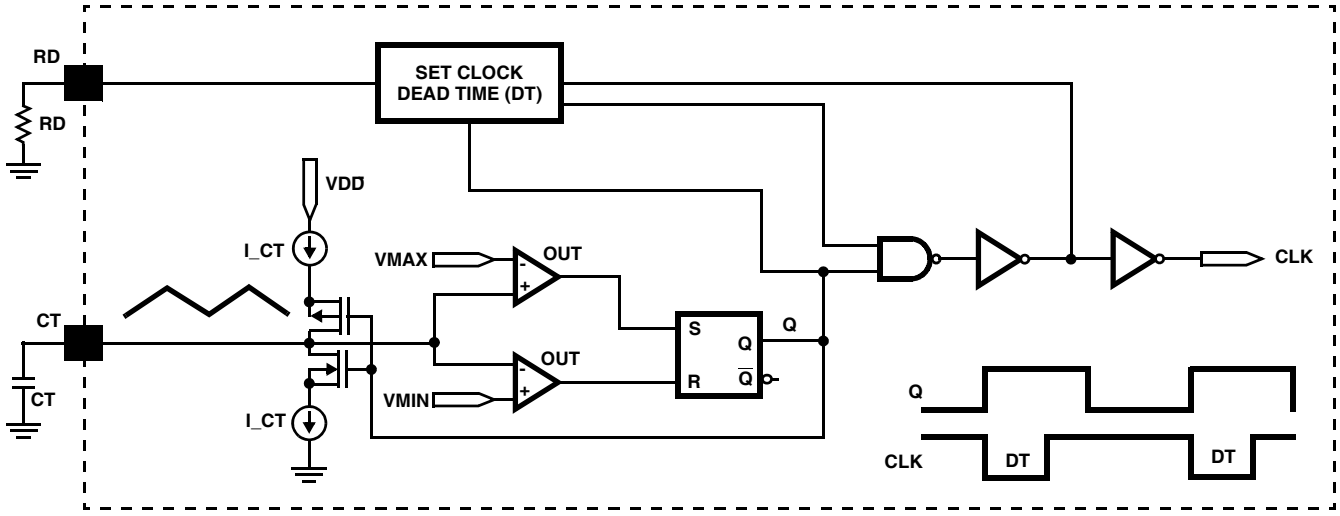


FIGURE 2. SIMPLIFIED CLOCK GENERATOR CIRCUIT

- Note that the capacitance of a scope probe (~12pF for single-ended) would induce a smaller frequency at the CT pin. It can be easily seen at a higher frequency. An accurate operating frequency can be measured at the outputs of the bridge/synchronous drivers.

The dead time is the delay to turn on the upper FET (UPPER1/UPPER2) after its corresponding lower FET (LOWER1/LOWER2) is turned off when the bridge is operating at maximum duty cycle in normal conditions, or is responding to load transients or input line dipping conditions. This helps to prevent shoot through between the upper FET and the lower FET that are located at the same side of the bridge. The dead time can be estimated using Equation 2:

$$DT = \frac{M \times RD}{k\Omega} \quad (ns) \qquad \text{(EQ. 2)}$$

where M = 11.4 (VDD = 12V), 11.1(VDD = 14V), and 12 (VDD = 10V), and RD is in kΩ. This relationship is shown in Figure 3.

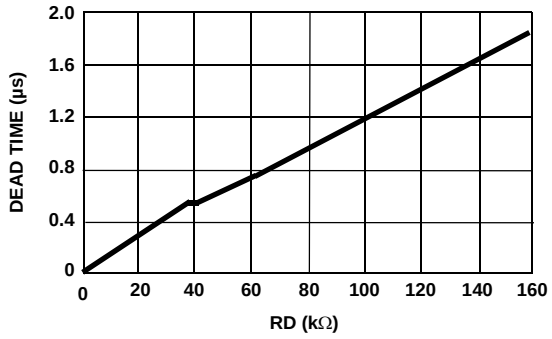


FIGURE 3. RD vs DEAD TIME (VDD = 12V)

Error Amplifier (EAI, EANI, EAO)

- This amplifier compares the feedback signal received at the EAI pin to a reference signal set at the EANI pin and provides an error signal (EAO) to the PWM Logic. The feedback loop compensation can be programmed via these pins.
- Both EANI and EAO are clamped by the voltage (Vclamp) set at the CSS pin, as shown in Figure 5. Note that the diodes in the functional block diagram represent the clamp function of the CSS in a simplified way.

Soft-Start (CSS)

- The voltage on an external capacitor charged by an internal current source I_{SS} is fed into a control pin on the error amplifier. This causes the Error Amplifier to: 1) limit the EAO to the soft-start voltage level; and 2) over-ride the reference signal at the EANI with the soft-start voltage, when the EANI voltage is higher than the soft-start voltage. Thus, both the output voltage and current of the power supply can be controlled by the soft-start.
- The clamping voltage determines the cycle-by-cycle peak current limiting of the power supply. It should be set above the EANI and EAO voltages and can be programmed by an external resistor, as shown in Figure 5 using Equation 3.

$$Vclamp = Rcss \bullet Iss \quad (V) \qquad \text{(EQ. 3)}$$

- Per Equation 3, the clamping voltage is a function of the charge current Iss. For a more predictable clamping voltage, the CSS pin can be connected to a reference based clamp circuit, as shown in Figure 4. To make the Vclamp less dependent on the soft-start current (Iss), the currents flowing through R1 and R2 should be scaled much greater than Iss. The relationship of this circuit can be found in Equation 4.

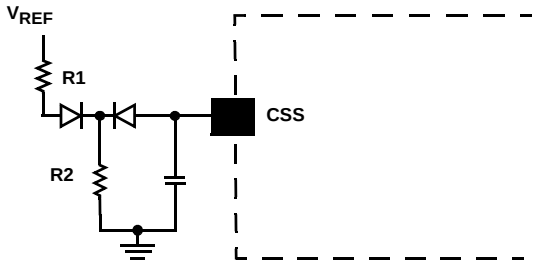


FIGURE 4. REFERENCE-BASED CLAMP CIRCUIT

$$Vclamp \approx Iss \bullet \frac{R1 \times R2}{R1 + R2} + Vref \bullet \frac{R2}{R1 + R2} \qquad \text{(EQ. 4)}$$

- The soft-start rise time (t_{ss}) can be calculated with Equation 5. The rise time (t_{rise}) of the output voltage is approximated with Equation 6.

$$t_{rise} = \frac{EANI \times Css}{Iss} \quad (s) \qquad \text{(EQ. 6)}$$

$$t_{ss} = \frac{Vclamp \times Css}{Iss} \quad (s) \qquad \text{(EQ. 5)}$$

Drivers (Upper1, Upper2, Lower1, Lower2)

- The two upper drivers are driven at a fixed 50% duty cycle and the two lower drivers are PWM-controlled on the trailing edge while the leading edge employs resonant delay. They are biased by VDDP1 and VDDP2, respectively.
- Each driver is capable of driving capacitive loads up to CL at 1MHz clock frequency and higher loads at lower frequencies on a layout with high effective thermal conductivity.
- The UVLO holds all the drivers low until the VDD has reached the turn-on threshold VDD_{ON}.
- The upper drivers require assistance of external level-shifting circuits, such as Intersil's HIP2100 or pulse transformers to drive the upper power switches of a bridge converter.

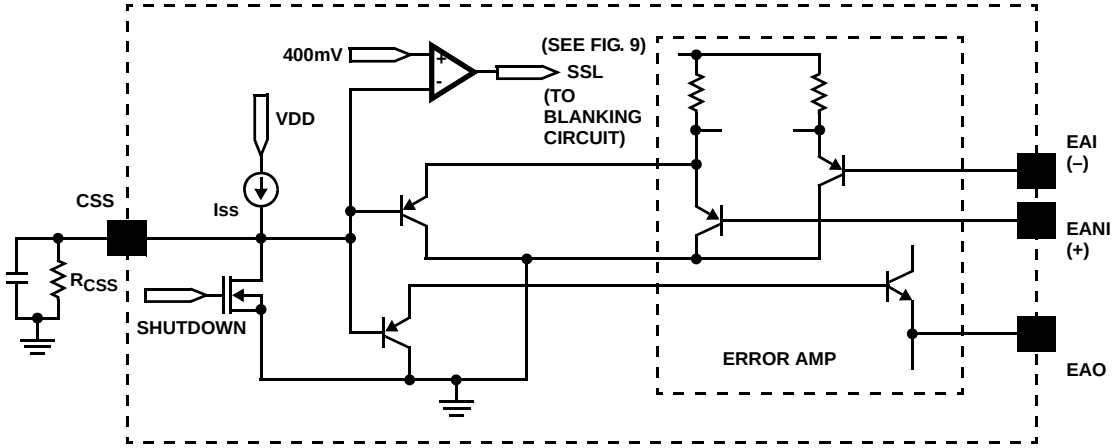


FIGURE 5. SIMPLIFIED CLAMP/SOFT-START

Peak Current Limit (PKILIM)

- When the voltage at PKILIM exceeds the BGREF voltage, the gate pulses are terminated and held low until the next clock cycle. The peak current limit circuit has a high-speed loop with propagation delay IpkDel. Peak current shutdown initiates a soft-start sequence.
- The peak current shutdown threshold is usually set slightly higher than the normal cycle-by-cycle PWM peak current limit (Vclamp) and therefore will normally only be activated in a short-circuit condition. The limit can be set with a resistor divider from the ISENSE pin. The resistor divider relationship is defined in Equation 7.
- In general, the trip point is a little smaller than the BGREF due to the noise and/or ripple at the BGREF.

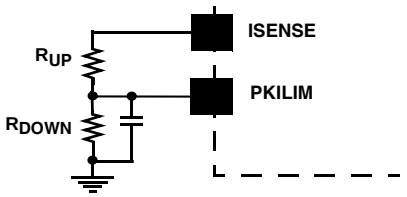


FIGURE 6. PEAK CURRENT LIMIT SET CIRCUIT

$$\frac{Rdown}{Rdown + Rup} = \frac{BGREF}{ISENSE(max)} \quad \text{(EQ. 7)}$$

Latching Shutdown (LATSD)

- A high TTL level on LATSD latches the IC off. The IC goes into a low power mode and is reset only after the power at the VDD pin is removed completely. The ON/OFF cannot reset the latch.
- This pin can be used to latch the power supply off on output overvoltage or other undesired conditions.

ON/OFF (ON/OFF)

- A high standard TTL input (safe also for VDD level) signals the controller to turn on. A low TTL input turns off the controller and terminates all drive signals including the SYNC outputs. The soft-start is reset.
- This pin is a non-latching input and can accept an enable command when monitoring the input voltage and the thermal condition of a converter.

Resonant Delay (R_RESDLY)

- A resistor tied between R_RESDLY and VSS determines the delay that is required to turn on a lower FET after its corresponding upper FET is turned off. This is the resonant delay, which can be estimated with Equation 8.

$$t_{RESDLY} = 4.01 \times R\_RESDLY/k\Omega + 13 \text{ (ns)} \quad \text{(EQ. 8)}$$

- Figure 7 illustrates the relationship of the value of the resistor (R_RESDLY) and the resonant delay (t_{RESDLY}). The percentages in the figure are the tolerances at the two end points of the curve.

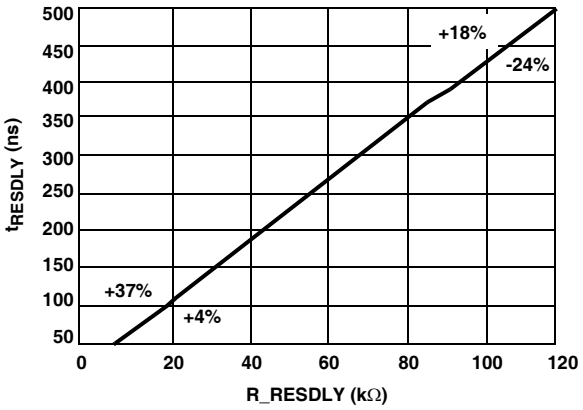


FIGURE 7. R_RESDLY vs RESDLY

Leading Edge Blanking (R_LEB)

- In current mode control, the sensed switch (FET) current is processed in the Ramp Adjust and LEB circuits and then compared to a control signal (EAO voltage). Spikes, due to parasitic elements in the bridge circuit, would falsely trigger the comparator generating the PWM signal. To prevent false triggering, the leading edge of the sensed current signal is blanked out by a period that can be programmed with the R_LEB resistor. Internal switches gate the analog input to the PWM comparator, implementing the blanking function that

eliminates response degrading delays which would be caused if filtering of the current feedback was incorporated. The current ramp is blanked out during the resonant delay period because no switching occurs in the lower FETs. The leading edge blanking function will not be activated until the soft-start (CSS) reaches over 400mV, as illustrated in Figures 5 and 9. The leading edge blanking (LEB) function can be disabled by tying the R_LEB pin to VDD, i.e., LEB = 1. Never leave the pin floating.

- The blanking time can be estimated with Equation 9, whose relationship can be seen in Figure 8. The percentages in the figure are the tolerances at the two endpoints of the curve.

$$t_{LEB} = 2 \times R\_LEB / k\Omega + 15\ (ns) \quad \text{(EQ. 9)}$$

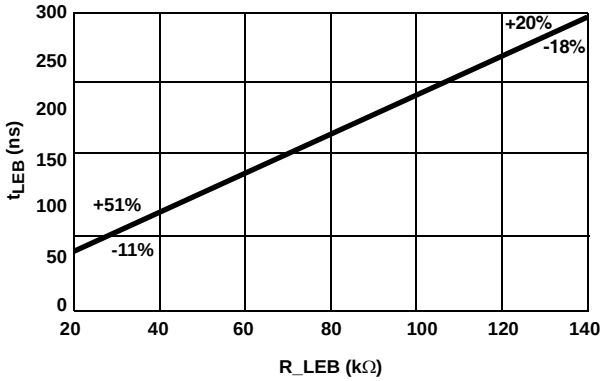


FIGURE 8. R_LEB vs t_{LEB}

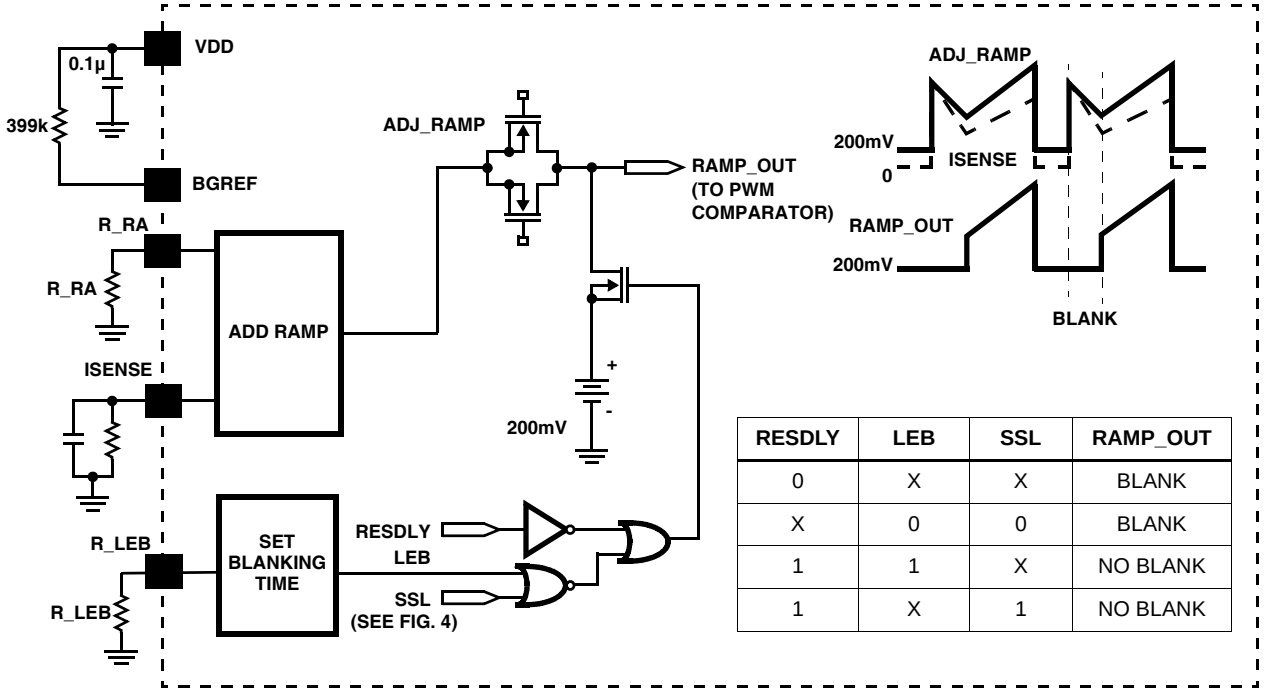
Ramp Adjust (R_RA, ISENSE)

- The ramp adjust block adds an offset component (200mV) and a slope adjust component to the ISENSE signal before processing it at the PWM Logic block, as shown in Figure 9. This ensures that the ramp voltage is always higher than the OAGS (ground sensing op amp) minimum voltage to achieve a “zero” state.
- It is critical that the input signal to ISENSE decays to zero prior to or during the clock dead time. The level-shifting and capacitive summing circuits in the RAMP ADJUST block are reset during the dead time. Any input signal transitions that occur after the rising edge of CLK and prior to the rising edge of RESDLY can cause severe errors in the signal reaching the PWM comparator.
- Typical ramp values are hundreds of mV over the period on a 3V full scale current. Too much ramp makes the controller look like a voltage mode PWM, and too little ramp leads to noise issues (jitter). The amount of ramp (Vramp), as shown in Figure 9, is programmed with the R_RA resistor and can be calculated with Equation 10.

$$V_{ramp} = BGREF \times dt / (R\_RA \times 500E\text{-}12)\ (V) \quad \text{(EQ. 10)}$$

where dt = Duty Cycle/Fsw - t_{LEB} (s). Duty cycle is discussed in detail in application note AN1002.

- The voltage representation of the current flowing through the power train at ISENSE pin is normally scaled such that the desired peak current is less than or equal to Vclamp-200mV-Vramp, where the clamping voltage is set at the CSS pin.



RESDLY	LEB	SSL	RAMP_OUT
0	X	X	BLANK
X	0	0	BLANK
1	1	X	NO BLANK
1	X	1	NO BLANK

FIGURE 9. SIMPLIFIED RAMP ADJUST AND LEADING EDGE BLANKING CIRCUITS

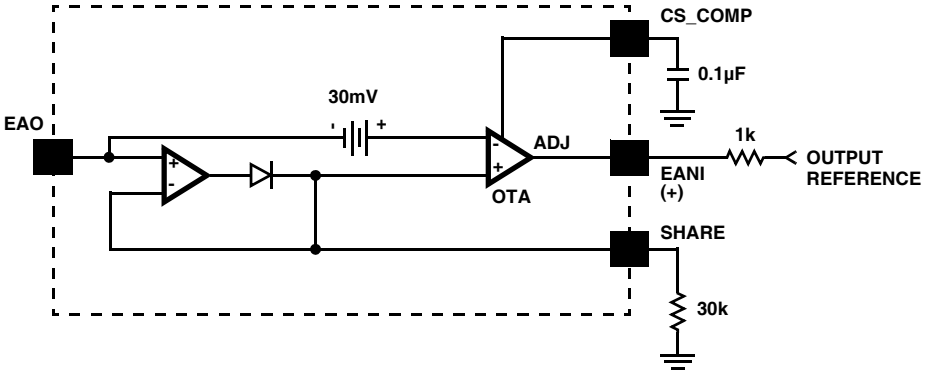


FIGURE 10. SIMPLIFIED CURRENT SHARE CIRCUIT

SYNC Outputs (SYNC1, SYNC2)

- SYNC1 and SYNC2 are the gate control signals for the output synchronous rectifiers. They are biased by VDD and are capable of driving capacitive loads up to 20pF at 1MHz clock frequency (500kHz switching frequency). These outputs are turned off sooner than the turn-off at UPPER1 and UPPER2 by the clock dead time, DT.
- Inverting both SYNC signals or both LOWER signals is another possible way to control the drivers of the synchronous rectifiers. When using these drive schemes, the user should understand the issues that might occur in his/her applications, especially the impacts on current share operation and light load operation. Refer to application note AN1002 for more details.
- External high current drivers controlled by the synchronous signals are required to drive the synchronous rectifiers. A pulse transformer is required to pass the drive signals to the secondary side if the IC is used in a primary control system.

Share Support (SHARE, CS_COMP)

- The unit with the highest reference is the master. Other units, as slaves, adjust their references via a source resistor to match the master reference sharing the load current. The source resistor is typically 1kΩ connecting the EANI pin and the OUTPUT REFERENCE (external reference or BGREF), as shown in Figure 10. The share bus represents a 30kΩ resistive load per unit, up to 10 units.
- The output (ADJ) of “Operational Transconductance Amplifier (OTA)” can only pull high and it is floating while in master mode. This ensures that no current is sourced to the OUTPUT REFERENCE when the IC is working by itself.
- The slave units attempt to drive their error amplifier voltage to be within a pre-determined offset (30mV typical) of the master error voltage (the share bus). The current-share error is nominally (30mV/EAO)*100% assuming no other source of error. With a 2.5V full load error amp voltage, the current-share error at full load would be -1.2% (slaves relative to master).
- The bandwidth of the current sharing loop should be much lower than that of the voltage loop to eliminate noise pick-up and interactions between the voltage regulation loop and the current loop. A 0.1µF capacitor is recommended between CS_COMP and VSS pins to achieve a low current sharing loop bandwidth (100Hz to 500Hz).

Power-Good (DCOK)

- DCOK pin is an open drain output capable of sinking 5mA. It is low when the output voltage is within the UVOV window. The static regulation limit is ±3%, while the ±5% is the dynamic regulation limit. It indicates power-good when the EAI is within -3% to +5% on the rising edge and within +3% to -5% on the falling edge, as shown in Figure 11.

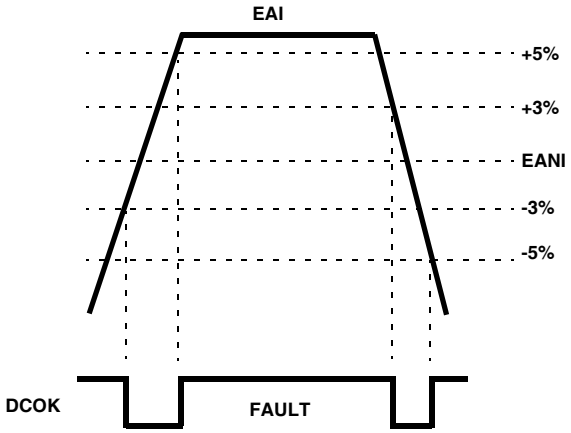


FIGURE 11. UNDERVOLTAGE-OVERVOLTAGE WINDOW

- The DCOK comparator might not be triggered even though the output voltage exceeds ± 5% limits at load transients. This is because the feedback network of the error amplifier filters out part of the transients and the EAI only sees the remaining portion that is still within the limits, as illustrated in Figure 12. The lower the “zero (1/RC)” of the error amplifier, the larger the portion of the transient that is filtered out.

Thermal Pad (in QFN only)

- In the QFN package, the pad underneath the center of the IC is a “floating” thermal substrate. The PCB “thermal land” design for this exposed die pad should include thermal vias that drop down and connect to one or more buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the QFN to achieve its full thermal potential. This pad should be connected to a low noise copper plane such as Vss.
- Refer to TB389 for design guidelines.

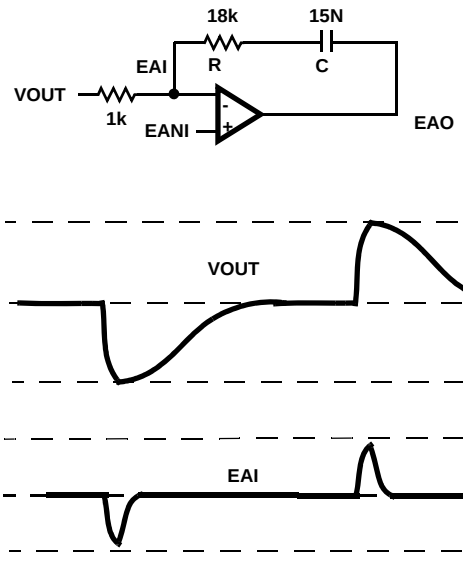


FIGURE 12. OUTPUT TRANSIENT REJECTION

Additional Applications Information

Table 11 highlights parameter setting for the ISL6551IREC. Designers can use this table as a design checklist. For detailed operation of the ISL6551IREC, see “Block/Pin Functional Descriptions” on page 9.

Figure 13 shows the block diagram of a power supply system employing the ISL6551IREC full bridge controller. The ISL6551IREC not only is a full bridge PWM controller but also can be used as a push-pull PWM controller. Users can design a power supply by selecting appropriate blocks in the System Blocks Chart based on the power system requirements. Figures 13A, 14A, 15A, 16A, 17A, 18A, 19, 20A, 21, 22A, and 24A have been used in the 200W telecom power supply reference design, which can be found in the Application Note AN1002. To meet the specifications of the power supply, minor modifications of each block are required. To take full advantage of the integrated features of the ISL6551IREC, “secondary side control” is recommended.

TABLE 1. PARAMETER SETTING HIGHLIGHTS/CHECKLIST

PARAMETER	PIN NAME	FORMULA OR SETTING HIGHLIGHT	UNIT	FIGURE #
Frequency	CT	Set 50% Duty Cycle Pulses with a fixed frequency	kHz	1, 2
Dead Time	RD	DT = MxRD/kΩ, where M = 11.4	ns	3
Resonant Delay	R_RESDLY	t_{RESDLY} = 4.01xR_RESDLY/kΩ + 13	ns	7
Ramp Adjust	R_RA	Vramp = BGREF/(R_RAx500E-12)xdt	V	-
Current Sense	ISENSE	<Vclamp - 200mV - Vramp	V	-
Peak Current	PKILIM	<BGREF and slightly higher than Vclamp	V	6
Bandgap Reference	BGREF	1.263V ±2%, 399kΩ pull-up, No more than 100µA load	V	-
Leading Edge Blanking	R_LEB	t_{LEB} = 2 x R_LEB/kΩ + 15, never leave it floating	ns	8, 9
Current Share Compensation	CS_COMP	0.1µ for a low current loop bandwidth (100 - 500Hz)	Hz	10
Soft-Start & Output Rise Time	CSS	t_{ss} = VclampxCss/Iss, t_{rise} = EANI x CSS/Iss, Iss = 10µA ±20%	S	4
Clamp Voltage (Vclamp)	CSS	Vclamp = IssxRcss, or Reference-based clamp	V	4, 5
Error Amplifier	EANI, EAI, EAO	EANI, EAO < Vclamp	V	-
Share Support	SHARE	30K load and a resistor (1k, typ.) between EANI and OUTPUT REF.	-	-
Latching Shutdown	LATSD	Latch IC off at > 3V	V	-
Power-Good	DCOK	±5% with hysteresis, Sink up to 5mA, transient rejection	V	11, 12
IC Enable	ON/OFF	Turn on/off at TTL level	V	-
Reference Ground	VSS	Connect to PGND in only one single point	-	-
Power Ground	PGND	Single point to VSS plane	-	-
Upper Drivers	UPPER1, UPPER2	Capacitive load up to 1.6nF at Fsw = 500kHz	-	-
Lower Drivers	LOWER1, LOWER2	Capacitive load up to 1.6nF at Fsw = 500kHz	-	-
Synchronous Drive Signals	SYNC1, SYNC2	Capacitive load up to 20pF at Fsw = 500kHz	-	-
Bias for Control Circuits	VDD	12V ±10%, 0.1µF decoupling capacitor	V	-
Biases for Bridge Drivers	VDDP1, VDDP2	Need decoupling capacitors	V	-

NOTE: VDD = 12V at room temperature, unless otherwise stated.

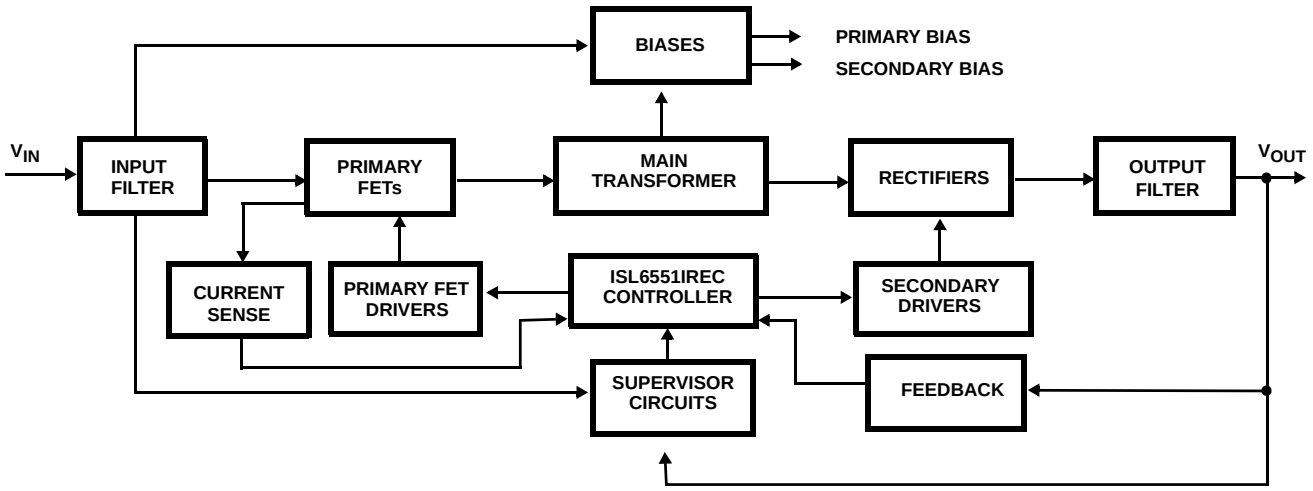


FIGURE 13. BLOCK DIAGRAM OF A POWER SUPPLY SYSTEM USING ISL6551IREC CONTROLLER

System Blocks Chart

Input Filters

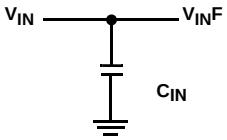


FIGURE 13A. GENERAL

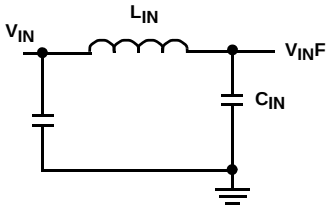


FIGURE 13B. EMI

GENERAL

Input capacitors are required to absorb the power switch (FET) pulsating currents.

EMI

For good EMI performance, the ripple current that is reflected back to the input line can be reduced by an input L-C filter, which filters the differential-mode noises and operates at two times the switching frequency, i.e., the clock frequency (Fclock). In some cases, an additional common-mode choke might be required to filter the common-mode noises.

Current Sense

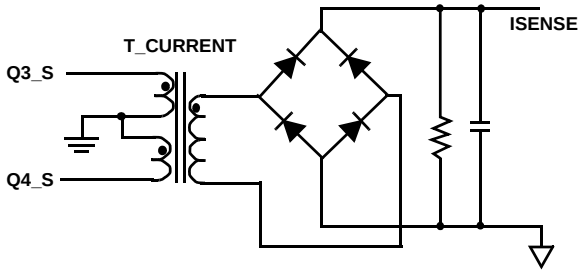


FIGURE 14A. TWO-LEG SENSE

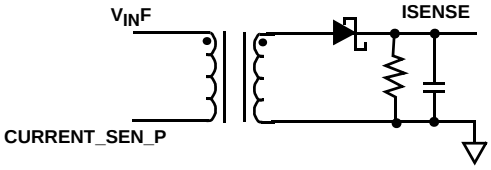


FIGURE 14B. TOP SENSE

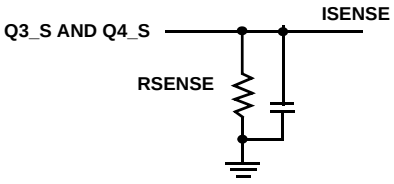


FIGURE 14C. RESISTOR SENSE (PRIMARY CONTROL)

TWO-LEG SENSE

Senses the current that flows through both lower primary FETs. Operates at the switching frequency.

TOP SENSE

Senses the sum of the current that flows through both upper primary FETs. Operates at the clock frequency.

RESISTOR SENSE

This simple scheme is used in a primary side control system. The sum of the current that flows through both lower primary FETs is sensed with a low impedance power resistor. The sources of Q3 and Q4 and ISENSE should be tied at the same point as close as possible.

Biases

Linear Regulator - In a primary side control system, a linear regulator derived from the input line can be used for the start-up purpose, and an extra winding coupled with the main transformer can provide the controller power after the start-up.

DCM Flyback - Use a PWM controller to develop both primary and secondary biases with discontinuous current mode flyback topology.

Primary FETs

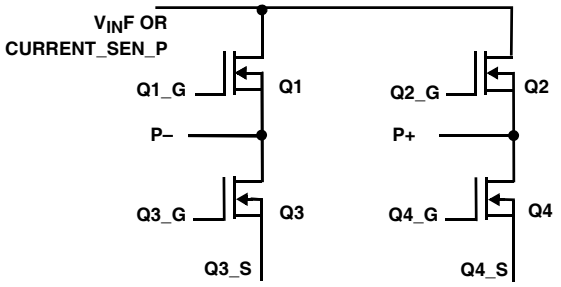


FIGURE 15A. FULL BRIDGE

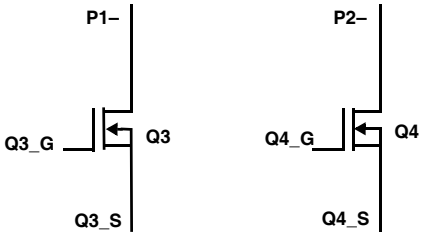


FIGURE 15B. PUSH-PULL

FULL BRIDGE

Four MOSFETs are required for full bridge converters. The drain to source voltage rating of the MOSFETs is Vin.

PUSH-PULL

Only the two lower MOSFETs are required for push-pull converters. The two upper drivers are not used. The V_{DS} of the MOSFETs is 2xVin.

Feedback

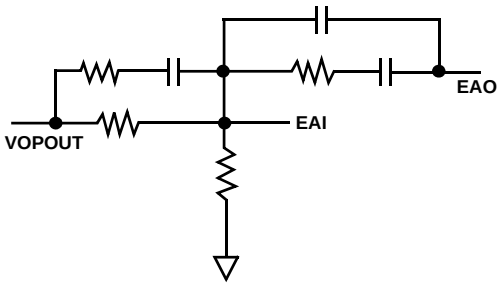


FIGURE 16A. SECONDARY CONTROL

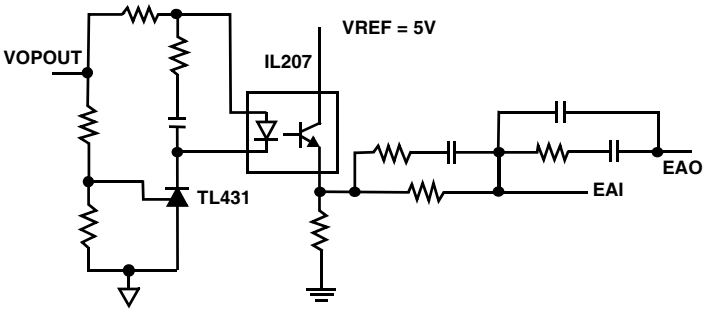


FIGURE 16B. PRIMARY CONTROL

SECONDARY CONTROL

In secondary side control systems, only a few resistors and capacitors are required to complete the feedback loop.

PRIMARY CONTROL

This feedback loop configuration for primary side control systems requires an optocoupler for isolation. The bandwidth is limited by the optocoupler.

Rectifiers

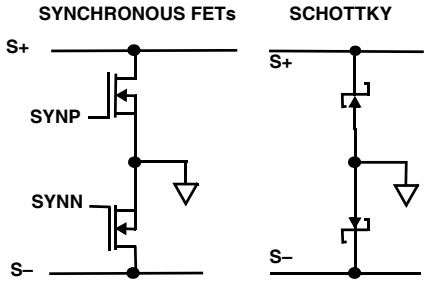


FIGURE 17A. CURRENT DOUBLER RECTIFIERS

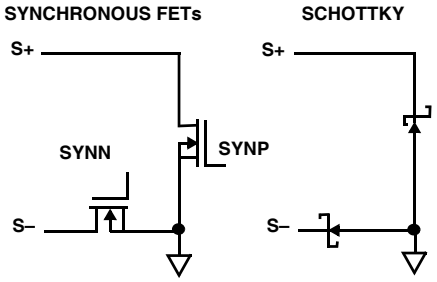


FIGURE 17B. CONVENTIONAL RECTIFIERS

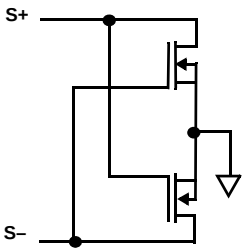


FIGURE 17C. SELF-DRIVEN RECTIFIERS

CURRENT DOUBLER RECTIFIERS

1. Synchronous FETs are used for low output voltage, high output current and/or high efficiency applications.
2. Schottky diodes are used for lower current applications. Pins S+ and S- are connected to the output filter and the main transformer with current doubler configurations.

CONVENTIONAL RECTIFIERS

1. Synchronous FETs are used for low output voltage, high output current and/or high efficiency applications.
2. Schottky diodes are used for lower current applications. Pins S+ and S- are connected to the main transformer with conventional configurations.

SELF-DRIVEN RECTIFIERS

For low output voltage applications, both FETs can be driven by the voltage across the secondary winding. This can work with all kinds of main transformer configurations, as shown in Figures 18A, 18B, 18C and 18D.

Main Transformers

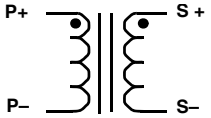


FIGURE 18A. FULL BRIDGE AND CURRENT DOUBLER

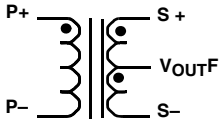


FIGURE 18B. CONVENTIONAL FULL BRIDGE

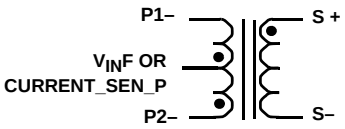


FIGURE 18C. PUSH-PULL AND CURRENT DOUBLER

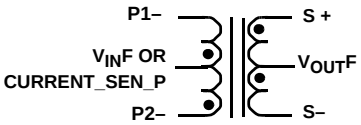


FIGURE 18D. CONVENTIONAL PUSH-PULL

FULL BRIDGE AND CURRENT DOUBLER

No center tap is required. The secondary winding carries half of the load, i.e., only half of the load is reflected to the primary.

CONVENTIONAL FULL BRIDGE

Center tap is required on the secondary side, and no center tap is required on the primary side. The secondary winding carries all the load. i.e., all the load is reflected to the primary.

PUSH-PULL AND CURRENT DOUBLER

Center tap is required on the primary side, and no center tap is required on the secondary side. The secondary winding carries half of the load, i.e., only half of the load is reflected to the primary.

CONVENTIONAL PUSH-PULL

Both primary and secondary sides require center taps. The secondary winding carries all the load, i.e., all the load is reflected to the primary.

Supervisor Circuits

INTEGRATED SOLUTION

- Intersil ISL6550 Supervisor and Monitor (SAM).
- Over-temperature protection (discrete)
- Input UV lockout (discrete)

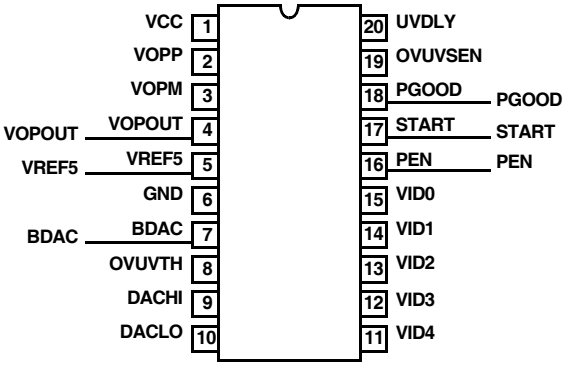


FIGURE 19. ISL6550

DISCRETE SOLUTION

- Differential Amplifier
- VCC undervoltage lockout
- Programmable output OV and UV
- Programmable output
- Status indicators (PGOOD and START)
- Precision Reference
- Over- temperature protection
- Input UV lockout

The Integrated Solution is much simpler than a discrete solution. Over-temperature protection and input undervoltage lockout can be added for better system protection and performance.

The Discrete Solution requires a significant number of components to implement the features that the ISL6550 can provide.

Output Filter

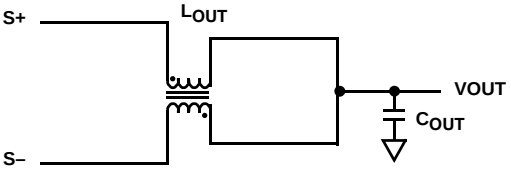


FIGURE 20A. CURRENT DOUBLER FILTER

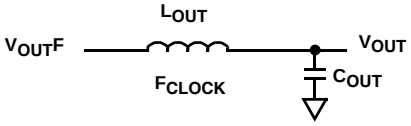


FIGURE 20B. CONVENTIONAL FILTER

Current Doubler Filter - Two inductors are needed, but they can be integrated and coupled into one core. Each inductor carries half of the load operating at the switching frequency.

Conventional Filter - One inductor is needed. The inductor carries all the load operating at two times the switching frequency.

Controller

ISL6551IREC CONTROLLER

It can be used as a full bridge or push-pull PWM controller. The QFN package requires less space.

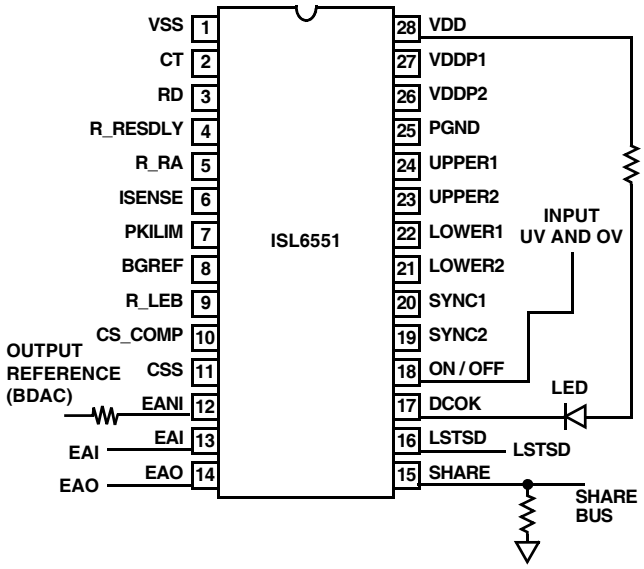


FIGURE 21. ISL6551IREC CONTROLLER

Secondary Drivers

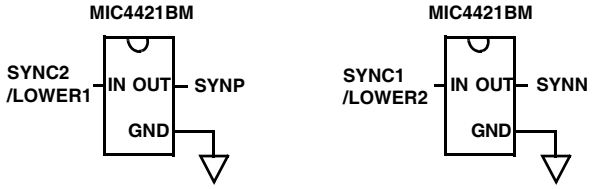


FIGURE 22A. INVERTING DRIVERS

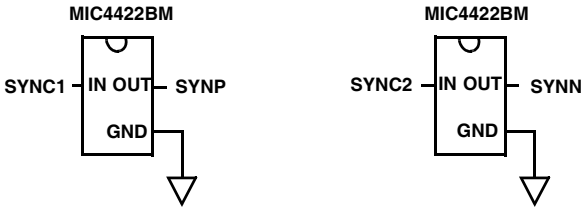


FIGURE 22B. NON-INVERTING DRIVERS

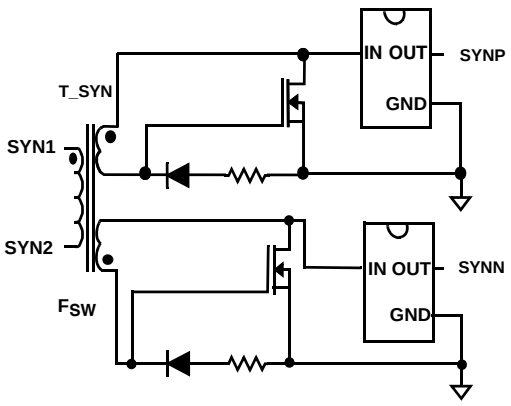


FIGURE 22C. PRIMARY CONTROL

	INVERTING	NON INVERTING
SYN1	SYNC2/LOWER1	SYNC1
SYN2	SYNC1/LOWER2	SYNC2
IC	MIC4421BM	MIC4422BM

INVERTING DRIVERS

Inverting the SYNC signals or the LOWER signals with external high current drivers to drive the synchronous FETs.

NON-INVERTING DRIVERS

Cascading SYNC signals with non-inverting high current drivers to drive the synchronous FETs. There is a dead time between SYNC1 and SYNC2. For a higher efficiency, Schottky diodes are normally in parallel with the synchronous FETs to reduce the conduction losses during the dead time in high output current applications.

PRIMARY CONTROL

This requires a pulse transformer, operating at the switching frequency, for isolation. There are three options to drive the synchronous FETs, as described in previous lines.

Primary FET Drivers

PUSH-PULL DRIVERS

Push-Pull Medium Current Drivers

Upper drivers are not used. No external drivers are required. Secondary control. Operate at the switching frequency.

Push-Pull High Current Drivers

Upper drivers are not used. External high current drivers are required and less power is dissipated in the ISL6551IREC controller. Secondary control. Operate at the switching frequency.

Push-Pull Primary Control

Upper drivers are not used. Both lower drivers can directly drive the power switches. External drivers are required in high gate capacitance applications.

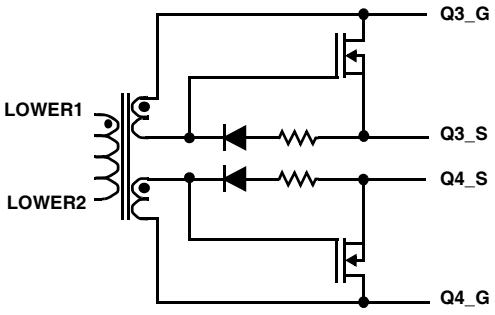


FIGURE 23A. PUSH-PULL MEDIUM CURRENT DRIVERS

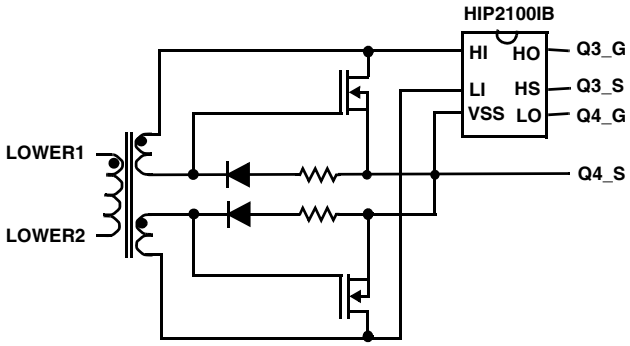


FIGURE 23B. PUSH-PULL HIGH CURRENT DRIVERS

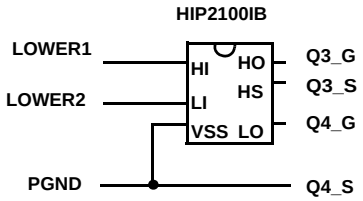


FIGURE 23C. PUSH-PULL PRIMARY CONTROL

FULL BRIDGE DRIVERS

FULL BRIDGE HIGH CURRENT DRIVERS

External high current drivers are required and less power is dissipated in the ISL6551IREC controller. Secondary control. Operate at the switching frequency.

FULL BRIDGE MEDIUM CURRENT DRIVERS

No external drivers are required. Secondary control. Operate at the switching frequency.

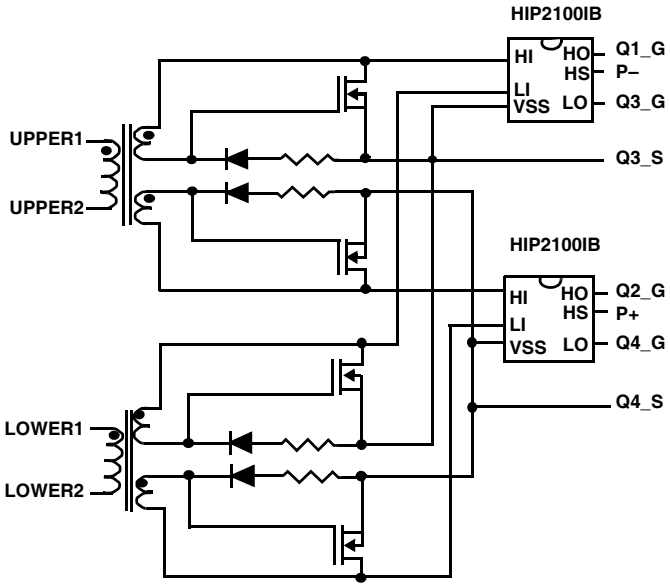


FIGURE 24A. FULL BRIDGE HIGH CURRENT DRIVERS

FULL BRIDGE PRIMARY CONTROL

Lower drivers can directly drive the power switches, while upper drivers require the assistance of level-shifting circuits such as a pulse transformer or Intersil's HIP2100 half-bridge driver. External high current drivers are not required in medium power applications, but level-shifting circuits are still required for upper drivers. Operate at the switching frequency.

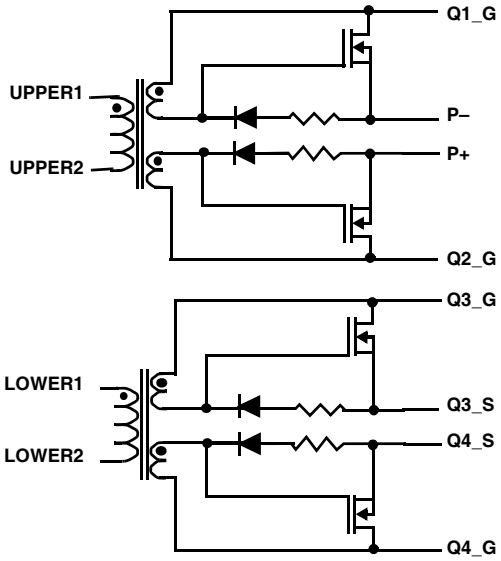


FIGURE 24B. FULL BRIDGE MEDIUM CURRENT DRIVERS

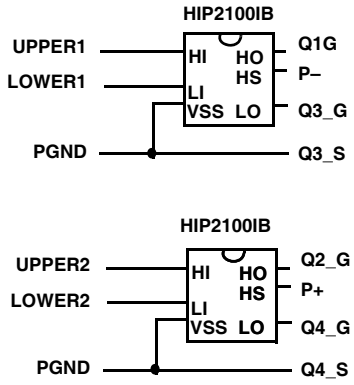
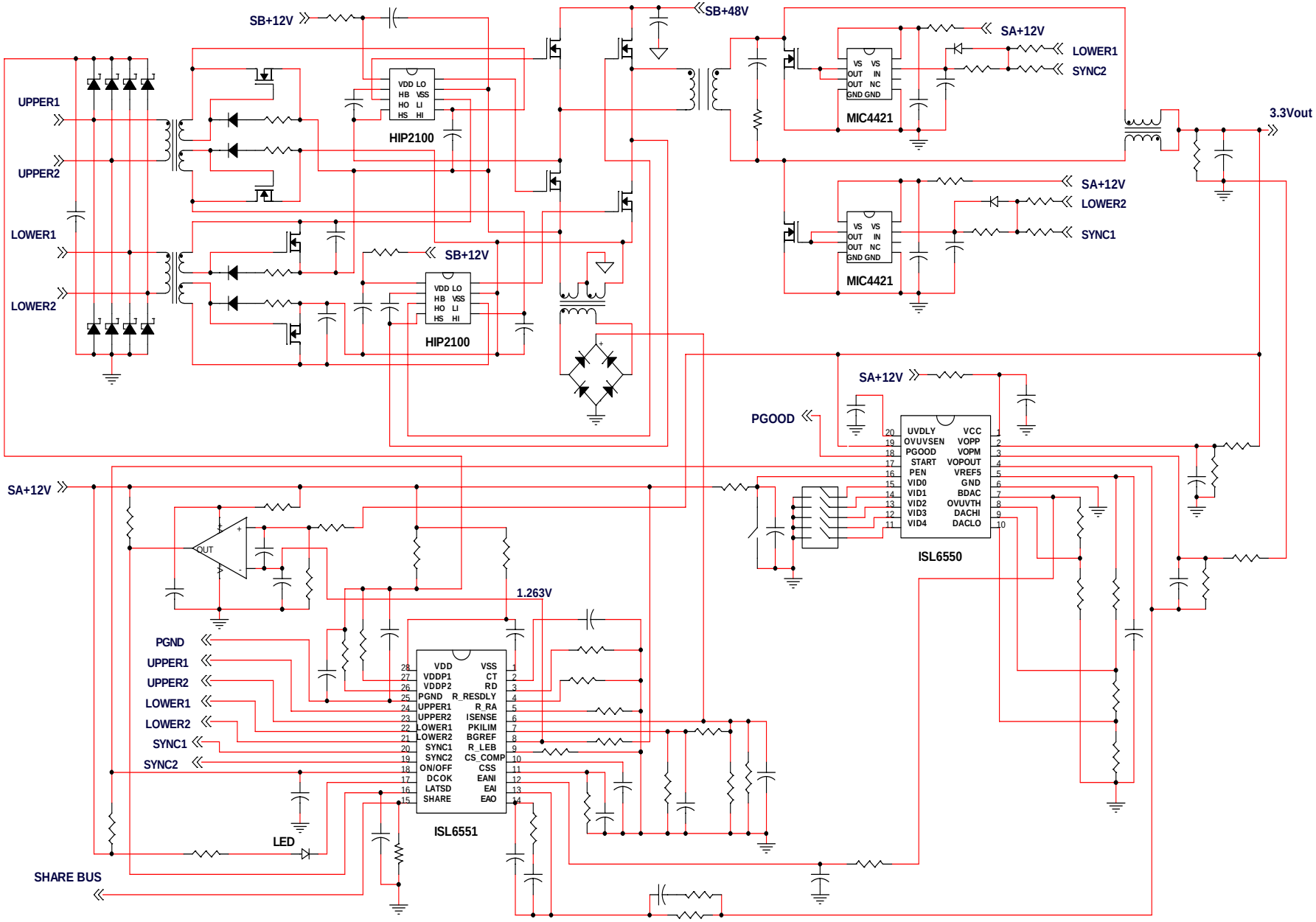


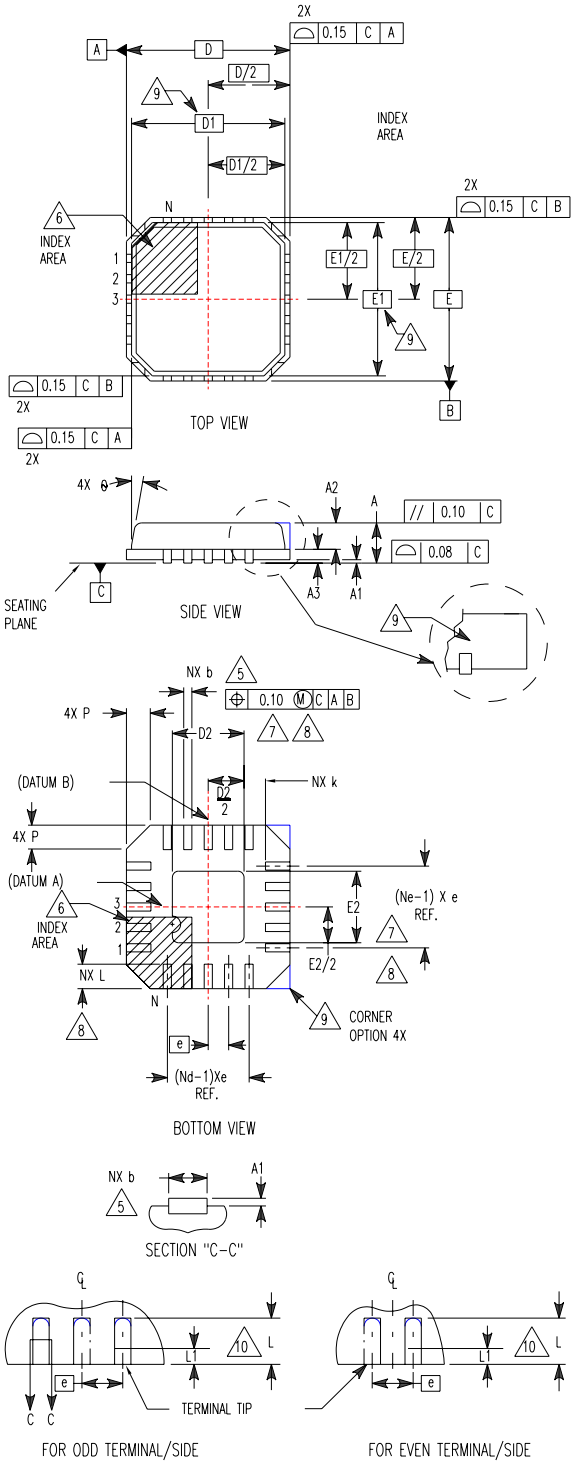
FIGURE 24C. FULL BRIDGE PRIMARY CONTROL

Simplified Typical Application Schematics



200W TELECOMMUNICATION POWER SUPPLY (SEE AN1002 FOR DETAILS)

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L28.6x6

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.95	4.10	4.25	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.95	4.10	4.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		28		2
Nd		7		3
Ne		7		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.