

### 5 Volt, Byte Alterable EEPROM

The X28HC64 is an 8K x 8 EEPROM, fabricated with Intersil's proprietary, high performance, floating gate CMOS technology. Like all Intersil programmable nonvolatile memories, the X28HC64 is a 5V only device. It features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

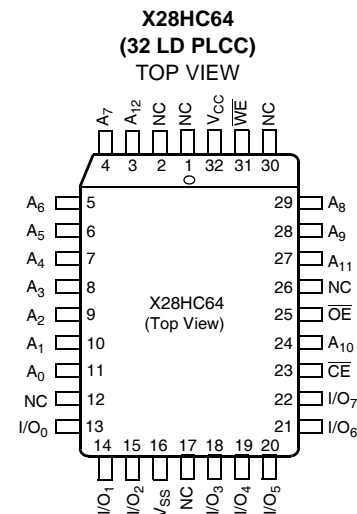
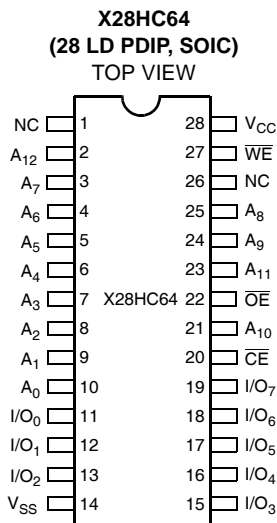
The X28HC64 supports a 64-byte page write operation, effectively providing a 32µs/byte write cycle, and enabling the entire memory to be typically written in 0.25 seconds. The X28HC64 also features DATA Polling and Toggle Bit Polling, two methods providing early end of write detection. In addition, the X28HC64 includes a user-optional software data protection mode that further enhances Intersil's hardware write protect capability.

Intersil EEPROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

### Features

- 70ns access time
- Simple byte and page write
  - Single 5V supply
  - No external high voltages or  $V_{PP}$  control circuits
  - Self-timed
  - No erase before write
  - No complex programming algorithms
  - No overerase problem
- Low power CMOS
  - 40mA active current max.
- 200µA standby current max.
- Fast write cycle times
  - 64-byte page write operation
  - Byte or page write cycle: 2ms typical
  - Complete memory rewrite: 0.25 sec. typical
  - Effective byte write cycle time: 32µs typical
- Software data protection
- End of write detection
  - DATA polling
  - Toggle bit
- High reliability
  - Endurance: 100000 cycles
  - Data retention: 100 years
- JEDEC approved byte-wide pin out
- Pb-free available (RoHS compliant)

### Pinouts



## X28HC64

### Ordering Information

PART NUMBER	PART MARKING	TEMPERATURE RANGE (°C)	ACCESS TIME (ns)	PACKAGE	PKG. DWG. #	
X28HC64J-70*	X28HC64J-70 RR	0 to +70	70	32 Ld PLCC	N32.45x55	
X28HC64JIZ-70* (Note 1)	X28HC64JI-70 ZRR	-40 to +85		32 Ld PLCC (Pb-free)	N32.45x55	
X28HC64JZ-70* (Note 1)	X28HC64J-70 ZRR	0 to +70		32 Ld PLCC (Pb-free)	N32.45x55	
X28HC64SIZ-70	X28HC64SI-70 RR	-40 to +85		28 Ld SOIC (300 mil)	M28.3	
X28HC64SZ-70 (Note 1)	X28HC64S-70 RRZ	0 to +70		28 Ld SOIC (300 mil) (Pb-free)	M28.3	
X28HC64J-90*	X28HC64J-90 RR	0 to +70		90	32 Ld PLCC	N32.45x55
X28HC64JI-90**	X28HC64JI-90 RR	-40 to +85	32 Ld PLCC		N32.45x55	
X28HC64JIZ-90* (Note 1)	X28HC64JI-90 ZRR	-40 to +85	32 Ld PLCC (Pb-free)		N32.45x55	
X28HC64P-90	X28HC64P-90 RR	0 to +70	28 Ld PDIP		E28.6	
X28HC64PI-90	X28HC64PI-90 RR	-40 to +85	28 Ld PDIP		E28.6	
X28HC64PIZ-90 (Notes 1, 2)	X28HC64PI-90 RRZ	-40 to +85	28 Ld PDIP (Pb-free)		E28.6	
X28HC64PZ-90 (Notes 1, 2)	X28HC64P-90 RRZ	0 to +70	28 Ld PDIP (Pb-free)		E28.6	
X28HC64J-12*	X28HC64J-12 RR	0 to +70	120		32 Ld PLCC	N32.45x55
X28HC64JI-12*	X28HC64JI-12 RR	-40 to +85			32 Ld PLCC	N32.45x55
X28HC64JIZ-12* (Note 1)	X28HC64JI-12 Z RR	-40 to +85			32 Ld PLCC (Pb-free)	N32.45x55
X28HC64JZ-12* (Note 1)	X28HC64J-12 RRZ	0 to +70			32 Ld PLCC (Pb-free)	N32.45x55
X28HC64P-12	X28HC64P-12 RR	0 to +70			28 Ld PDIP	E28.6
X28HC64PI-12	X28HC64PI-12 RR	-40 to +85		28 Ld PDIP	E28.6	
X28HC64PIZ-12 (Notes 1, 2)	X28HC64PI-12 RRZ	-40 to +85		28 Ld PDIP (Pb-free)	E28.6	
X28HC64PZ-12 (Notes 1, 2)	X28HC64P-12 RRZ	0 to +70		28 Ld PDIP (Pb-free)	E28.6	
X28HC64S-12*, **	X28HC64S-12 RR	0 to +70		28 Ld SOIC (300 mil)	M28.3	
X28HC64SI-12*	X28HC64SI-12 RR	-40 to +85		28 Ld SOIC (300 mil)	M28.3	
X28HC64SIZ-12* (Note 1)	X28HC64SI-12 RRZ	-40 to +85		28 Ld SOIC (300 mil) (Pb-free)	M28.3	
X28HC64SZ-12 (Note 1)	X28HC64S-12 RRZ	0 to +70		28 Ld SOIC (300 mil) (Pb-free)	M28.3	

\*Add "T1" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

\*\*\*Add "T2" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

#### NOTES:

- These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

**Pin Descriptions**

**Addresses ( $A_0$ - $A_{12}$ )**

The Address inputs select an 8-bit memory location during a read or write operation.

**Chip Enable ( $\overline{CE}$ )**

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

**Output Enable ( $\overline{OE}$ )**

The Output Enable input controls the data output buffers and is used to initiate read operations.

**Data In/Data Out ( $I/O_0$ - $I/O_7$ )**

Data is written to or read from the X28HC64 through the I/O pins.

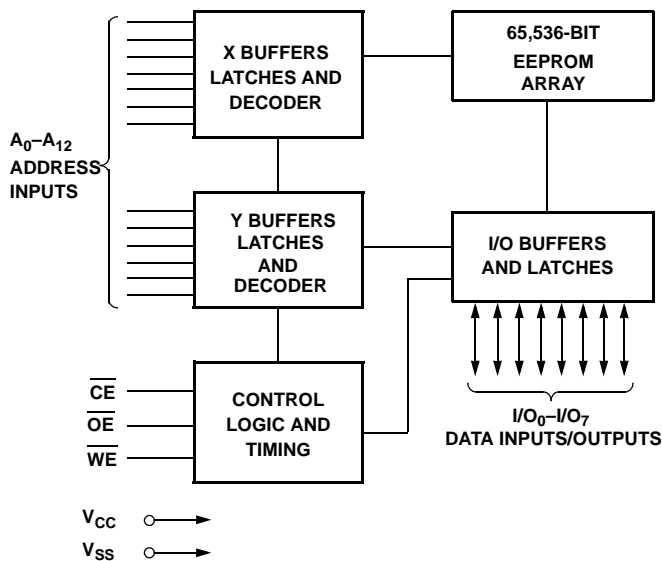
**Write Enable ( $\overline{WE}$ )**

The Write Enable input controls the writing of data to the X28HC64.

TABLE 1. PIN NAMES

SYMBOL	DESCRIPTION
$A_0$ - $A_{12}$	Address Inputs
$I/O_0$ - $I/O_7$	Data Input/Output
WE	Write Enable
CE	Chip Enable
OE	Output Enable
$V_{CC}$	+5V
$V_{SS}$	Ground
NC	No Connect

**Block Diagram**



**Device Operation**

**Read**

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

**Write**

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28HC64 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 2ms.

**Page Write Operation**

The page write feature of the X28HC64 allows the entire memory to be written in 0.25 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28HC64 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{12}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

**Write Operation Status Bits**

The X28HC64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

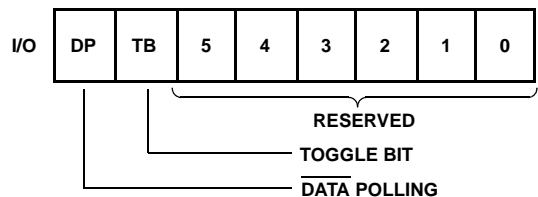


FIGURE 1. STATUS BIT ASSIGNMENT

**DATA Polling (I/O<sub>7</sub>)**

The X28HC64 features  $\overline{\text{DATA}}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{\text{DATA}}$  Polling allows a simple bit test operation to determine the status of the X28HC64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data.

**Toggle Bit (I/O<sub>6</sub>)**

The X28HC64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

**DATA Polling I/O<sub>7</sub>**

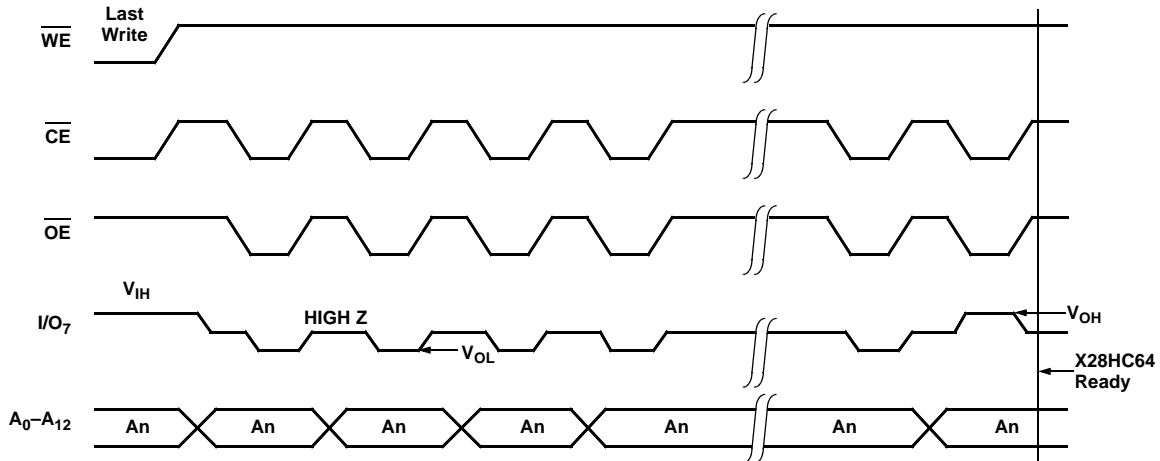
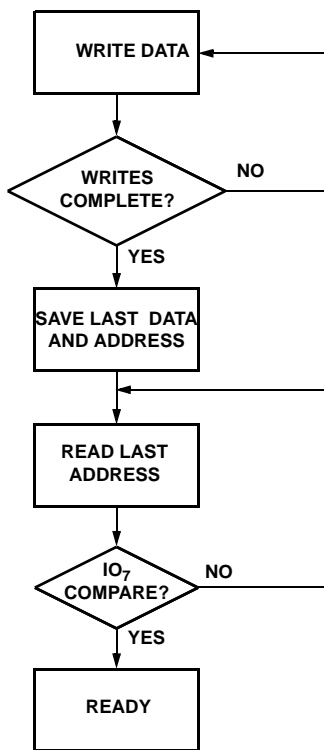


FIGURE 2. DATA POLLING BUS SEQUENCE



$\overline{\text{DATA}}$  Polling can effectively reduce the time for writing to the X28HC64. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

FIGURE 3. DATA POLLING SOFTWARE FLOW

**The Toggle Bit I/O<sub>6</sub>**

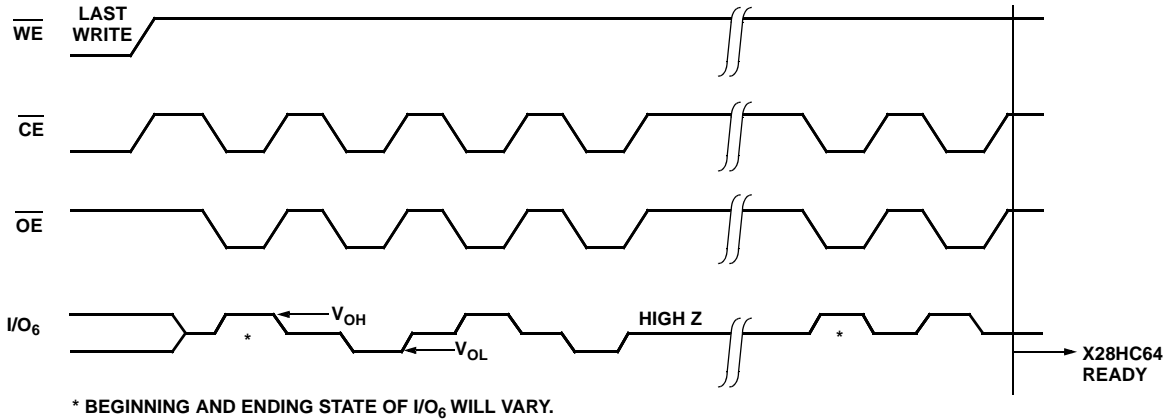


FIGURE 4. TOGGLE BIT BUS SEQUENCE

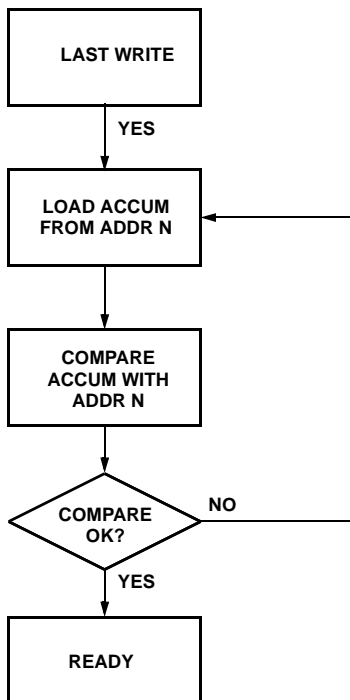


FIGURE 5. TOGGLE BIT SOFTWARE FLOW

The Toggle Bit can eliminate the chore of saving and fetching the last address and data in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28HC64 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

**Hardware Data Protection**

The X28HC64 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default V<sub>CC</sub> Sense—All write functions are inhibited when V<sub>CC</sub> is 3V typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

**Software Data Protection**

The X28HC64 offers a software controlled data protection feature. The X28HC64 is shipped from Intersil with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V<sub>CC</sub> was stable.

The X28HC64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device, unless the reset command is issued.

Once the software protection is enabled, the X28HC64 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

**Software Algorithm**

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three-byte sequence opens the page write window, enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Software Data Protection

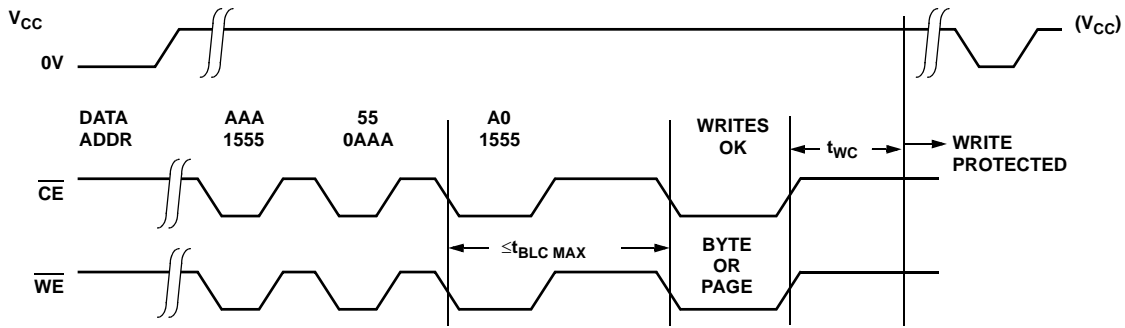


FIGURE 6. TIMING SEQUENCE—BYTE OR PAGE WRITE

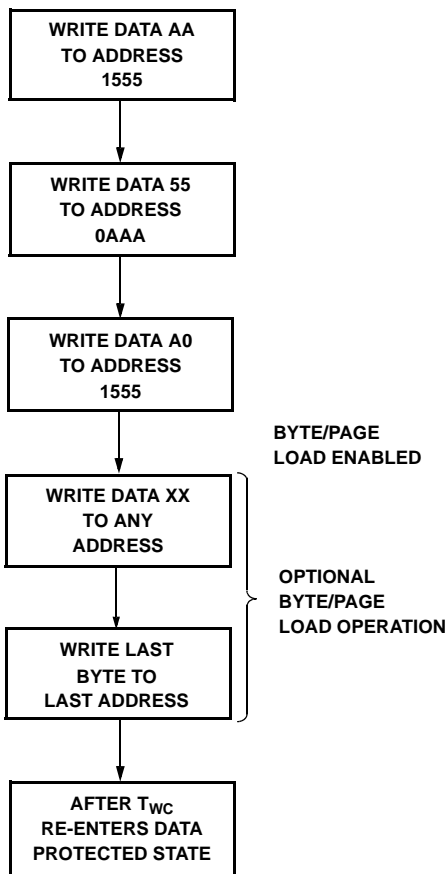
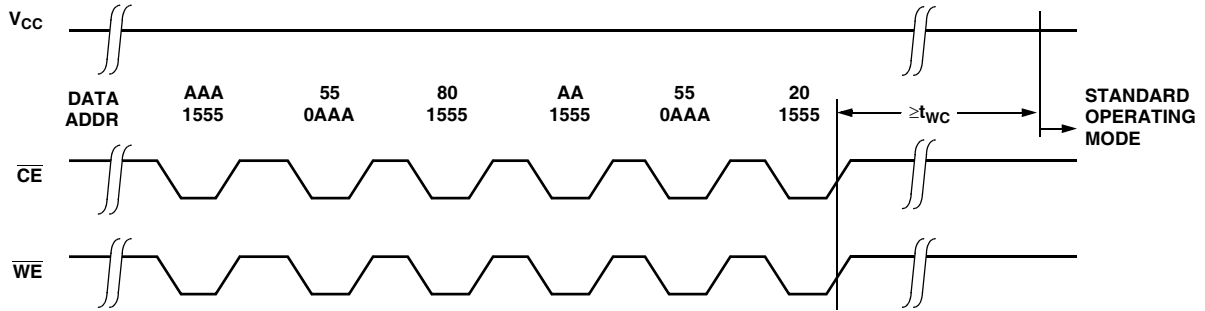


FIGURE 7. WRITE SEQUENCE FOR SOFTWARE DATA PROTECTION

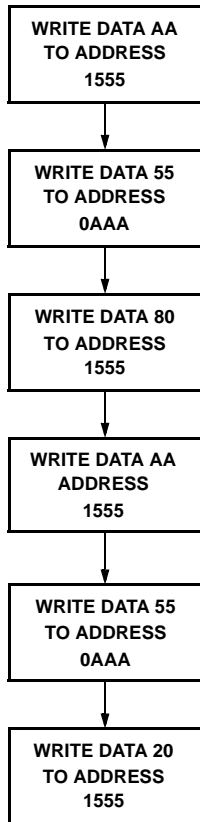
Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used, the X28HC64 will automatically disable further writes unless another command is issued to deactivate it. If no further commands are issued the X28HC64 will be write protected during power-down and after any subsequent power-up.

**Note:** Once initiated, the sequence of write operations should not be interrupted.

**Resetting Software Data Protection**



**FIGURE 8. RESET SOFTWARE DATA PROTECTION TIMING SEQUENCE**



**FIGURE 9. SOFTWARE SEQUENCE TO DEACTIVATE SOFTWARE**

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an EEPROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the X28HC64 will be in standard operating mode.

**Note:** Once initiated, the sequence of write operations should not be interrupted.

### System Considerations

Because the X28HC64 is frequently used in large memory arrays, it is provided with a two-line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation, and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that  $\overline{CE}$  be decoded from the address bus, and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation, this assures that all deselected devices are in their standby mode, and that only the selected device(s) is/are outputting data on the bus.

Because the X28HC64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 $\mu$ F high frequency ceramic capacitor be used between  $V_{CC}$  and  $V_{SS}$  at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 $\mu$ F electrolytic bulk capacitor be placed between  $V_{CC}$  and  $V_{SS}$  for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

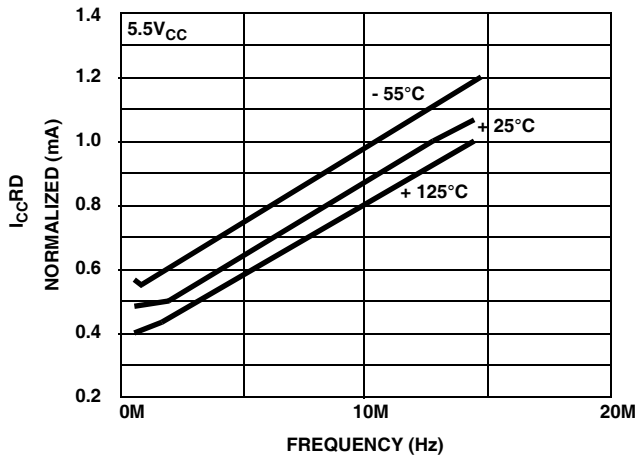


FIGURE 10. NORMALIZED  $I_{CC(RD)}$  BY TEMPERATURE OVER FREQUENCY DATA PROTECTION

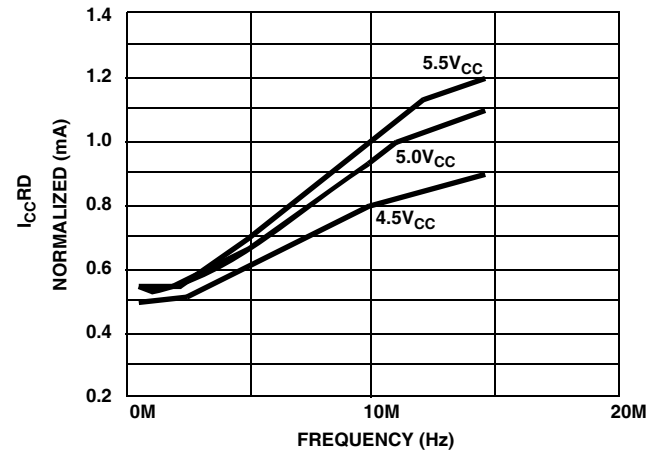


FIGURE 11. NORMALIZED  $I_{CC(RD)}$  @ 25% OVER THE  $V_{CC}$  RANGE AND FREQUENCY



# X28HC64

## Absolute Maximum Ratings

Temperature Under Bias	
X28HC64	-10°C to +85°C
X28HC64I	-65°C to +135°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to $V_{SS}$	-1V to +7V
DC Output Current	5mA

## Thermal Information

Pb-Free Reflow Profile. . . . .see link below  
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

## Recommended Operating Conditions

Commercial Temperature Range	0°C to +70°C
Industrial Temperature Range	-40°C to +85°C
Supply Voltage Range	
X28HC64	.5V ±10%

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**DC Electrical Specifications** Over recommended operating conditions, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 3)	MAX	UNIT
$V_{CC}$ Current (active) (TTL Inputs)	$I_{CC}$	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/O's = open, address inputs = TTL levels @ $f = 10$ MHz		15	40	mA
$V_{CC}$ Current (Standby) (TTL Inputs)	$I_{SB1}$	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ All I/O's = open, other inputs = $V_{IH}$		1	2	mA
$V_{CC}$ Current (Standby) (CMOS Inputs)	$I_{SB2}$	$\overline{CE} = V_{CC} - 0.3V$ , $\overline{OE} = GND$ , All I/O's = open, other inputs = $V_{CC} - 0.3V$		100	200	µA
Input Leakage Current	$I_{LI}$	$V_{IN} = V_{SS}$ to $V_{CC}$			±10	µA
Output Leakage Current	$I_{LO}$	$V_{OUT} = V_{SS}$ to $V_{CC}$ , $\overline{CE} = V_{IH}$			±10	µA
Input LOW Voltage (Note 4)	$V_{IL}$		-1		0.8	V
Input HIGH Voltage (Note 4)	$V_{IH}$		2		$V_{CC} + 1$	V
Output LOW Voltage	$V_{OL}$	$I_{OL} = 5mA$			0.4	V
Output HIGH Voltage	$V_{OH}$	$I_{OH} = -5mA$	2.4			V

**NOTES:**

3. Typical values are for  $T_A = +25^\circ C$  and nominal supply voltage
4.  $V_{IL}$  min. and  $V_{IH}$  max. are for reference only and are not tested.

**Endurance and Data Retention** Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	MIN	MAX	UNIT
Minimum Endurance	100,000		Cycles
Data Retention	100		Years

**Power-up Timing** Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TYP (Note 3)	UNIT
Power-up to Read Operation (Note 5)	$t_{PUR}$	100	$\mu s$
Power-up to Write Operation (Note 5)	$t_{PUW}$	5	ms

**Capacitance**  $T_A = +25^\circ C, f = 1MHz, V_{CC} = 5V$

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Input/output Capacitance (Note 5)	$C_{I/O}$	$V_{I/O} = 0V$	10	$\mu F$
Input Capacitance (Note 5)	$C_{IN}$	$V_{IN} = 0V$	6	$\mu F$

NOTE:

5. This parameter is periodically sampled and not 100% tested.

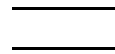




TABLE 2. AC CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

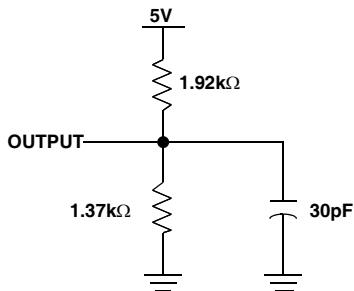
TABLE 3. MODE SELECTION

CE	OE	WE	MODE	I/O	POWER
L	L	H	Read	$D_{OUT}$	Active
L	H	L	Write	$D_{IN}$	Active
H	X	X	Standby and write inhibit	High Z	Standby
X	L	X	Write inhibit	—	—
X	X	H	Write inhibit	—	—

**Symbol Table**

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**Equivalent AC Load Circuits**



**AC Electrical Specifications**

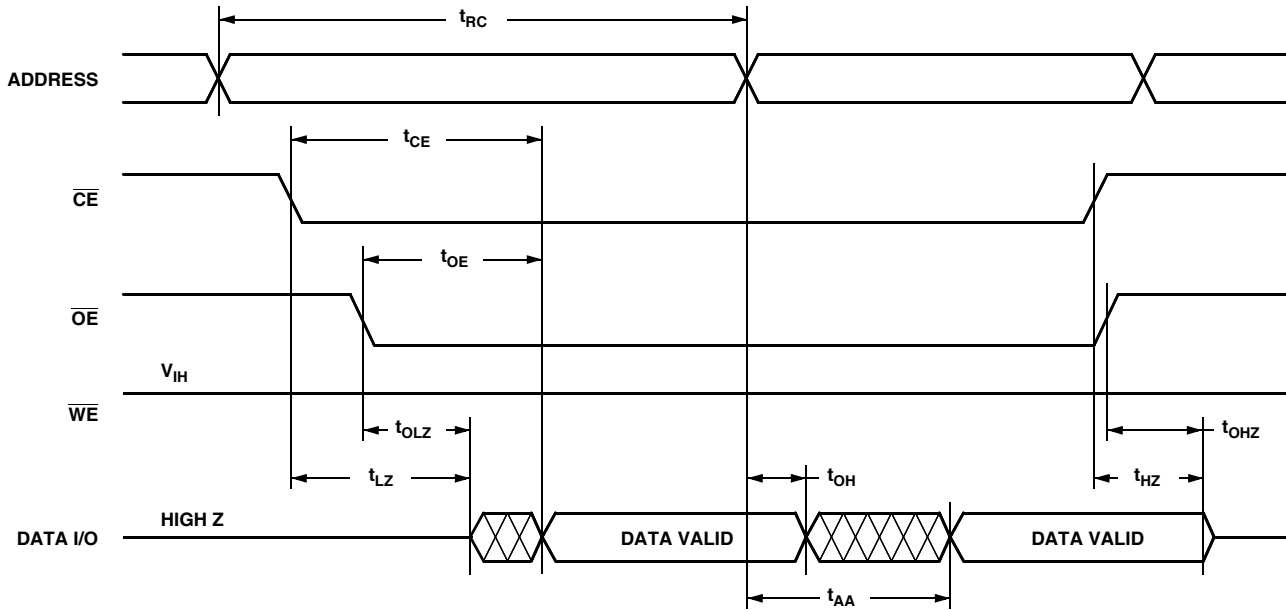
**Read Cycle Limits** Over the recommended operating conditions unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	X28HC64-70		X28HC64-90		X28HC64-12		UNIT
		-55°C TO +125°C		-55°C TO +125°C		-55°C TO +125°C		
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	$t_{RC}$	70		90		120		ns
Chip Enable Access Time	$t_{CE}$		70		90		120	ns
Address Access Time	$t_{AA}$		70		90		120	ns
Output Enable Access Time	$t_{OE}$		35		40		50	ns
$\overline{CE}$ LOW to Active Output (Note 6)	$t_{LZ}$	0		0		0		ns
$\overline{OE}$ LOW to Active Output (Note 6)	$t_{OLZ}$	0		0		0		ns
$\overline{CE}$ HIGH to High Z Output (Note 6)	$t_{HZ}$		30		30		30	ns
$\overline{OE}$ HIGH to High Z Output (Note 6)	$t_{OHZ}$		30		30		30	ns
Output Hold from Address Change	$t_{OH}$	0		0		0		ns

NOTE:

- $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured from the point when  $\overline{CE}$  or  $\overline{OE}$  return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

**Read Cycle**



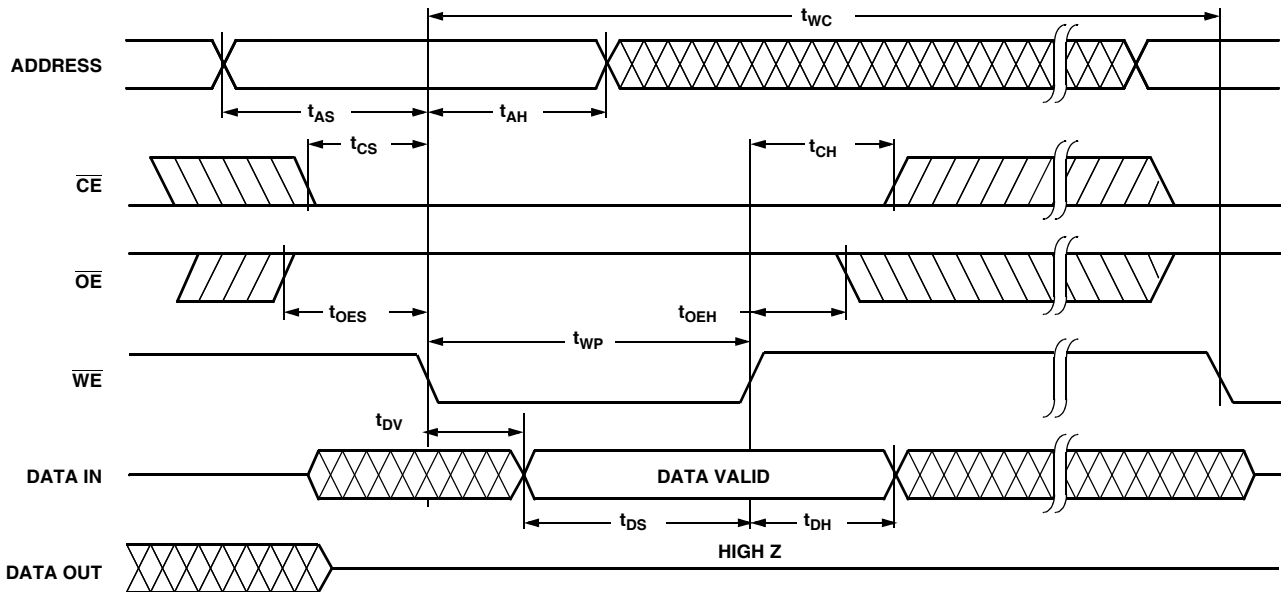
**Write Cycle Limits** Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	MIN	TYP (Note 3)	MAX	UNIT
Write Cycle Time (Note 7)	$t_{WC}$		2	5	ms
Address Setup Time	$t_{AS}$	0			ns
Address Hold Time	$t_{AH}$	50			ns
Write Setup Time	$t_{CS}$	0			ns
Write Hold Time	$t_{CH}$	0			ns
$\overline{CE}$ Pulse Width	$t_{CW}$	50			ns
$\overline{OE}$ High Setup Time	$t_{OES}$	0			ns
$\overline{OE}$ High Hold Time	$t_{OEH}$	0			ns
$\overline{WE}$ Pulse Width	$t_{WP}$	50			ns
$\overline{WE}$ HIGH Recovery (Note 8)	$t_{WPH}$	50			ns
Data Valid (Note 8)	$t_{DV}$			1	$\mu$ s
Data Setup	$t_{DS}$	50			ns
Data Hold	$t_{DH}$	0			ns
Delay to Next Write (Note 8)	$t_{DW}$	10			$\mu$ s
Byte Load Cycle	$t_{BLC}$	0.15		100	$\mu$ s

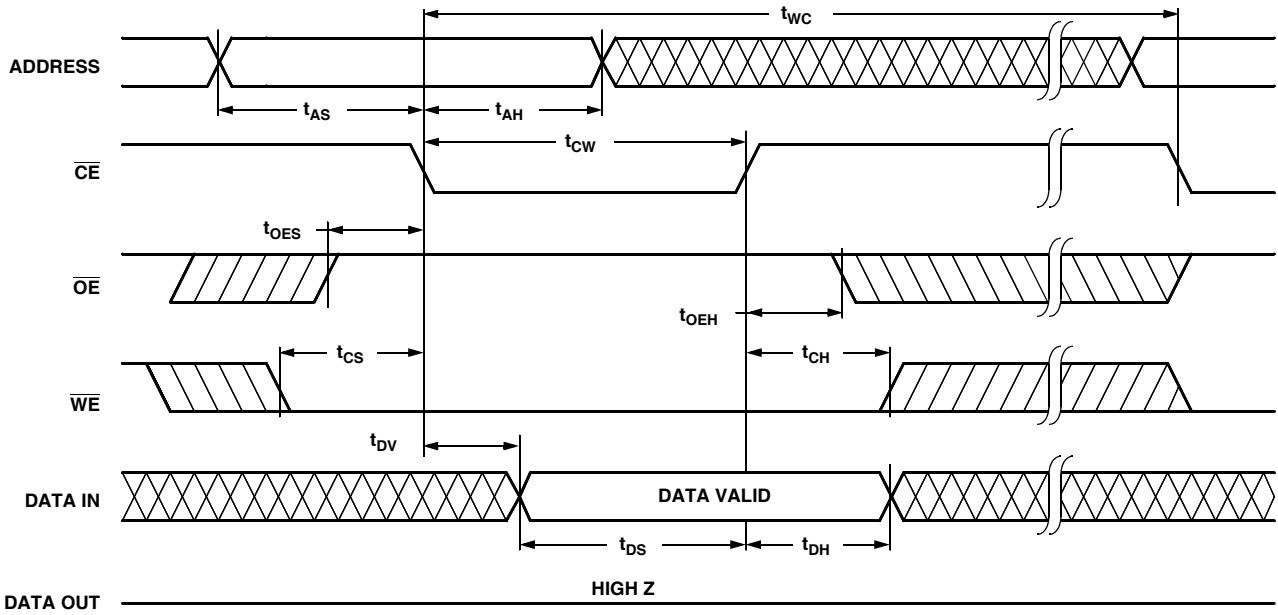
NOTES:

- 7.  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
- 8.  $t_{WPH}$  and  $t_{DW}$  are periodically sampled and not 100% tested.

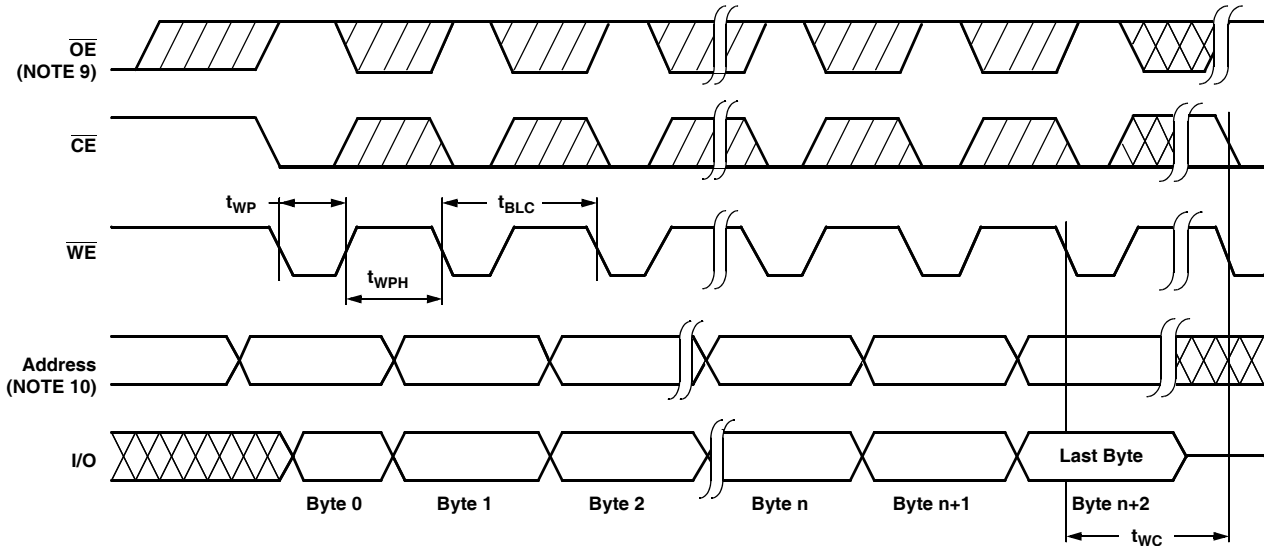
**$\overline{WE}$  Controlled Write Cycle**



**$\overline{CE}$  Controlled Write Cycle**



**Page Write Cycle**

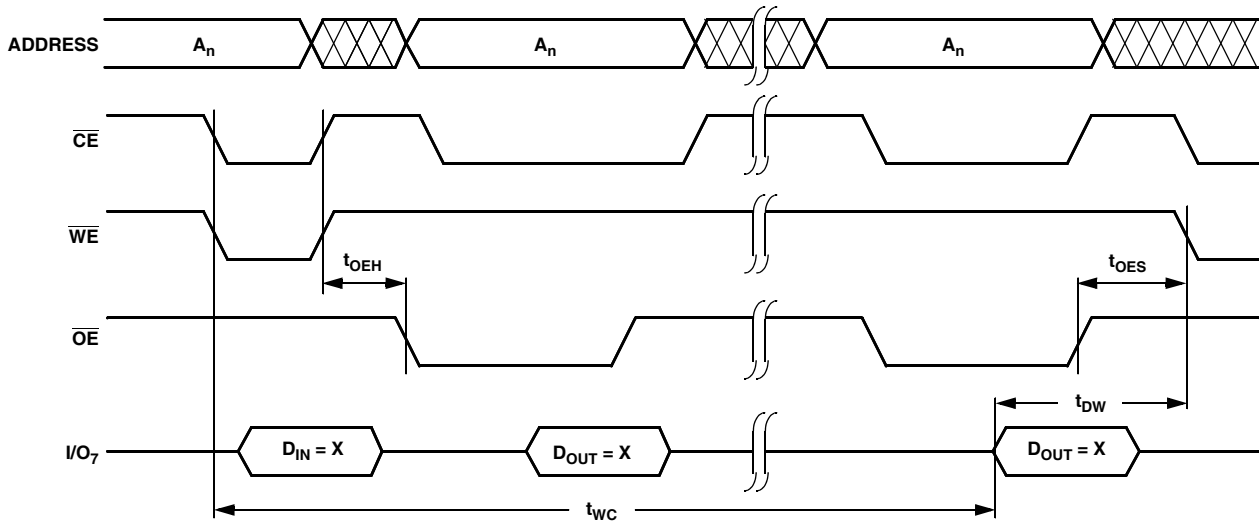


\*For each successive write within the page write operation,  $A_6-A_{12}$  should be the same or writes to an unknown address could occur.

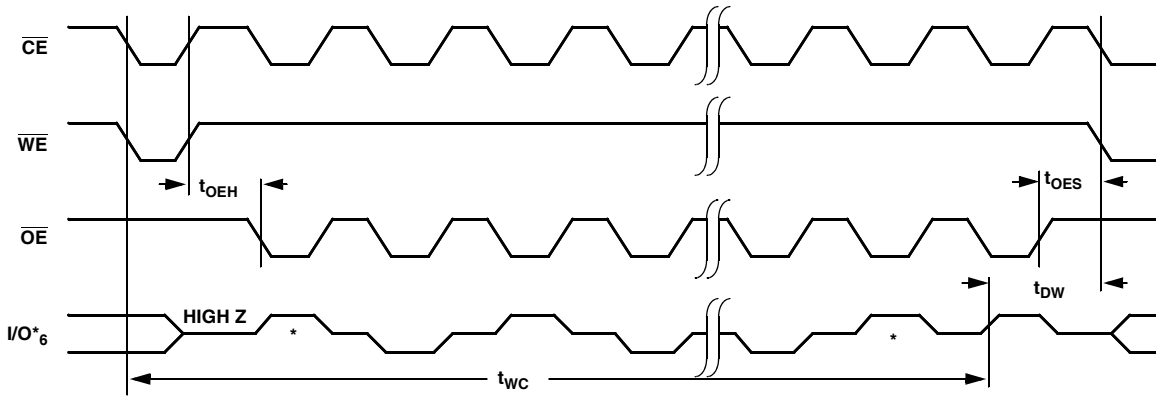
NOTES:

9. Between successive byte writes within a page write operation,  $\overline{OE}$  can be strobed LOW: e.g. this can be done with  $\overline{CE}$  and  $\overline{WE}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{WE}$  HIGH and  $\overline{CE}$  LOW effectively performing a polling operation.
10. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{CE}$  or  $\overline{WE}$  controlled write cycle timing.

**DATA Polling Timing Diagram (Note 11)**



**Toggle Bit Timing Diagram (Note 11)**

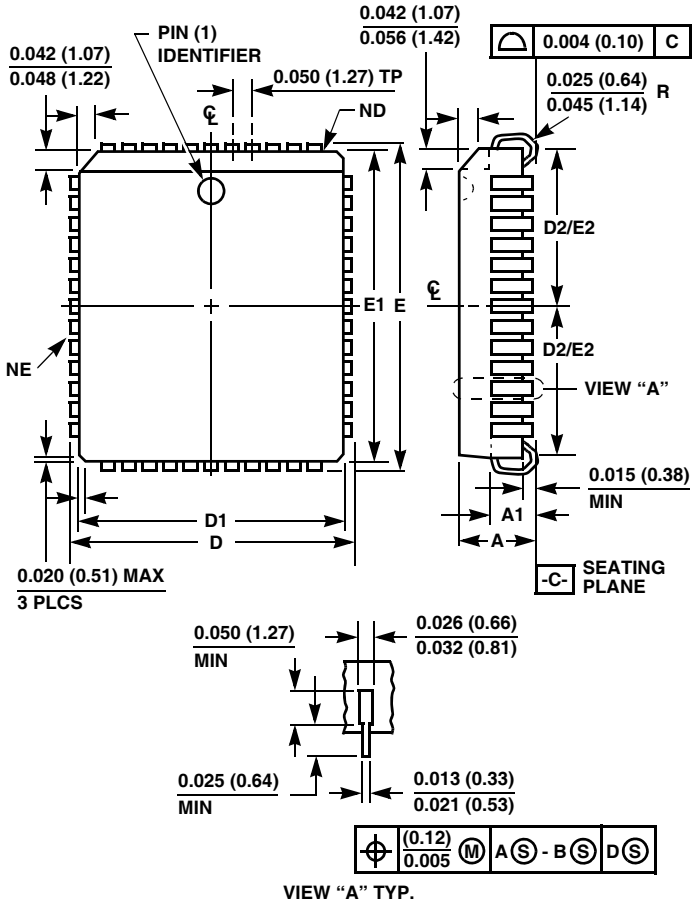


\*  $I/O_6$  beginning and ending state will vary, depending upon actual  $t_{WC}$ .

NOTE:

11. Polling operations are by definition read cycles and are therefore subject to read cycle timings.

Plastic Leaded Chip Carrier Packages (PLCC)



N32.45x55 (JEDEC MS-016AE ISSUE A)  
32 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

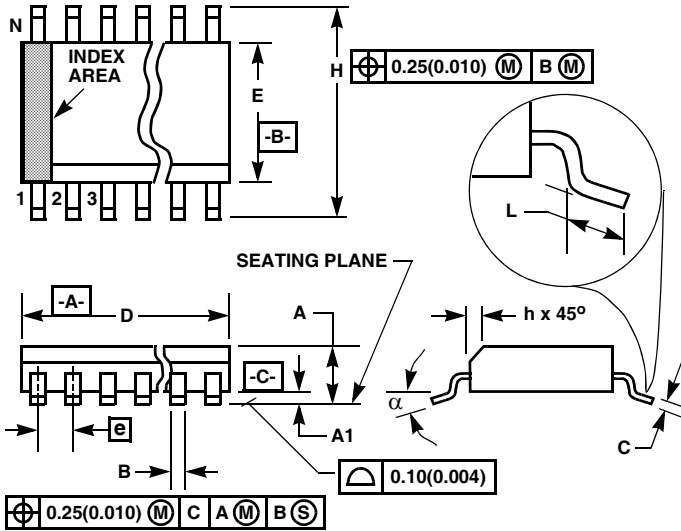
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.125	0.140	3.18	3.55	-
A1	0.060	0.095	1.53	2.41	-
D	0.485	0.495	12.32	12.57	-
D1	0.447	0.453	11.36	11.50	3
D2	0.188	0.223	4.78	5.66	4, 5
E	0.585	0.595	14.86	15.11	-
E1	0.547	0.553	13.90	14.04	3
E2	0.238	0.273	6.05	6.93	4, 5
N	28		28		6
ND	7		7		7
NE	9		9		7

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane [-C-] contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.
7. ND denotes the number of leads on the two shorts sides of the package, one of which contains pin #1. NE denotes the number of leads on the two long sides of the package.

Small Outline Plastic Packages (SOIC)



**M28.3 (JEDEC MS-013-AE ISSUE C)**  
**28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
$\alpha$	0°	8°	0°	8°	-

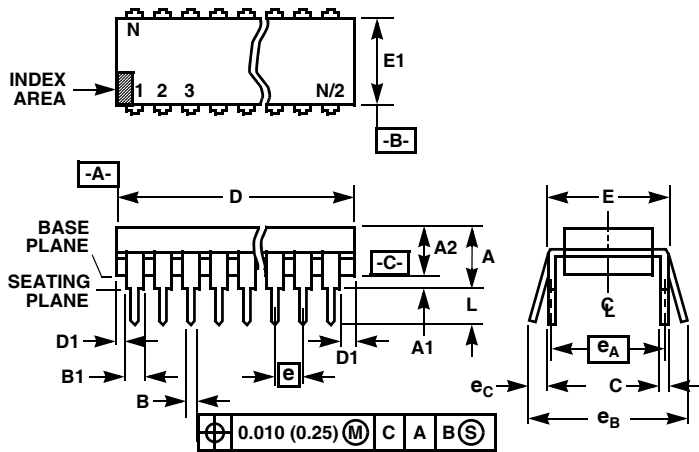
NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)  
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.600 BSC		15.24 BSC		6
$e_B$	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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