High Frequency 100mA CMOS Charge Pump, Inverter/Doubler

FEATURES

- Converts V+ to V- or V+ to 2V+
- Low output resistance, 10Ω max.
- High power efficiency
- Selectable charge pump frequency of 25kHz or 135kHz; optimize capacitor size.
- Low quiescent current
- Pin-compatible to MAX660, LTC660 with higher frequency operation
- Available in 8-pin SOIC andDIP packages
- Lead-free, halogen-free package option

APPLICATIONS

- Negative voltage generator
- Voltage doubler
- Voltage splitter
- Low EMI power source
- GaAs FET biasing
- Lithium battery power supply
- Instrumentation
- LCD contrast bias
- Cellular phones, pagers

DESCRIPTION

The CAT661 is a charge-pump voltage converter. It can invert a positive input voltage to a negative output. Only two external capacitors are needed. With a guaranteed 100mA output current capability, the CAT661 can replace a switching regulator and its inductor. Lower EMI is achieved due to the absence of an inductor.

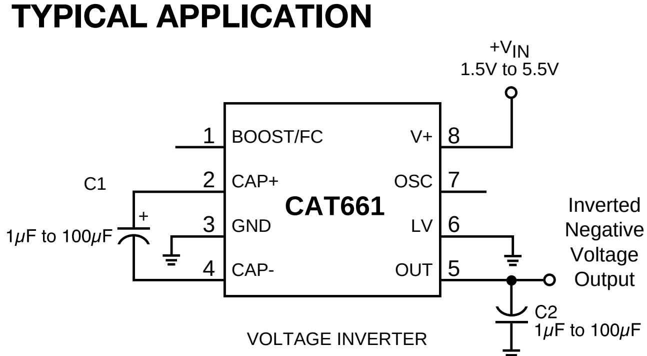
In addition, the CAT661 can double a voltage supplied from a battery or power supply. Inputs from 2.5V to 5.5V will yield a doubled, 5V to 11V output.

A Frequency Control pin (BOOST/FC) is provided to select either a high (typically 135kHz) or low (25kHz) internal oscillator frequency, thus allowing quiescent current vs. capacitor size trade-offs to be made. The 135kHz frequency is selected when the FC pin is connected to V+. The operating frequency can also be adjusted with an external capacitor at the OSC pin or by driving OSC with an external clock.

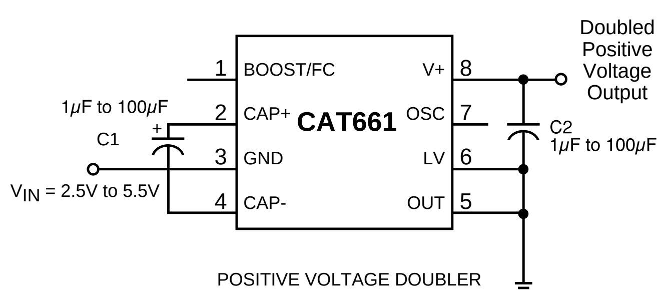
Both 8-pin DIP and SO packages are available. For die availability, contact Catalyst Semiconductor marketing.

The CAT661 can replace the MAX660 and the LTC660 in applications where higher oscillator frequency and smaller capacitors are needed. In addition, the CAT661 is pin compatible with the 7660/1044, offering an easy upgrade for applications with 100mA loads.

TYPICAL APPLICATION



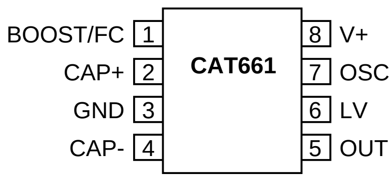
VOLTAGE INVERTER



POSITIVE VOLTAGE DOUBLER

PIN CONFIGURATION

SOIC 8-Lead (V)
PDIP 8-Lead (L)



(Top View)

PIN DESCRIPTIONS

		Circuit Configu		
Pin Number	**Name**	**Inverter**		
1	Boost/FC	Freqency Control for the internal oscillator. With an external oscillator BOOST/FC has no effect.		Same as inverter.
		Boost/FC	**Oscillator Frequency**	**Oscillator Frequency**
		Open	25kHz typical, 10kHz minimum	40kHz typical
		V+	135kHz typical, 80kHz minimum	135kHz typical, 40kHz minimum
2	CAP+	Charge Pump Capacitor. Positive terminal.		Same as inverter.
3	GND	Power Supply Ground.		Power supply. Positive voltage input.
4	CAP-	Charge pump capacitor. Negative terminal.		Same as inverter.
5	OUT	Output for negative voltage.		Power supply ground.
6	LV	Low-Voltage selection pin. When the input voltage is less than 3V, connect LV to GND. For input voltages above 3V, LV may be connected to GND or left open. If OSC is driven externally, connect LV to GND.		LV must be tied to OUT for all input voltages.
7	OSC	Oscillator control input. An external capacitor can be connected to lower the oscillator frequency. An external oscillator can drive OSC and set the chip operating frequency. The charge-pump frequency is one-half the frequency at OSC.		Same as inverter. Do not overdrive OSC in doubling mode. Standard logic levels will not be suitable. See the applications section for additional information.
8	V+	Power supply. Positive voltage input.		Positive voltage output.

ORDERING INFORMATION

Part Number	Package	Quanity	Package Marking
CAT661ELA	PDIP, 8-lead	50/tube	661ELA
CAT661EVA	SOIC	100/tube	661EVA
CAT661EVA-T3	SOIC	3,000/reel	661EVA

Note: All packages are RoHS compliant.

ABSOLUTE MAXIMUM RATINGS

V+ to GND 6V

Input Voltage (Pins 1, 6 and 7) .. -0.3V to (V+ + 0.3V)

BOOST/FC and OSC Input Voltage .... The least negative of (Out - 0.3V) or (V+ - 6V) to (V+ + 0.3V)

Output Short-circuit Duration to GND .... 1 sec.

(OUT may be shorted to GND for 1 sec without damage but shorting OUT to V+ should be avoided.)

Continuous Power Dissipation (T_A = 70°C)
- Plastic DIP 730mW
- SO 500mW
- TDFN 1W

Storage Temperature .... -65°C to 160°C
Lead Soldering Temperature (10 sec) .... 300°C
ESD Rating-Human Body Model 2000V

Note: T_A = Ambient Temperature

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolongued time periods may affect device reliability. All voltages are with respect to ground.

Operating Ambient Temperature Ranges

CAT661E .... -40°C to 85°C

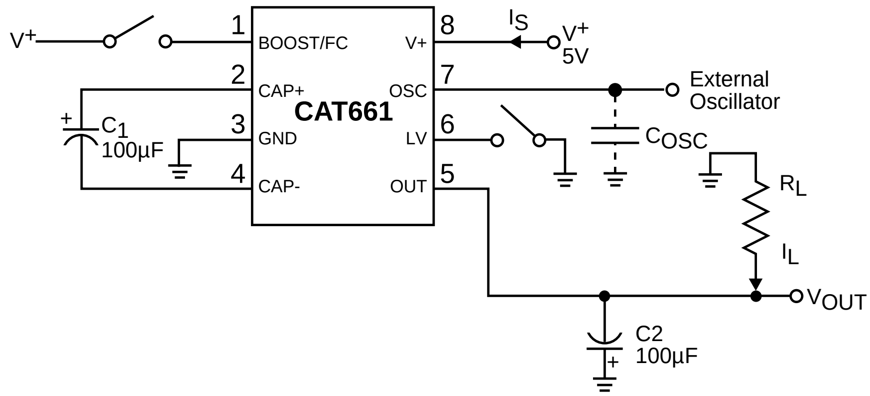
ELECTRICAL CHARACTERISTICS

V+ = 5V, C1 = C2 = 100µF, Boost/FC = Open, C_{OSC} = 0pF, and Test Circuit is Figure 1 unless otherwise noted. Temperature is T_A = T_{AMIN} to T_{AMAX} unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units
Supply Voltage	VS	Inverter: LV = Open. R_L = 1kΩ	3.0		5.5	V
		Inverter: LV = GND. R_L = 1kΩ	1.5		5.5	
		Doubler: LV = OUT. R_L = 1kΩ	2.5		5.5	
Supply Current	IS	BOOST/FC = open, LV = Open		0.2	0.5	mA
		BOOST/FC = V+ , LV = Open		1	3	
Output Current	IOUT	OUT is more negative than -4V	100			mA
Output Resistance	RO	C1 = C2 = 10µF, BOOST/FC = V+ (C1, C2 ESR ≤ 0.5Ω)		3.5	10	Ω
		C1 = C2 = 100µF (Note 2)		3.5	10	
Oscillator Frequency (Note 3)	FOSC	BOOST/FC = Open	10	25		kHz
		BOOST/FC = V+	80	135		
OSC Input Current	IOSC	BOOST/FC = Open BOOST/FC = V+		±2 ±10		µA
Power Efficiency	PE	R_L = 1kΩ connected between V+ and OUT, T_A = 25°C (Doubler)	96	98		%
		R_L = 500Ω connected between GND and OUT, T_A = 25°C (Inverter)	92	96		
		I_L = 100mA to GND, T_A = 25°C (Inverter)		88		
Voltage Conversion Efficiency	VEFF	No load, T_A = 25°C	99	99.9		%

1. In Figure 1, test circuit electrolytic capacitors C1 and C2 are 100µF and have 0.2Ω maximum ESR. Higher ESR levels may reduce efficiency and output voltage.
2. The output resistance is a combination of the internal switch resistance and the external capacitor ESR. For maximum voltage and efficiency keep external capacitor ESR under 0.2Ω.
3. FOSC is tested with C_{OSC} = 100pF to minimize test fixture loading. The test is correlated back to C_{OSC}=0pF to simulate the capacitance at OSC when the device is inserted into a test socket without an external C_{OSC}.

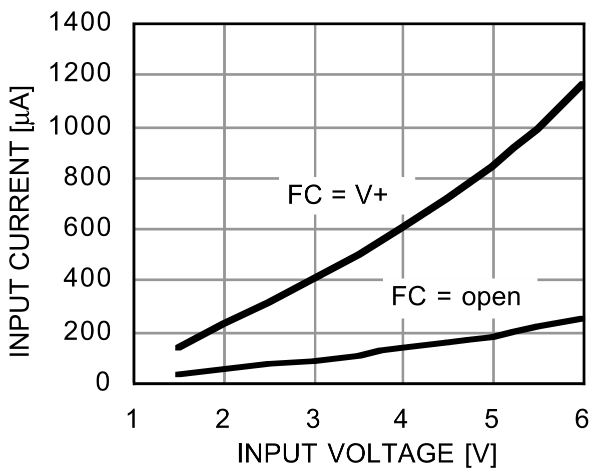
Figure 1. Test Circuit Voltage Inverter



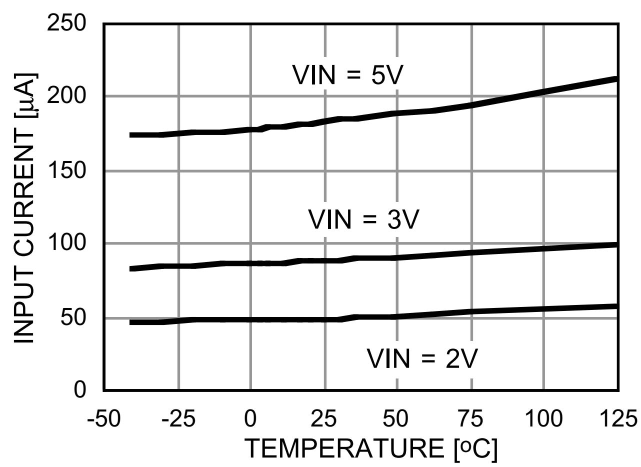
TYPICAL OPERATING CHARACTERISTICS

Typical characteristic curves are generated using the circuit in Figure 1. Inverter test conditions are: V+ 5V, LV = GND, BOOST/FC = Open and T_A = 25˚C unless otherwise indicated. Note that the charge-pump frequency is one-half the oscillator frequency.

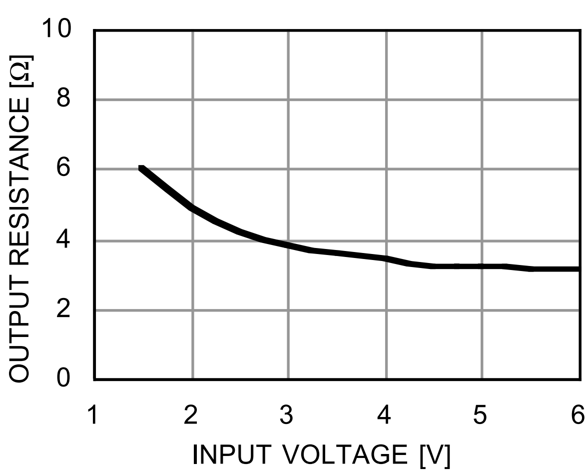
Supply Current vs. Input Voltage



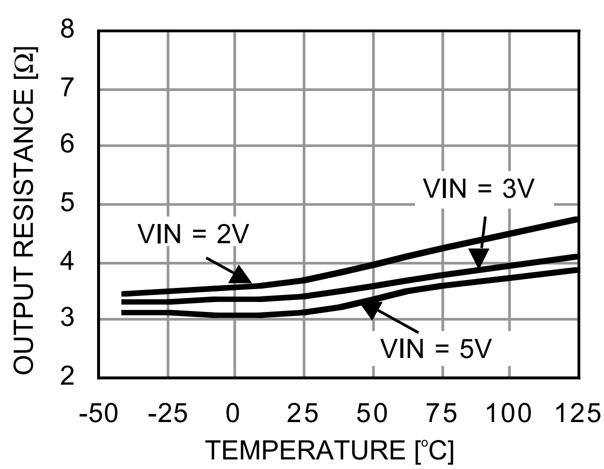
Supply Current vs. Temperature (No Load)



Output Resistance vs. Input Voltage

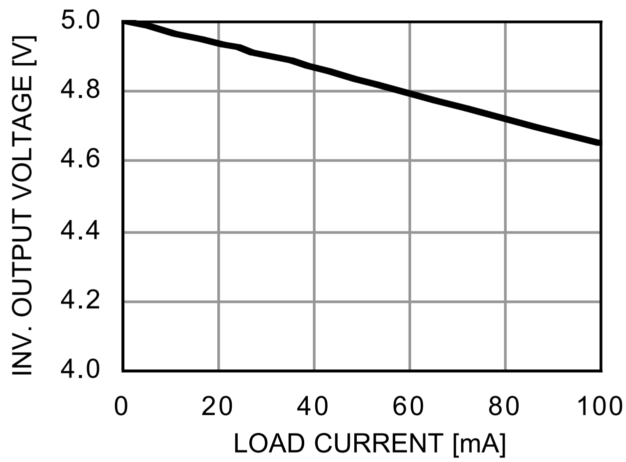


Output Resistance vs. Temperature (50Ω load)

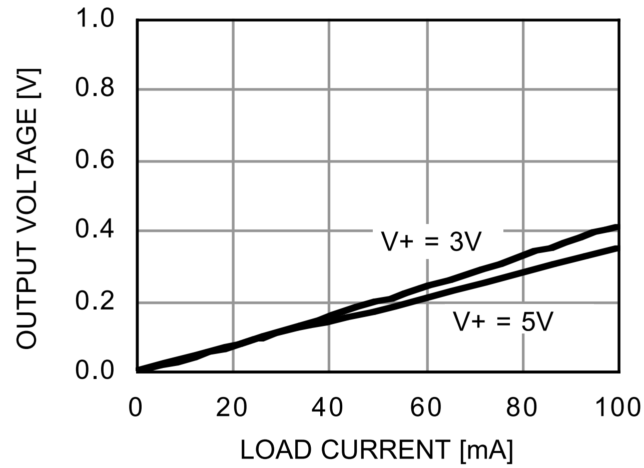


TYPICAL OPERATING CHARACTERISTICS

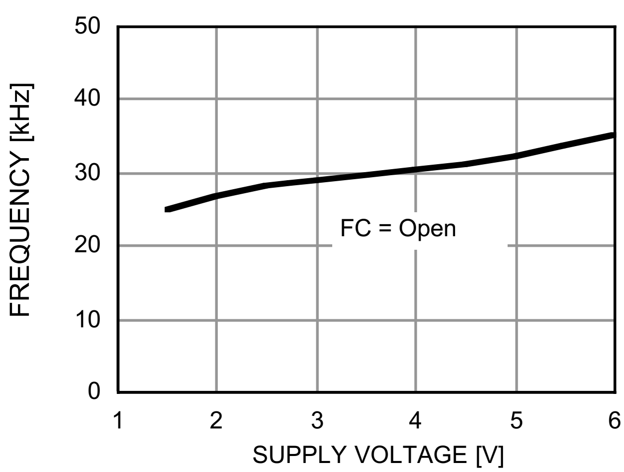
Inverted Output voltage vs. Load, V+ = 5V



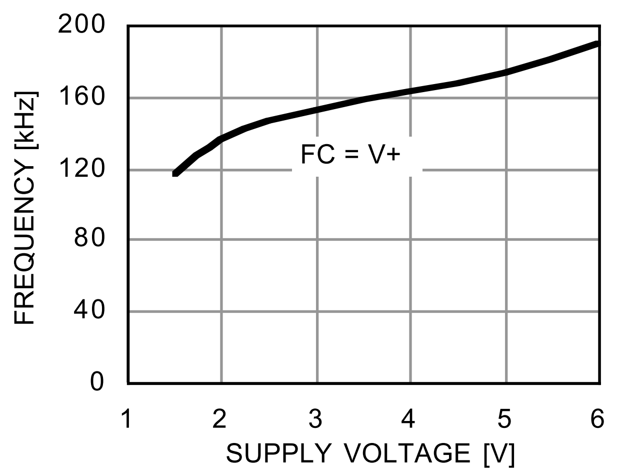
Output Voltage Drop vs. Load Current



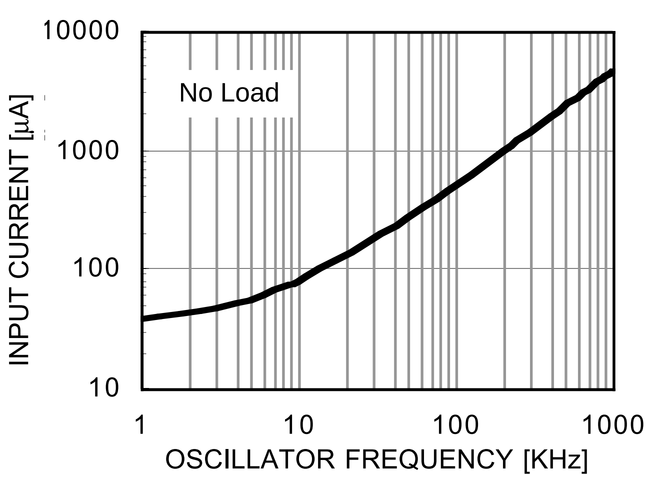
Oscillator Frequency vs. Supply Voltage



Oscillator Frequency vs. Supply Voltage



Supply Current vs. Oscillator Frequency



Efficiency vs. Load Current

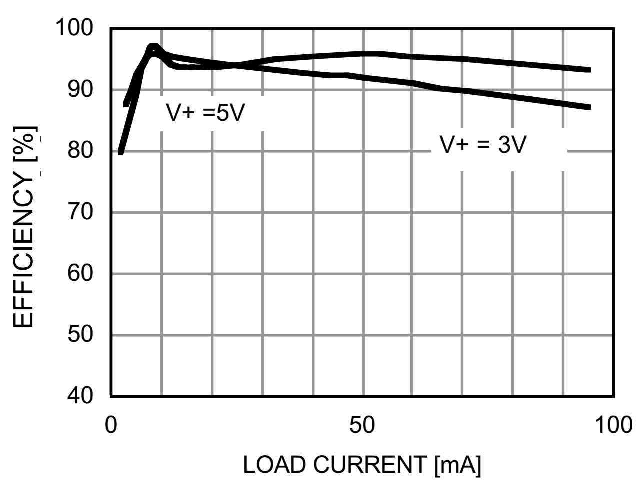
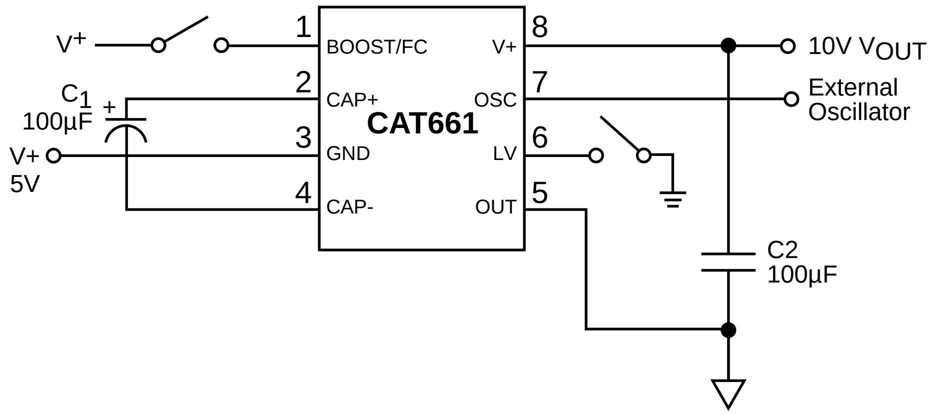


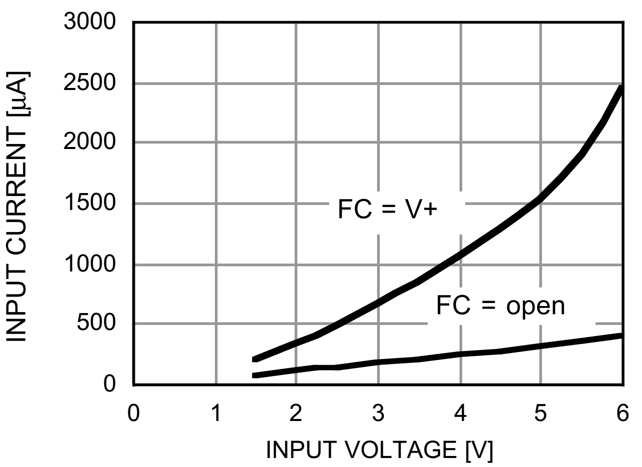
Figure 2. Test Circuit Voltage Doubler



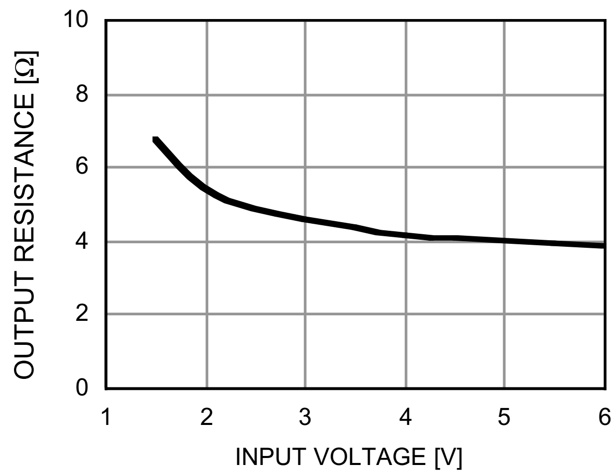
TYPICAL OPERATING CHARACTERISTICS

Typical characteristic curves are generated using the circuit in Figure 2. Doubler test conditions are: V+ 5V, LV = GND, BOOST/FC = Open and T_A = 25˚C unless otherwise indicated.

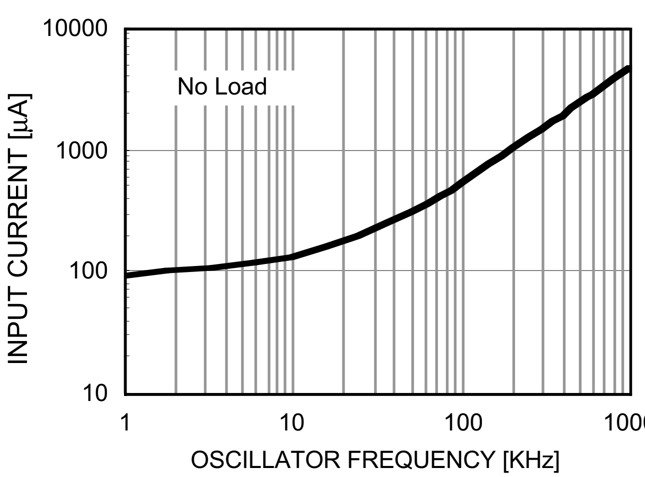
Supply Current vs. Input Voltage (No Load)



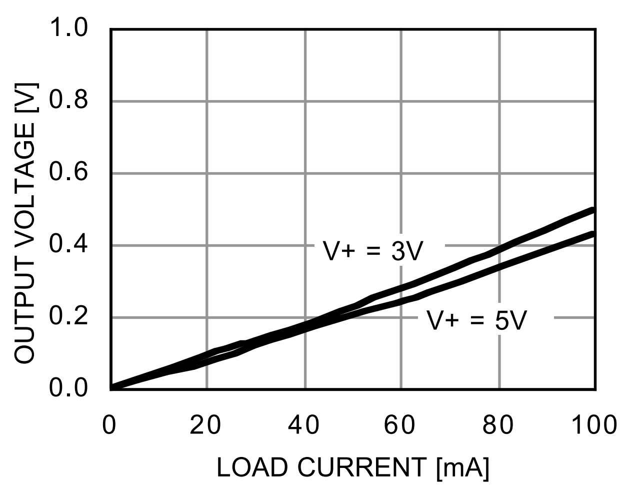
Output Resistance vs. Input Voltage



Supply Current vs. Oscillator Frequency



Output Voltage Drop vs. Load Current



APPLICATION INFORMATION

Circuit Description and Operating Theory

The CAT661 switches capacitors to invert or double an input voltage.

Figure 3 shows a simple switch capacitor circuit. In position 1 capacitor C1 is charged to voltage V1. The total charge on C1 is Q1 = C1V1. When the switch moves to position 2, the input capacitor C1 is discharged to voltage V2. After discharge, the charge on C1 is Q2 = C1V2.

The charge transferred is:

$$\Delta Q = Q1 - Q2 = C1 \times (V1 - V2)$$

If the switch is cycled "F" times per second, the current (charge transfer per unit time) is:

$$I = F \times \Delta Q = F \times C1\ (V1 - V2)$$

Rearranging in terms of impedance:

$$I = \frac{(V1-V2)}{(1/FC1)} = \frac{V1-V2}{REQ}$$

The 1/FC1 term can be modeled as an equivalent impedance REQ. A simple equivalent circuit is shown in figure 4. This circuit does not include the switch resistance nor does it include output voltage ripple. It does allow one to understand the switch-capacitor topology and make prudent engineering tradeoffs.

For example, power conversion efficiency is set by the output impedance, which consists of REQ and switch resistance. As switching frequency is decreased, REQ, the 1/FC1 term, will dominate the output impedance, causing higher voltage losses and decreased efficiency. As the frequency is increased quiescent current increases. At high frequency this current becomes significant and the power efficiency degrades.

The oscillator is designed to operate where voltage losses are a minimum. With external 150µF capacitors, the internal switch resistances and the Equivalent Series Resistance (ESR) of the external capacitors determine the effective output impedance.

A block diagram of the CAT661 is shown in figure 5.

Figure 3. Switched-Capacitor Building Block

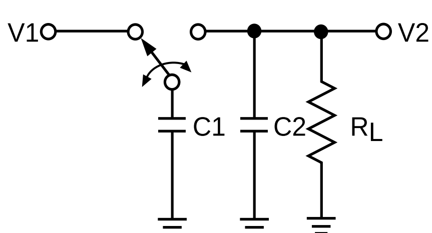
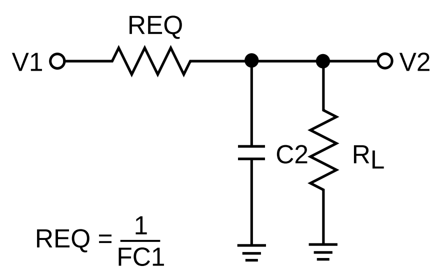


Figure 4. Switched-Capacitor Equivalent Circuit



OSCILLATOR FREQUENCY CONTROL

The switching frequency can be raised, lowered or driven from an external source. Figure 6 shows a functional diagram of the oscillator circuit.

The CAT661 oscillator has four control modes:

BOOST/FC Pin Connection	OSC Pin Connection	Nominal Oscillator Frequency
Open	Open	25kHz
BOOST/FC= V+	Open	135kHz
Open or BOOST/FC= V+	External Capacitor	—
Open	External Clock	Frequency of external clock

If BOOST/FC and OSC are left floating (Open), the nominal oscillator frequency is 25kHz. The pump frequency is one-half the oscillator frequency.

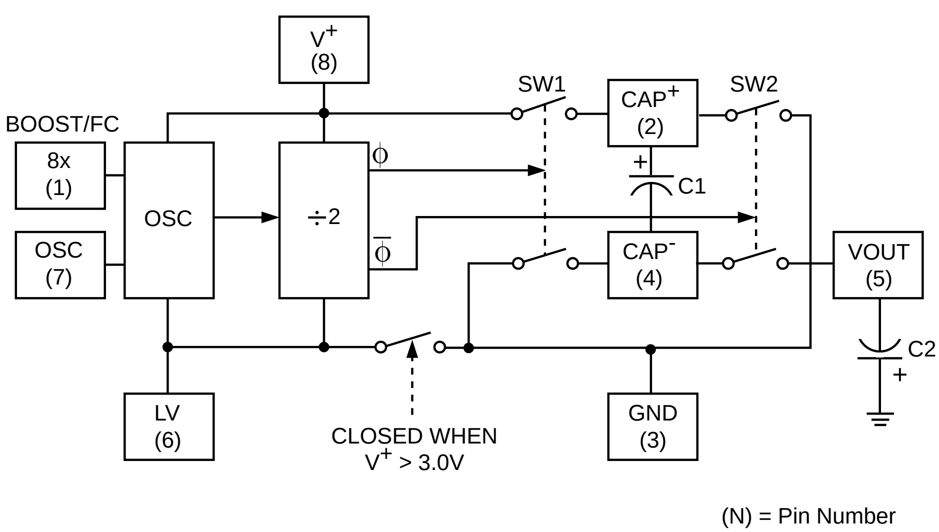
By connecting the BOOST/FC pin to V+, the charge and discharge currents are increased, and the frequency is increased by approximately 6 times. Increasing the frequency will decrease the output impedance and ripple currents. This can be an advantage at high load currents. Increasing the frequency raises quiescent current but allows smaller capacitance values for C1 and C2.

If pin 7, OSC, is loaded with an external capacitor the frequency is lowered. By using the BOOST/FC pin and an external capacitor at OSC, the operating frequency can be set.

Note that the frequency appearing at CAP+ or CAP- is one-half that of the oscillator.

Driving the CAT661 from an external frequency source can be easily achieved by driving Pin 7 and leaving the BOOST pin open, as shown in figure 6. The output current from Pin 7 is small, typically 1µA to 8µA, so a CMOS can drive the OSC pin. For 5V applications, a TTL logic gate can be used if an external 100kΩ pull-up resistor is used as shown in figure 7.

Figure 5. CAT661 Block Diagram



CAPACITOR SELECTION

Low ESR capacitors are necessary to minimize voltage losses, especially at high load currents. The exact values of C1 and C2 are not critical but low ESR capacitors are necessary.

The ESR of capacitor C1, the pump capacitor, can have a pronounced effect on the output. C1 currents are approximately twice the output current and losses occur on both the charge and discharge cycle. The ESR effects are thus multiplied by four. A 0.5Ω ESR for C1 will have the same effect as a 2Ω increase in CAT661 output impedance.

Output voltage ripple is determined by the value of C2 and the load current. C2 is charged and discharged at a current roughly equal to the load current. The internal switching frequency is one-half the oscillator frequency.

VRIPPLE = IOUT/(FOSC x C2) + IOUT x ESRC2

For example, with a 25kHz oscillator frequency (12.5kHz switching frequency), a 150µF C2 capacitor with an ESR of 0.2Ω and a 100mA load peak-to-peak the ripple voltage is 45mV.

VRIPPLE vs. FOSC

VRIPPLE (mV)	IOUT (mA)	FOSC (kHz)	C2 (µF)	C2 ESR (Ω)
45	100	25	150	0.2
25	100	135	150	0.2

Figure 6. Oscillator

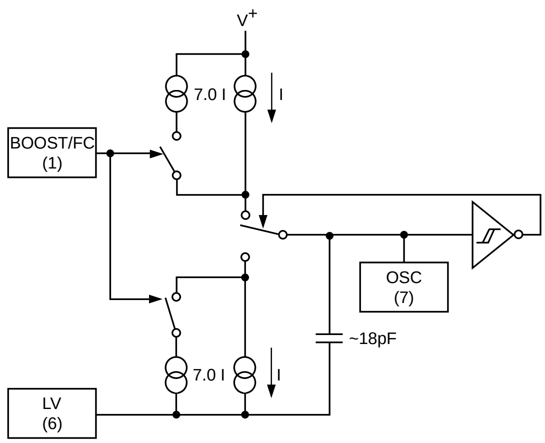
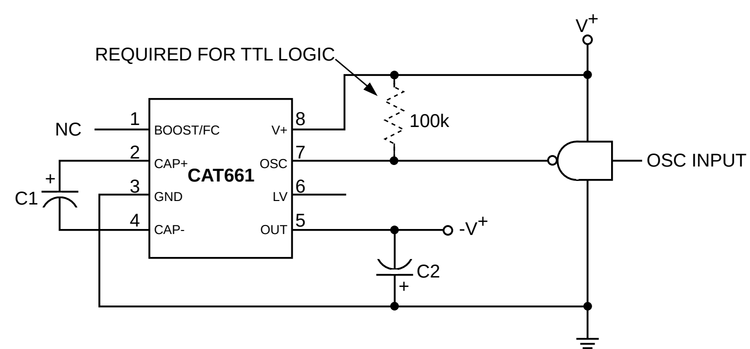


Figure 7. External Clocking



CAPACITOR SUPPLIERS

The following manufacturers supply low-ESR capacitors:

Manufacturer	Capacitor Type	Phone	WEB	Email	Comments
AVX/Kyocera	TPS/TPS3	843-448-9411	www.avxcorp.com	avx@avxcorp.com	Tantalum
Vishay/Sprague	595	402-563-6866	www.vishay.com	—	Aluminum
Sanyo	MV-AX, UGX	619-661-6835	www.sanyo.com	Svcsales@sanyo.com	Aluminum
Nichicon	F55	847-843-7500	www.nichicon-us.com	—	Tantalum
	HC/HD				Aluminum

Capacitor manufacturers continually introduce new series and offer different package styles. It is recommended that before a design is finalized capacitor manufacturers should be surveyed for their latest product offerings.

CONTROLLING LOSS IN CAT661 APPLICATIONS

There are three primary sources of voltage loss:

1. Output resistance
   VLOSS = ILOAD x ROUT, where ROUT is the CAT661 output resistance and ILOAD is the load current.
2. Charge pump (C1) capacitor ESR:
   VLOSSC1 ≈ 4 x ESRC1 x ILOAD, where ESRC1 is the ESR of capacitor C1.
3. Output or reservoir (C2) capacitor ESR:
   VLOSSC2 = ESRC2 x ILOAD, where ESRC2 is the ESR of capacitor C2.

Increasing the value of C2 and/or decreasing its ESR will reduce noise and ripple.

The effective output impedance of a CAT661 circuit is approximately:

Rcircuit ≈ Rout 661 + (4 x ESRC1) + ESRC2

VOLTAGE INVERSION POSITIVE-TO-NEGATIVE

The CAT661 easily provides a negative supply voltage from a positive supply in the system. Figure 8 shows a typical circuit. The LV pin may be left floating for positive input voltages at or above 3.3V.

TYPICAL APPLICATIONS

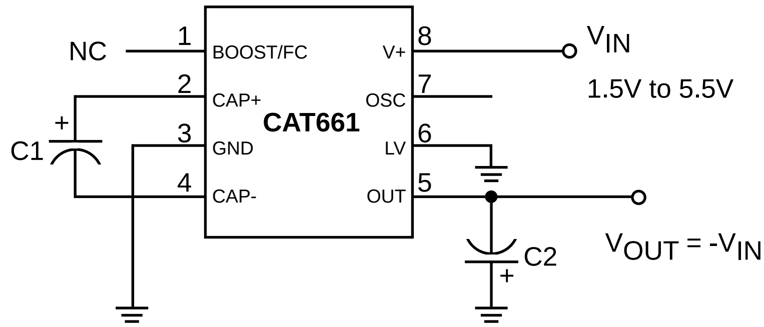


Figure 8: Voltage Inverter

POSITIVE VOLTAGE DOUBLER

The voltage doubler circuit shown in figure 9 gives VOUT = 2 x VIN for input voltages from 2.5V to 5.5V.

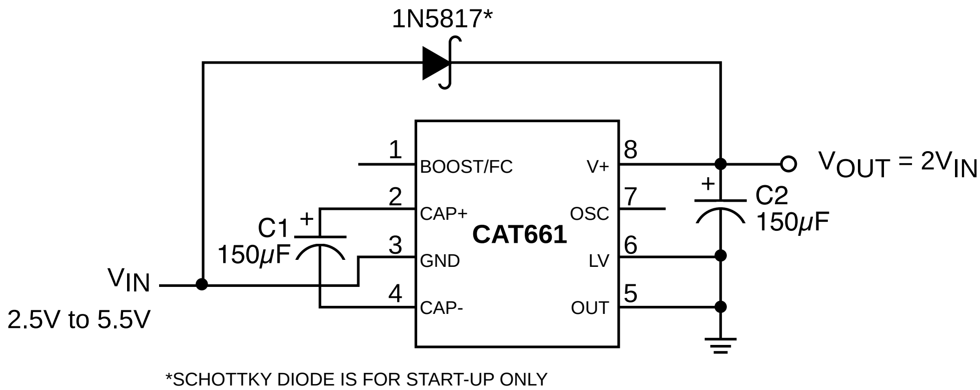


Figure 9: Voltage Doubler

PRECISION VOLTAGE DIVIDER

A precision voltage divider is shown in figure 10. With load currents under 100nA, the voltage at pin 2 will be within 0.002% of V+/2 .

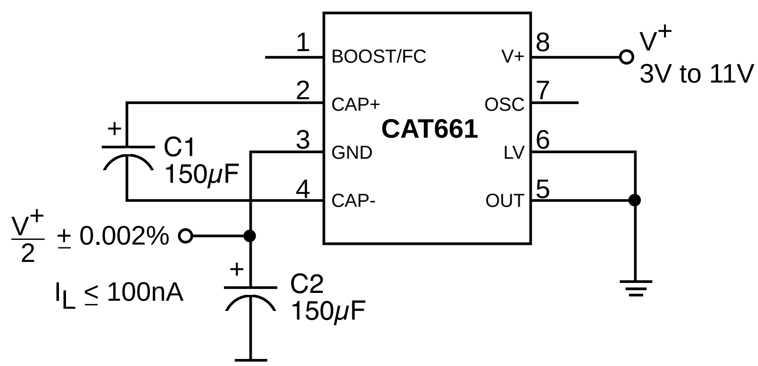


Figure 10: Precision Voltage Divider (Load ≤ 100nA)

BATTERY VOLTAGE SPLITTER

Positive and negative voltages that track each other can be obtained from a battery. Figure 11 shows how a 9V battery can provide symmetrical positive and negative voltages equal to one-half the battery voltage.

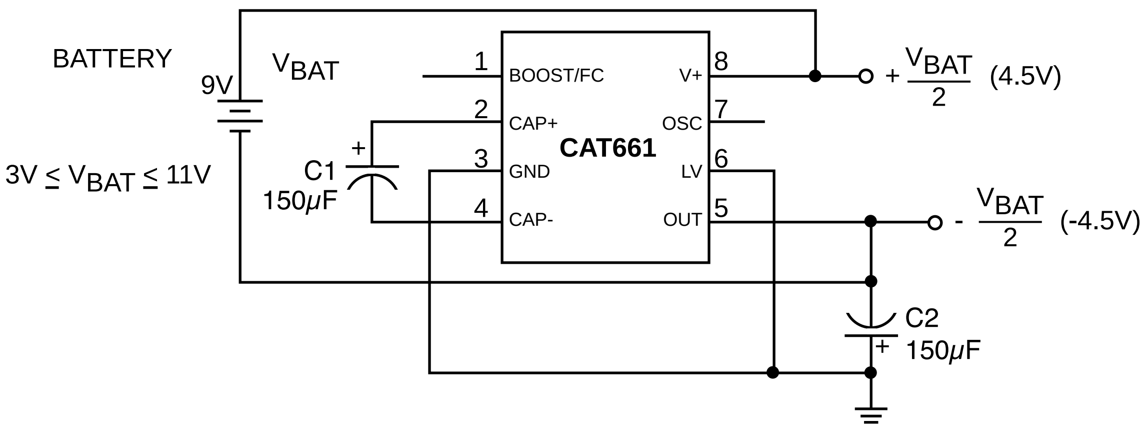


Figure 11: Battery Splitter

CASCADE OPERATION FOR HIGHER NEGATIVE VOLTAGES

The CAT661 can be cascaded as shown in figure 12 to generate more negative voltage levels. The output resistance is approximately the sum of the individual CAT661 output resistance.

V_{OUT}= -N x V_{IN}, where N represents the number of cascaded devices.

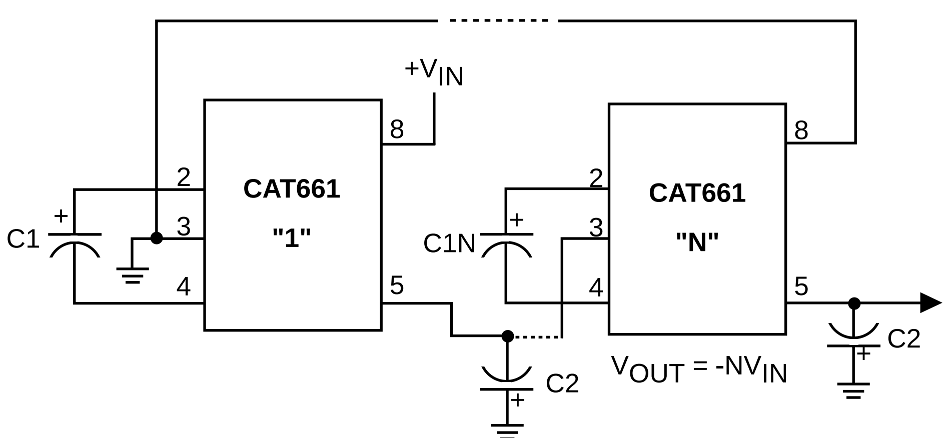


Figure 12: Cascading to Increase Output Voltage

PARALLEL OPERATION

Paralleling CAT661 devices will lower output resistance. As shown in figure 13, each device requires its own pump capacitor, C2, but the output reservoir capacitor is shared with all devices. The value of C2 should be increased by a factor of N, where N is the number of devices.

$$\text{ROUT} = \frac{\text{ROUT (of CAT661)}}{\text{N (NUMBER OF DEVICES)}}$$

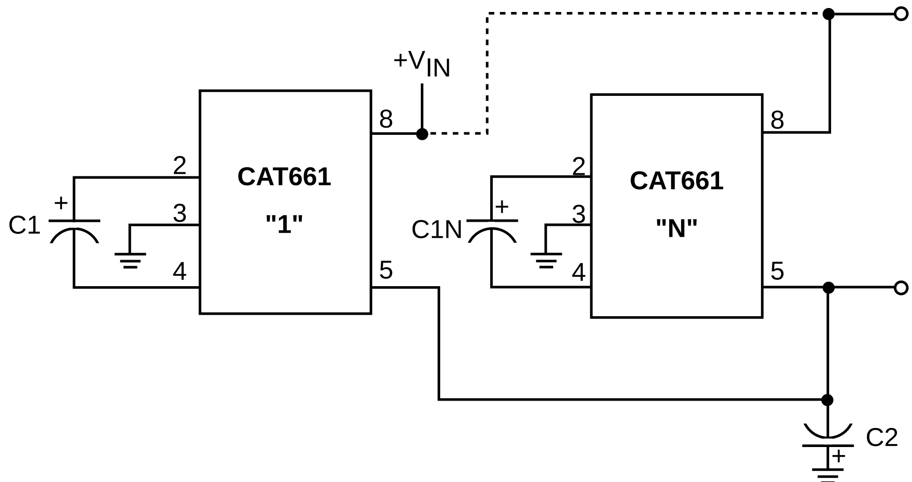
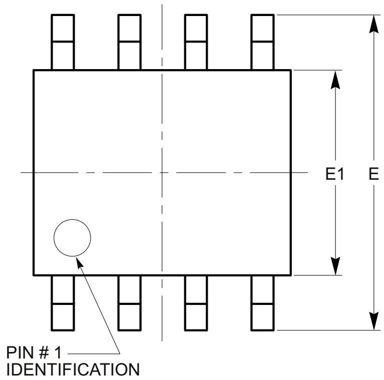


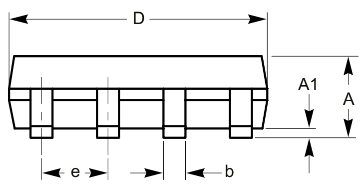
Figure 13: Reduce Output Resistance by Paralleling Devices

PACKAGE OUTLINE DRAWINGS
SOIC 8-Lead 150mils (V)

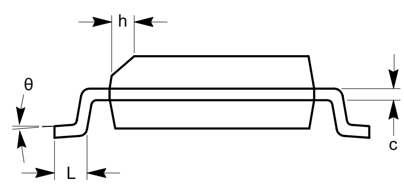


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



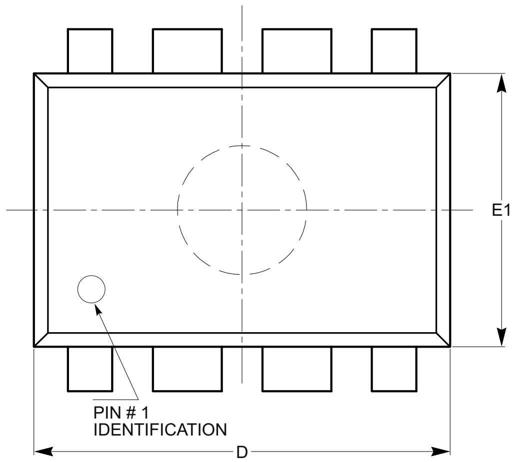
SIDE VIEW



END VIEW

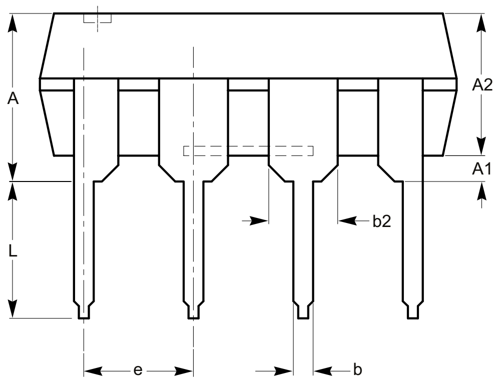
Notes:
1. Al dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC standard MS-012.

PDIP 8-Lead 300mils (L)

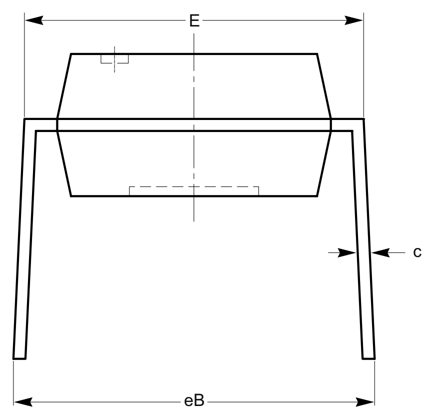


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
e	2.54 BSC		
E1	6.10	6.35	7.11
eB	7.87		10.92
L	2.92	3.30	3.80



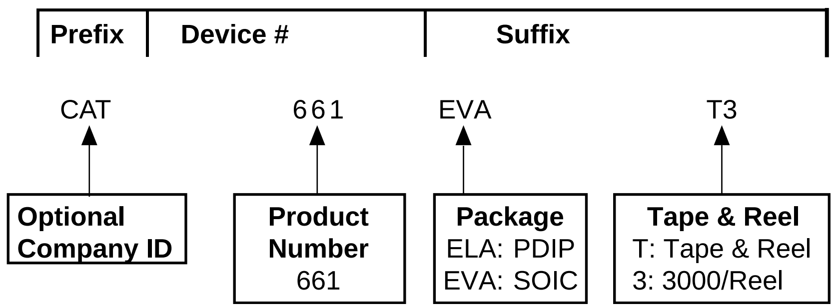
SIDE VIEW



END VIEW

Notes:
1. Al dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC standard MS-001.

EXAMPLE OF ORDERING INFORMATION



Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is Matte-Tin.
(3) The device used in the above example is a CAT661W-T3 (SOIC, Tape & Reel).

REVISION HISTORY

Date	Revision	Description
15-Oct-03	G	Updated Description - eliminated Commercial temperature range
27-Oct-04	H	Minor changes throughout data sheet
20-Jan-05	I	Changed ordering information for CAT661EXA to CAT661EVA Changed ordering information for CAT661EXA-TE13 to CAT661EVA-TE13
22-Apr-05	J	Removed Preliminary Information from data sheet header
16-Nov-07	K	Update Features and Description Update Package Outline Drawings and remove TDFN Add Example of Ordering Information Add Ordering Part Number Add "MD-" to document number
14-Nov-08	L	Update Package Outline Drawing - PDIP Change logo and fine print to ON Semiconductor

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
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