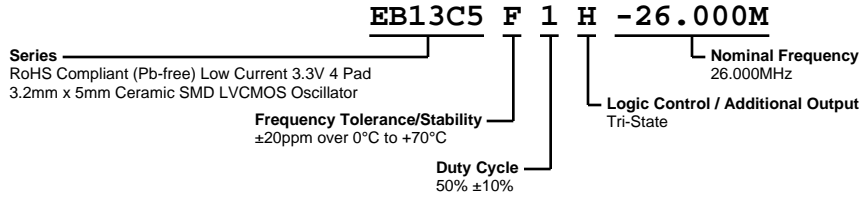


EB13C5F1H-26.000M



ECLIPTEK[®]
CORPORATION



ELECTRICAL SPECIFICATIONS

Nominal Frequency	26.000MHz
Frequency Tolerance/Stability	±20ppm over 0°C to +70°C (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration)
Supply Voltage	3.3Vdc ±10%
Input Current	5mA Maximum
Output Voltage Logic High (Voh)	90% of Vdd Minimum
Input Current Logic High (Ioh)	-1.6mA
Output Voltage Logic Low (Vol)	10% of Vdd Maximum
Input Current Logic Low (Iol)	+1.6mA
Rise/Fall Time	4nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50% ±10% (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Logic Control / Additional Output	Tri-State
Tri-State Input Voltage (Vih and Vil)	90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)
Standby Current	10µA Maximum (Disabled Output: High Impedance)
One Sigma Clock Period Jitter	25pSec Maximum
Start Up Time	10 mSec Maximum
Storage Temperature Range	-55°C to +125°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-202, Method 213, Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007, Condition A

EB13C5F1H-26.000M

MECHANICAL DIMENSIONS (all dimensions in millimeters)



PIN	CONNECTION
1	Tri-State
2	Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	E26.000 E=Ecliptek Designator
2	XXYYZ XX=Ecliptek Manufacturing Code Y=Last Digit of the Year ZZ=Week of the Year

Suggested Solder Pad Layout

All Dimensions in Millimeters



All Tolerances are ±0.1

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OUTPUT WAVEFORM & TIMING DIAGRAM



Test Circuit for CMOS Output



Note 1: An external 0.1µF low frequency tantalum bypass capacitor in parallel with a 0.01µF high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

Recommended Solder Reflow Methods



High Temperature Infrared/Convection

$T_s \text{ MAX}$ to T_L (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum ($T_s \text{ MIN}$)	150°C
- Temperature Typical ($T_s \text{ TYP}$)	175°C
- Temperature Maximum ($T_s \text{ MAX}$)	200°C
- Time ($t_s \text{ MIN}$)	60 - 180 Seconds
Ramp-up Rate (T_L to T_p)	3°C/second Maximum
Time Maintained Above:	
- Temperature (T_L)	217°C
- Time (t_L)	60 - 150 Seconds
Peak Temperature (T_p)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature ($T_p \text{ Target}$)	250°C +0/-5°C
Time within 5°C of actual peak (t_p)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1

Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T_s MAX to T_L (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T_s MIN)	N/A
- Temperature Typical (T_s TYP)	150°C
- Temperature Maximum (T_s MAX)	N/A
- Time (t_s MIN)	60 - 120 Seconds
Ramp-up Rate (T_L to T_p)	5°C/second Maximum
Time Maintained Above:	
- Temperature (T_L)	150°C
- Time (t_L)	200 Seconds Maximum
Peak Temperature (T_p)	240°C Maximum
Target Peak Temperature (T_p Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (t_p)	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum.