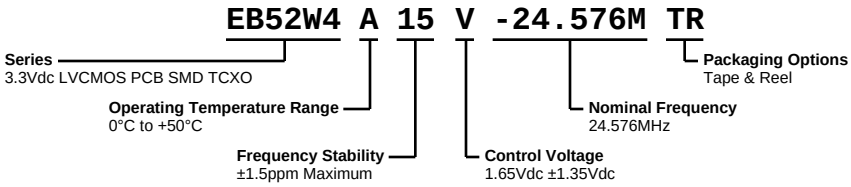
EB52W4A15V-24.576M TR



ELECTRICAL SPECIFICATIONS

Nominal Frequency	24.576MHz
Frequency Stability	±1.5ppm Maximum (Inclusive of Operating Temperature Range)
Frequency Stability vs. Input Voltage	±0.3ppm Maximum (±5%)
Aging at 25°C	±1ppm/Year Maximum
Frequency Stability vs. Load	±0.2ppm Maximum (±2pF)
Operating Temperature Range	0°C to +50°C
Supply Voltage	3.3Vdc ±5%
Input Current	20mA Maximum
Output Voltage Logic High (Voh)	90% of Vdd Minimum
Output Voltage Logic Low (Vol)	10% of Vdd Maximum
Rise/Fall Time	10nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50% ±10% (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Control Voltage	1.65Vdc ±1.35Vdc
Frequency Deviation	±7ppm Minimum, ±20ppm Maximum (Referenced to Fo at Vc=1.65Vdc; Vdd=3.3Vdc)
Transfer Function	Postive Transfer Characteristic
Internal Trim	±3ppm Minimum (Top of Can)
Modulation Bandwidth	10kHz Minimum (Measured at -3dB with a Control Voltage of 1.65Vdc)
Input Impedance	10kOhms Typical
Phase Noise	-70dBc at 10Hz Offset, -100dBc at 100Hz Offset, -130dBc at 1kHz Offset, -140dBc at 10kHz Offset, -145dBc at 100kHz Offset (Typical Values Fo=19.200MHz at 25°C at Nominal Vdd and Vc)
Storage Temperature Range	-40°C to +85°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014 Condition A (Internal Crystal Only)
Gross Leak Test	MIL-STD-883, Method 1014 Condition C (Internal Crystal Only)
Lead Integrity	MIL-STD-883, Method 2004
Mechanical Shock	MIL-STD-202, Method 213 Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007 Condition A

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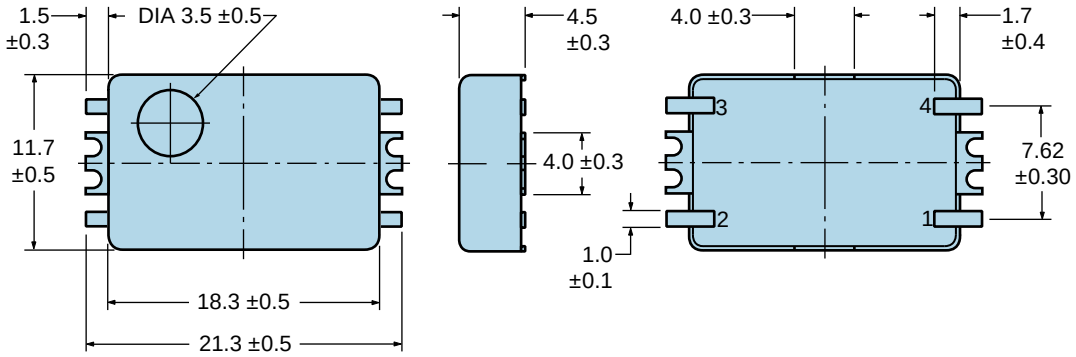
MECHANICAL DIMENSIONS (all dimensions in millimeters)

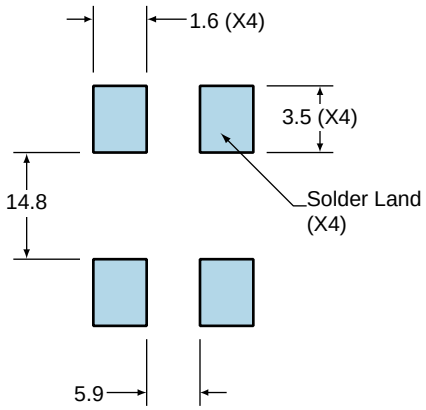


PIN	CONNECTION
1	Voltage Control
2	Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	**ECLIPTEK**
2	**24.576M** *M=MHz*
3	**XXYZZ** *XX=Ecliptek Manufacturing Code* *Y=Last Digit of the Year* *ZZ=Week of the Year*

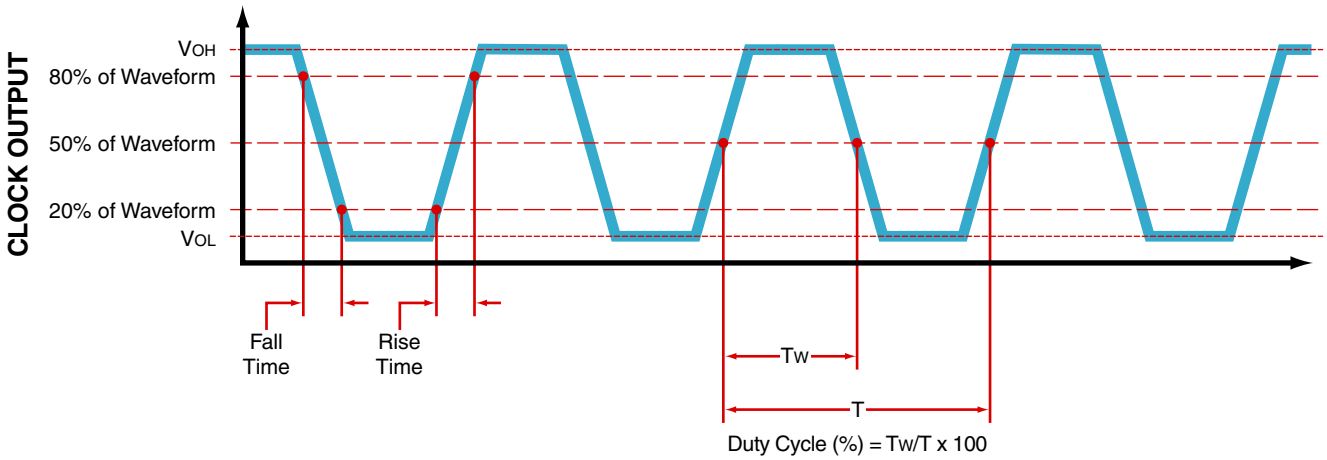
Suggested Solder Pad Layout

All Dimensions in Millimeters

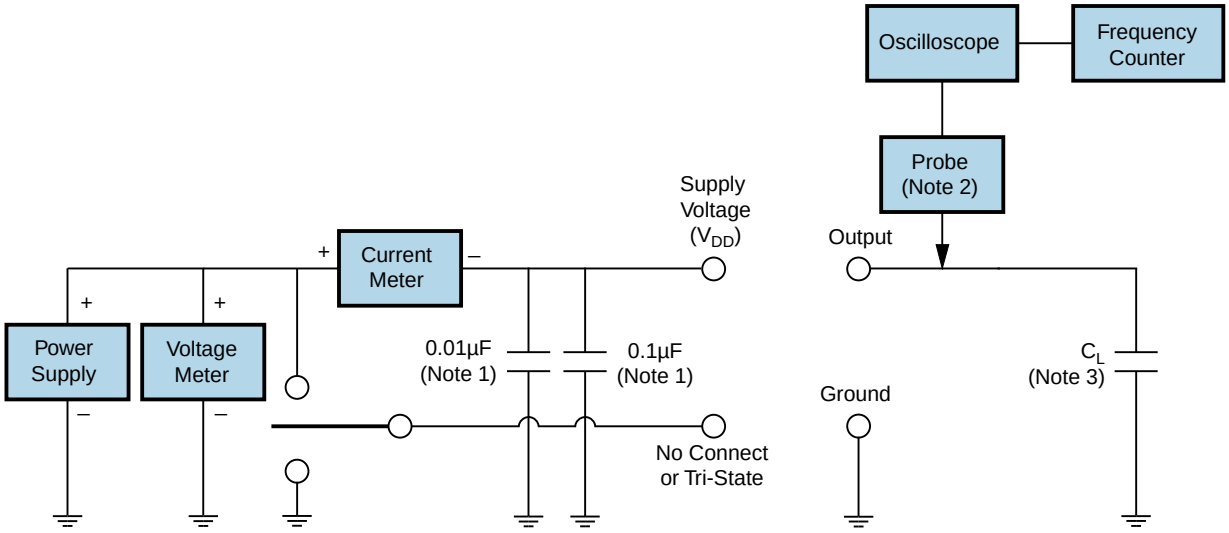


All Tolerances are ±0.1

OUTPUT WAVEFORM



Test Circuit for CMOS Output



Note 1: An external 0.1µF low frequency tantalum bypass capacitor in parallel with a 0.01µF high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.
Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

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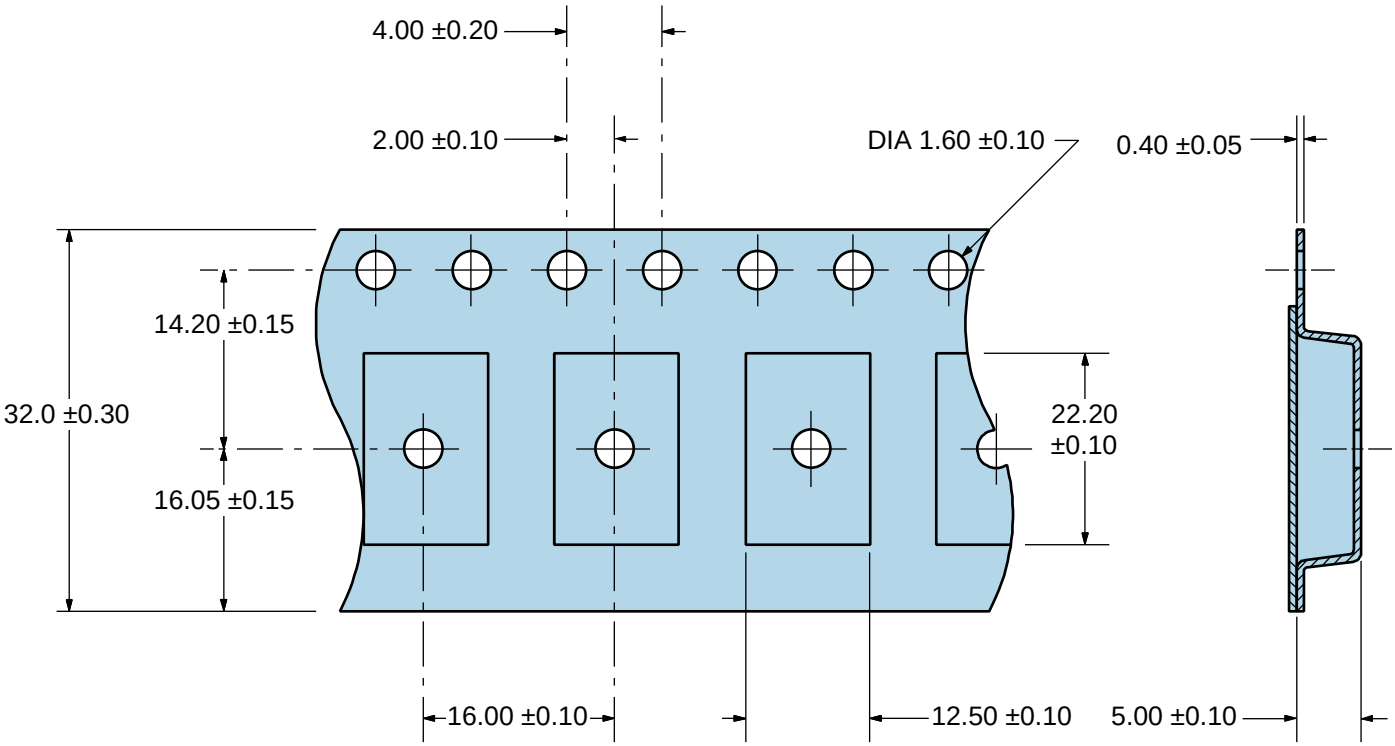
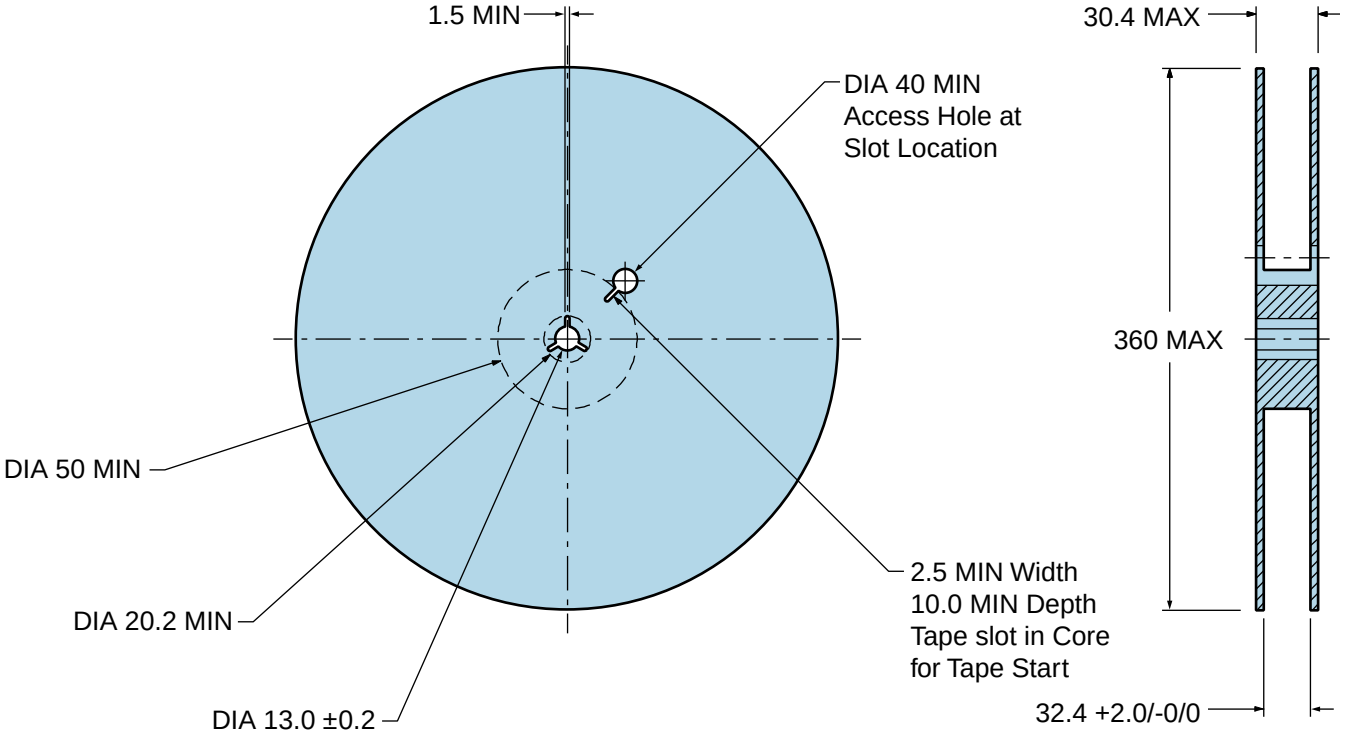
Tape & Reel Dimensions

1,000 pieces per reel



*Compliant to EIA 481A



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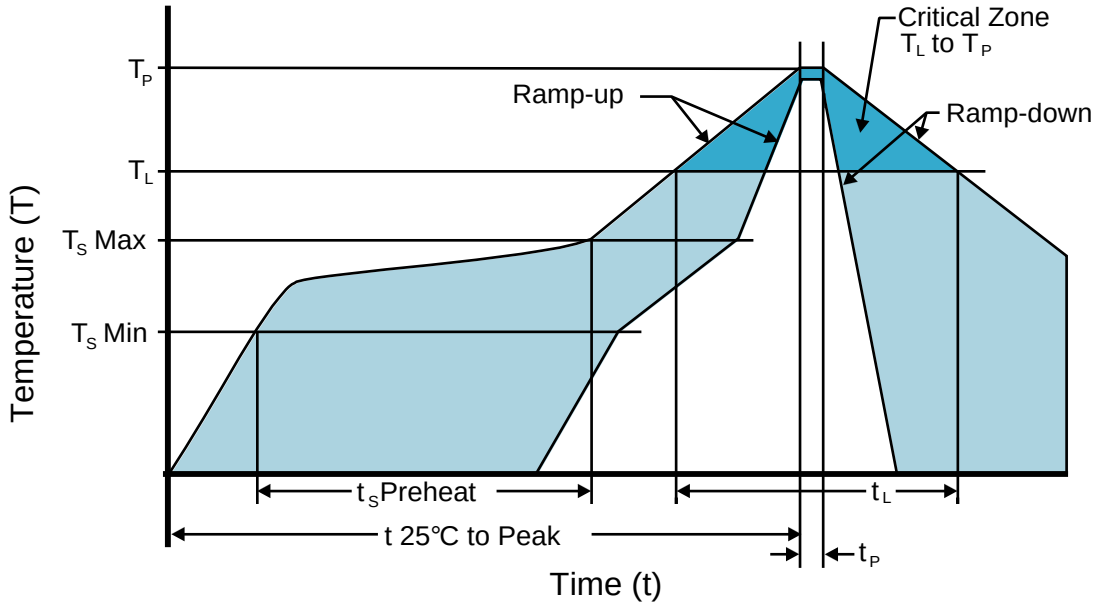
Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T_S MAX to T_L (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T_S MIN)	N/A
- Temperature Typical (T_S TYP)	150°C
- Temperature Maximum (T_S MAX)	N/A
- Time (t_S MIN)	60 - 120 Seconds
Ramp-up Rate (T_L to T_P)	5°C/second Maximum
Time Maintained Above:	
- Temperature (T_L)	150°C
- Time (t_L)	200 Seconds Maximum
Peak Temperature (T_P)	240°C Maximum
Target Peak Temperature (T_P Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (t_p)	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum.