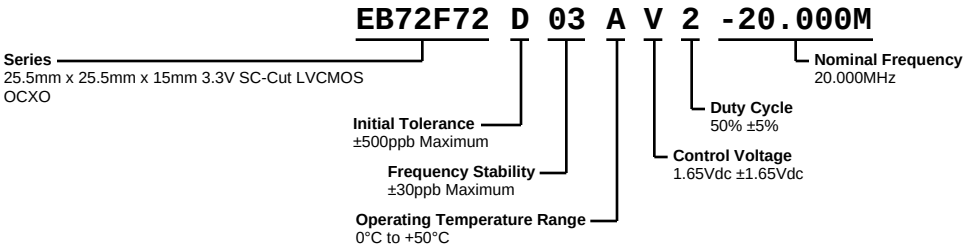
EB72F72D03AV2-20.000M

ECLIPTEK CORPORATION



ELECTRICAL SPECIFICATIONS

Nominal Frequency	20.000MHz
Initial Tolerance	±500ppb Maximum (Measured at nominal Vdd and Vc)
Frequency Stability	±30ppb Maximum
Frequency Stability vs. Input Voltage	±20ppb Maximum (Vdd ±5%)
Frequency Stability vs. Load	±20ppb Maximum (Vload ±5%)
Frequency Stability vs. Aging (10 Years)	±500ppb Maximum (after 72 hours of operation)
Frequency Stability vs. Aging (1 Day)	±2.0ppb Maximum (after 72 hours of operation)
Frequency Stability vs. Aging (1 Year)	±100ppb Maximum (after 72 hours of operation)
Operating Temperature Range	0°C to +50°C
Supply Voltage	3.3Vdc ±5%
Warm Up Time	3 Minutes Maximum (to ±50ppb of final frequency at 1 hour at 25°C)
Power Consumption	1.2Watts Maximum at Steady State at 25°C, 3.6Watts Maximum during Warm Up
Output Voltage Logic High (Voh)	2.6Vdc Minimum (IOH=-4mA)
Output Voltage Logic Low (Vol)	0.4Vdc Maximum (IOL=+4mA)
Rise/Fall Time	6nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50% ±5% (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Control Voltage	1.65Vdc ±1.65Vdc
Control Voltage Range	0.0Vdc to Vdd
Frequency Deviation	±0.5ppm Minimum (Referenced to Fo at Vc=1.65Vdc; Vcc=3.3Vdc)
Linearity	±10% Maximum
Reference Voltage Output	2.8Vdc ±0.2Vdc (Pin 4)
Transfer Function	Positive Transfer Characteristic
Crystal Cut	SC-Cut
Input Impedance	10kOhms Typical
Phase Noise	-90dBc/Hz at 1Hz Offset, -100dBc/Hz at 10Hz Offset, -130dBc/Hz at 100Hz Offset, -145dBc/Hz at 1kHz Offset, -150dBc/Hz at 10kHz Offset (Typical Values)
Storage Temperature Range	-55°C to +125°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Lead Integrity	MIL-STD-883, Method 2004
Mechanical Shock	MIL-STD-202, Method 213 Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007 Condition A

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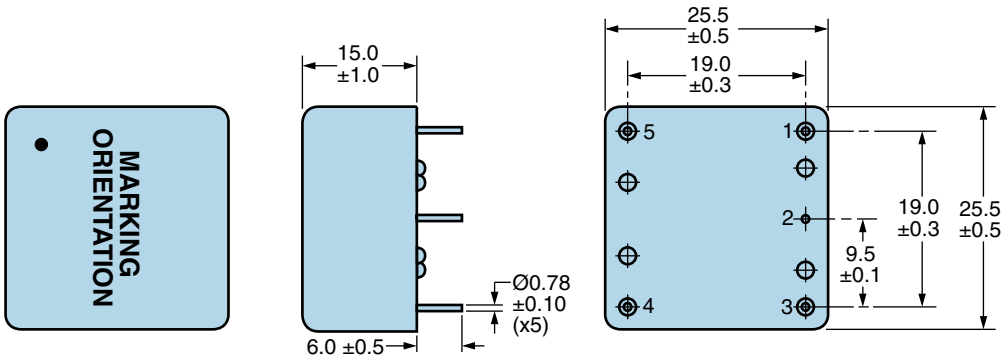
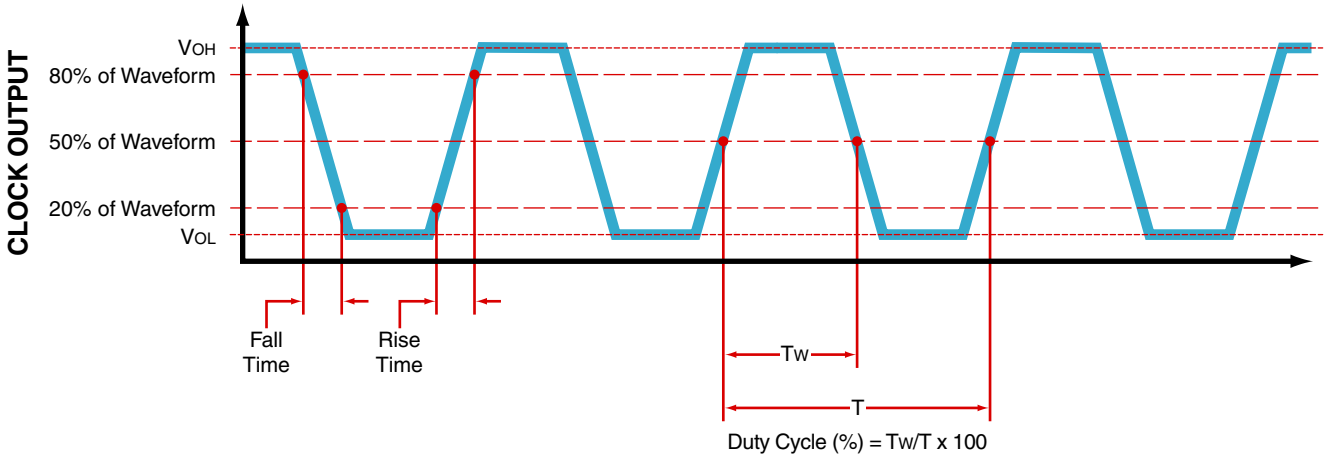
MECHANICAL DIMENSIONS (all dimensions in millimeters)



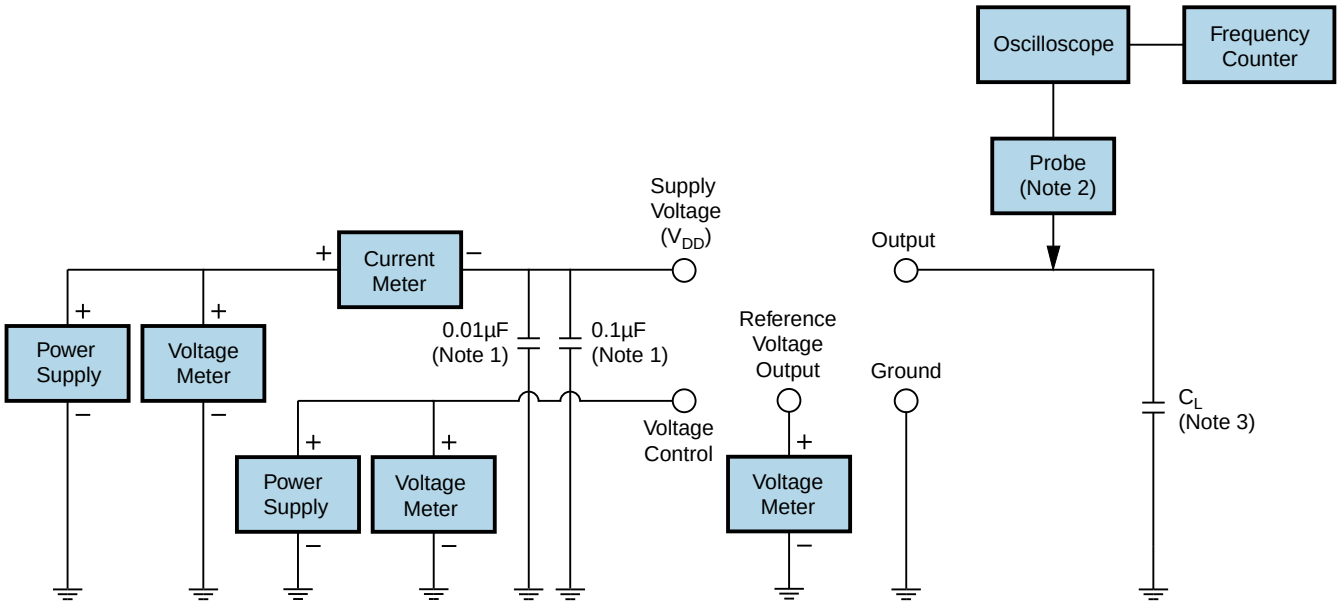
PIN	CONNECTION
1	Output
2	Case/Ground
3	Voltage Control
4	Reference Voltage Output
5	Supply Voltage

LINE	MARKING
1	**ECLIPTEK**
2	**20.000M**
3	**XXYZZ** *XX=Ecliptek Manufacturing Code* *Y=Last Digit of the Year* *ZZ=Week of the Year*

OUTPUT WAVEFORM



Test Circuit for Voltage Control Option



Note 1: An external 0.1µF low frequency tantalum bypass capacitor in parallel with a 0.01µF high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.
Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.